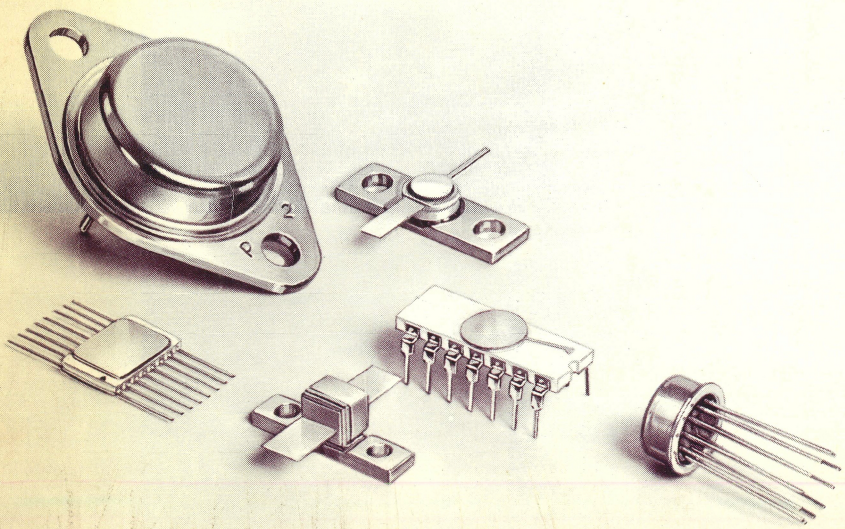
RCA Solid State

'74 DATABOOK Series

SSD-207B

High-Reliability Devices

Power Transistors
RF Power Devices
Integrated Circuits



A New Approach To Data Service... and Customer Service

1974 RCA Solid State DATABOOKS

Seven textbook-size volumes covering all current commercial RCA solid-state devices (through January 1, 1974) . . . . . $2.00 each*

SSD-201B	Linear Integrated Circuits and MOS Devices (Data only)	792 pages
SSD-202B	Linear Integrated Circuits and MOS Devices (Application Notes only)	456 pages
SSD-203B	COS/MOS Digital Integrated Circuits	528 pages
SSD-204B	Power Transistors and Power Hybrid Circuits	896 pages
SSD-205B	RF Power Devices	544 pages
SSD-206B	Thyristors, Rectifiers, and Diacs	536 pages
SSD-207B	High-Reliability Devices	576 pages

Announcement Newsletter: "What's New in Solid State" Available FREE to all DATABOOK users . . . see pages 3 and 4

"Bingo-type Response-Card Service" included with Newsletter Available FREE to all DATABOOK users . . . see pages 3 and 4

Update Mailing Service for IC's, power devices, or entire product line . . . see pages 3 and 4

Indexed Binder for Update Filing . . . see pages 3 and 4

*optional price

RCA Solid State '74 DATABOOK Series

High-Reliability Devices

This DATABOOK contains descriptive text, data, and related application notes on power transistors, rf power devices, and integrated circuits presently available from RCA Solid State Division as either standard or custom products. For ease of type selection, a complete index to these high-reliability devices is given on pages 6–7. Text material and data are then grouped according to type of devices: (a) power transistors, (b) rf power devices, (c) linear and COS/MOS integrated circuits.

A feature of this DATABOOK is the complete Guide to RCA Solid State Devices at the back of the book. This section includes a comprehensive subject index and a complete index to all standard devices in the solid-state product line: linear integrated circuits, MOS field-effect (MOS/FET) devices, COS/MOS integrated circuits, power transistors, power hybrid circuits, rf power devices, thyristors, rectifiers, and diacs. All listings include references to volume number and page number in the 1974 7-volume DATABOOK series described on the facing page.

Printed in USA/11-73

RCA Solid State | Box 3200 | Somerville, N. J., U.S.A. 08876
RCA Limited | Sunbury-on-Thames | Middlesex TW16 7HW, England
RCA s.a. | 4400 Herstal | Liege, Belgium

RCA Solid State Total Data Service System

The RCA Solid State DATABOOKS are supplemented throughout the year by a comprehensive data service system that keeps you aware of all new device announcements and lets you obtain as much or as little product information as you need — when you need it.

New solid-state devices and related publications announced during the year are described in a monthly newsletter entitled "What's New in Solid State". If you obtained your DATABOOK(s) directly from RCA, your name is already on the mailing list for this newsletter. If you obtained your book(s) from a source other than RCA and wish to receive the newsletter, please fill out the form on page 4, detach it, and mail it to RCA.

Each newsletter issue contains a "bingo"-type fast-response form for your use in requesting information on new devices of interest to you. If you wish to receive all new product information published throughout the year, without having to use the newsletter response form, you may subscribe to a mailing service which will bring you all new data sheets and application notes in a package every other month. You can also obtain a binder for easy filing of all your supplementary material. Provisions for obtaining information on the update mailing service and the binder are included in the order form on page 4.

Because we are interested in your reaction to this approach to data service, we invite you to add your comments to the form when you return it, or to send your remarks to one of the addresses listed at the top of the form. We solicit your constructive criticism to help us improve our service to you.

Order Form for "What's New in Solid State"
and for further information on Update Mailings and Binders

Please fill out just one copy of this form, and mail it to:

(a) from U.S.A. and Canada:

RCA Solid State Division
Box 3200
Somerville, N. J., U.S.A. 08876

(b) from Latin America and Far East:

RCA Solid State
International Sales
Somerville, N. J., U.S.A. 08876

(c) from United Kingdom, Europe, Middle East, and Africa:

RCA Limited
Sunbury-on-Thames
Middlesex TW16 7HW, England

or

RCA s.a.
4400 Herstal
Liege, Belgium

☐ Please add my name to the mailing list for "What's New in Solid State"

☐ Please send me details on obtaining update mailings for my DATABOOKS and a binder for filing of supplementary material.

Name ☐☐☐☐☐☐☐☐☐☐☐☐☐☐ ☐☐☐
(Last) (Initials)

Company ☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐

Address ☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐
(Number) (Street, RFD, P.O. Box)

Home ☐
Business ☐
(City) (State or Prov.)

(Country) (Zip or Pstl. Zone)

Function: (Check One)

A ☐ Executive/Administration
B ☐ Purchasing/Procurement
C ☐ Research/Development
D ☐ Design Engineer
E ☐ Application/Components Engineer
F ☐ Production/Manufacturing
G ☐ Documentation/Library
H ☐ Reliability/QA
I ☐ Education/Training
J ☐ Program/Project Management
K ☐ Marketing

Activity: (Check One)

A ☐ Broadcast
B ☐ Communication
C ☐ Instrumentation/Control
D ☐ Computer/Data Processing
E ☐ Computer, Peripheral
F ☐ Automotive
G ☐ Industrial
H ☐ Medical
I ☐ Research
J ☐ Transportation
K ☐ Consumer, Electronic
L ☐ Consumer, Appliance
M ☐ Space
N ☐ Ordnance
O ☐ Avionics
P ☐ Electronic Warfare

Product Interest:
(Indicate order of interest if more than one is marked)

A ☐ Linear IC's
B ☐ Digital IC's, COS/MOS
C ☐ Digital IC's, Bipolar
D ☐ Thyristors/Rectifiers
E ☐ Liquid Crystals
F ☐ Semiconductor Diodes
G ☐ RF Power Semiconductors
H ☐ MOSFETS
I ☐ Power Transistors
J ☐ Power Hybrid Circuits

Table of Contents

Index to High-Reliability Solid-State Devices

Type	Page	Product Line	Description
2N2102*	34	PWR	Medium-power n-p-n transistor
2N3054*	34	PWR	Hometaxial-base medium-power n-p-n transistor
2N3263*	35	PWR	High-speed n-p-n power transistor
2N3265*	35	PWR	High-speed n-p-n power transistor
2N3773*	36	PWR	Hometaxial-base n-p-n power transistor
2N3879*	36	PWR	High-speed n-p-n power transistor
2N4036*	37	PWR	Medium-power p-n-p transistor
2N5240*	37	PWR	High-voltage n-p-n power transistor
2N5262*	38	PWR	High-voltage, high-speed n-p-n transistor
2N5320*	38	PWR	General-purpose n-p-n power transistor
2N5322*	39	PWR	General-purpose p-n-p power transistor
2N5578*	39	PWR	Hometaxial-base n-p-n power transistor
2N5781*	40	PWR	General-purpose p-n-p power transistor
2N5784*	40	PWR	General-purpose p-n-p power transistor
2N5954*	41	PWR	Medium-power p-n-p transistor
2N6033*	41	PWR	High-speed n-p-n power transistor
2N6056*	42	PWR	8-A n-p-n Darlington power transistor
2N6079*	42	PWR	High-voltage n-p-n power transistor
2N6248*	43	PWR	High-power p-n-p transistor
2N6251*	43	PWR	High-voltage n-p-n power transistor
2N6385*	44	PWR	10-A n-p-n Darlington power transistor
2N6479*	45	PWR	Radiation-hardened n-p-n power transistor
2N6480*	45	PWR	Radiation-hardened n-p-n power transistor
2N6481*	45	PWR	Radiation-hardened n-p-n power transistor
2N6482*	45	PWR	Radiation-hardened n-p-n power transistor
40279	119	RF	VHF/UHF n-p-n power transistor
40294	123	RF	UHF n-p-n power transistor
40296	130	RF	UHF n-p-n power transistor
40305	137	RF	VHF/UHF n-p-n power transistor
40306	137	RF	VHF/UHF n-p-n power transistor
40307	137	RF	VHF/UHF n-p-n power transistor
40414	142	RF	UHF n-p-n power transistor
40577	148	RF	VHF n-p-n power transistor
40578	155	RF	VHF/UHF n-p-n power transistor
40605	161	RF	VHF/UHF n-p-n power transistor
40606	168	RF	VHF/UHF n-p-n power transistor
CA741/...	188	LIC	Operational amplifier
CA747/...	188	LIC	Operational amplifier
CA748/...	188	LIC	Operational amplifier
CA1558/...	188	LIC	Operational amplifier
CA3000/...	196	LIC	DC amplifier
CA3001/...	203	LIC	Video amplifier
CA3002/...	210	LIC	IF amplifier
CA3004/...	216	LIC	RF amplifier
CA3015A/...	222	LIC	Operational amplifier
CA3019/...	229	LIC	Diode array
CA3026/...	235	LIC	Dual differential amplifier
CA3028B/...	243	LIC	Differential/cascode amplifier
CA3039/...	250	LIC	Diode array
CA3045/...	255	LIC	Transistor array
CA3049/...	263	LIC	Dual differential amplifier
CA3058/...	269	LIC	Zero-voltage switch
CA3080/...	277	LIC	Operational transconductance amplifier
CA3080A/...	277	LIC	Operational transconductance amplifier
CA3085/...	285	LIC	Positive voltage regulator
CA3085A/...	285	LIC	Positive voltage regulator
CA3085B/...	285	LIC	Positive voltage regulator
CA3094/...	291	LIC	Programmable power-switch/amplifier
CA3094A/...	291	LIC	Programmable power-switch/amplifier
CA3094B/...	291	LIC	Programmable power-switch/amplifier
CD4000A/...	309	COS/MOS	Dual 3-input NOR gate plus inverter
CD4001A/...	309	COS/MOS	Quad 2-input NOR gate
CD4002A/...	309	COS/MOS	Dual 4-input NOR gate
CD4006A/...	316	COS/MOS	18-stage static shift register
CD4007A/...	321	COS/MOS	Dual complementary pair plus inverter
CD4008A/...	327	COS/MOS	4-bit full adder with parallel carry
CD4009A/...	332	COS/MOS	Hex buffer/converter (inverting)
CD4010A/...	332	COS/MOS	Hex buffer/converter (non-inverting)
CD4011A/...	339	COS/MOS	Quad 2-input NAND gate
CD4012A/...	339	COS/MOS	Dual 4-input NAND gate
CD4013A/...	346	COS/MOS	Dual "D" flip-flop with set/reset
CD4014A/...	352	COS/MOS	8-stage static shift register
CD4015A/...	357	COS/MOS	Dual 4-stage static shift register
CD4016A/...	362	COS/MOS	Quad bilateral switch
CD4017A/...	370	COS/MOS	Decade counter/divider
CD4018A/...	375	COS/MOS	Presettable divide-by-"N" counter
CD4019A/...	380	COS/MOS	Quad AND-OR select gates
CD4020A/...	384	COS/MOS	14-stage binary/ripple counter
CD4021A/...	389	COS/MOS	8-stage static shift register
CD4022A/...	394	COS/MOS	Divide-by-8 counter/divider
CD4023A/...	339	COS/MOS	Triple 3-input NAND gate
CD4024A/...	399	COS/MOS	7-stage binary counter
CD4025A/...	309	COS/MOS	Triple 3-input NOR gate
CD4026A/...	404	COS/MOS	Decade counter/divider
CD4027A/...	411	COS/MOS	Dual J-K master-slave flip-flop
CD4028A/...	417	COS/MOS	BCD-to-decimal decoder
CD4029A/...	421	COS/MOS	Presettable up/down counter
CD4030A/...	427	COS/MOS	Quad exclusive-OR gate
CD4031A/...	432	COS/MOS	64-stage static shift register
CD4032A/...	438	COS/MOS	Triple serial adder (positive logic)
CD4033A/...	404	COS/MOS	Decade counter/divider
CD4034A/...	442	COS/MOS	MSI 8-stage static shift register
CD4035A/...	449	COS/MOS	4-stage parallel in/out shift register
CD4036A/...	455	COS/MOS	4-word-x-8-bit RAM (binary addressing)
CD4038A/...	438	COS/MOS	Triple serial adder (negative logic)
CD4039A/...	455	COS/MOS	4-word-x-8-bit RAM (word-line addressing)
CD4040A/...	461	COS/MOS	12-stage binary/ripple counter
CD4041A/...	467	COS/MOS	Quad true/complement buffer
CD4042A/...	473	COS/MOS	Quad clocked "D" latch
CD4043A/...	477	COS/MOS	Quad 3-state NOR R/S latch

* High-reliability versions of these types are available on a custom basis.

Index to High-Reliability Solid-State Devices (Cont.)

Index to Application Notes

Introduction to High-Reliability Solid-State Devices

The advent of the transistor in 1948 marked a dramatic step forward in the potential reliability of electronic equipment. Much of this solid-state reliability potential has been realized and, without doubt, has played a key role in the phenomenal growth and diversification of electronics over the past two decades. In spite of this achievement, however, the demand and need for greater reliability assurance in solid-state devices continues to grow.

Electronic systems continue to grow more complex as more comprehensive functions are provided. In the process, greater quantities, or more sophisticated and complex devices are used. The development cycle for systems continues to decrease so that less and less time is available for component reliability testing in operating systems. Electronics systems are becoming interlocked with huge dollar investments, with the social and political fabric of society, and with vital national security to such a degree that a system failure may have immediate and visible impact. Consumers are demanding better warranties at a time when service costs are rising rapidly. Further, a dynamic solid-state technology rapidly generates new devices that offer even greater functional and reliability potential.

Solid-state devices classified as high-reliability types have come to be primarily associated with military and aerospace applications. In many ways, this association is misleading because the commercial equipment market is probably the largest user of high-reliability products, but not necessarily by that label. Military and aerospace agencies, however, have been largely responsible for establishment of comprehensive published reliability specifications and standards which have been accepted by the solid-state industry. MIL standards dominate the procedures used to specify high-reliability solid-state devices and represent a common reference point frequently used by commercial users to define their requirements.

Commercial High-Reliability Requirements

The dominant market for solid-state devices today is commercial. The bulk of the parts produced are initially designed, developed, and manufactured to meet specific functional, quality, and reliability needs of a class of commercial electronic equipment. Commercial equipment tends to be evolutionary and to be produced continuously over longer periods and in larger quantities than is the case with equipment for military and aerospace systems. At the outset, the commercial user is more likely, than is the military and aerospace user, to be involved in influencing the solid-state device manufacturer to his particular functional and economic requirements. His opportunity to evaluate early devices and influence corrective measures for his application is greater. All these factors enhance the ability of both the solid-state manufacturer and the user to reach a balance between reliability and economics which matches a particular need.

One of the most important factors, which brings lower cost to the commercial user without sacrifice in reliability, is his ability, together with that of the manufacturer, to identify accurately over a period of time a few relatively simple controls and/or screens which can be used to effectively eliminate potential failures in his particular application. This ability is possible because his application is specific and continuous, and device volumes are considerable. The commercial user generally achieves the reliability he requires without elaborate specifications and with a minimum of administrative procedures.

Military and Aerospace High-Reliability Requirements

Military and aerospace requirements for high-reliability solid-state devices are extremely large and diverse, not only in terms of performance, operating conditions, and reliability, but also in terms of logistics and procurement. As a result of these requirements, the military services have jointly developed specifications and standards under which most military end-use solid-state devices are procured. To simplify procurement, logistics, and the development of reliability data, MIL specs are not issued for the full spectrum of devices manufactured; rather, they are restricted to those devices for which significant need is demonstrated and are specified so that the device can have as wide applicability as possible. Although the limits for operating conditions may exceed those required for some applications, they simplify procurement and assure a supply of devices for the majority of military equipment. These standards also cover a wide range of requirements for the manufacturer on such things as:

(a) The procedure and requirements for a manufacturer to become certified to manufacture MIL-spec parts.

(b) The requirements for qualifying parts.

(c) Product-assurance provisions in such areas as quality control, inspection procedures, personnel training, cleanliness, failure analysis, and documentation.

(d) Test methods and procedures.

(e) Marking and identification of product.

(f) Preservation and packing.

A large number of transistor types are covered by published military specifications. Specifications for microcircuits (integrated circuits) are relatively new, and only a limited number of military specifications have been approved and issued. Many types of devices, both transistors and integrated circuits, are not covered by military specifications, either because they are too new

or are not used in sufficient quantities. Many of these devices offer the most recent technological advances or have special performance characteristics which offer advantages to the designer of high-reliability equipment. RCA cooperates with the users of such devices in establishment of high-reliability specifications, patterned after MIL standards, which allow these devices to be approved for use in military and aerospace systems, as well as commercial equipment. If the use warrants, these specifications may be submitted by RCA, or the user, to the cognizant military specification agency as candidates for MIL approval as a standard type.

Most procurements of solid-state devices for military systems are made by the equipment contractor from the MIL-STD parts list as awards are received for electronic equipment. Some military and aerospace programs, because of their size, duration, or special requirements (Minuteman and Apollo are two examples), require that special specifications and process methods, or even special production lines, be established and tailored to the particular functional, reliability, and economic needs of the program. RCA Solid State Division has frequently used the resources of its laboratories, production facilities, and expert technical staff to contribute to the success of such programs.

Military Specifications

There are two major military specifications used for the procurement of standard solid-state devices by the military. These specifications are MIL-S-19500, which covers devices such as discrete transistors, thyristors, and diodes, and MIL-M-38510, which covers microcircuits, both hybrid and monolithic.

MIL-S-19500 is the specification for the familiar "JAN" transistors. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center. At present, approximately five hundred detailed electrical specifications are included in the MIL-S-19500 system.

Three levels of reliability, JAN, TX, and TXV, are defined by MIL-S-19500. Devices designated as JAN types receive lot screening only and are the least expensive. Devices designated as TX receive some 100-per-cent screening (primarily burn-in) and a tight lot-sampling plan. Not all detailed specifications include TX requirements. Devices designated as TXV are tested the same as TX devices; however, they receive an additional visual inspection prior to sealing the package. Only a few detailed specifications include TXV testing.

The Defense Electronic Supply Center maintains a "Qualified Products List" of all vendors qualified to produce devices in accordance with MIL-S-19500. This list is published periodically and is available to manufacturers of military equipment. NASA, to date, has not been a heavy user of MIL-S-19500, preferring instead to procure devices to their own specifications.

MIL-M-38510 is the relatively new military specification for microcircuits. This specification is far more demanding than MIL-S-19500 and presently only a few vendors have parts on the Qualified Products List. MIL-M-38510 also defines three levels (classes A, B, and C) of reliability testing. These levels, however, are markedly different from those defined by MIL-S-19500. Class A, the highest level, is intended primarily for flight and other highly critical applications. Class A devices undergo a lengthy list of 100-per-cent screens, plus a tight lot-sampling plan. Class B devices are intended for general military usage and undergo less (but still extensive) 100-per-cent testing than Class A units. Class C devices undergo the least amount of 100-per-cent testing and are, of course, the least expensive.

Approximately 40 detailed specifications are currently included in the MIL-M-38510 system. A Qualified Products List for these devices is maintained by the Defense Electronic Supply Center. NASA is now starting to use MIL-M-38510 specifications.

Both MIL-M-38510 and MIL-S-19500 attempt to make available to the designer of military equipment a list of standard, qualified, general-purpose parts which are acceptable to the military. Although MIL-S-19500 and MIL-M-38510 do not cover every solid-state device available on the market, and do not attempt to do so, enough devices are available to build the majority of military equipment. Use of these devices makes the job of spare-parts inventory far simpler for the military and the job of specification negotiations far easier for the equipment manufacturer.

High-Reliability Power Transistors

High-Reliability Power Transistors

A number of factors such as second breakdown, power dissipation, current and voltage ratings, maximum operating areas, temperature, and thermal-fatigue considerations affect the performance and reliability of power transistors in various circuit applications. These factors define the maximum limits of reliable transistor operation for both steady-state and pulsed conditions. Each of these factors must be given careful consideration in the development and production of power transistors for military, aerospace, and critical industrial applications for which high reliability is a prime objective. In such applications, replacement of defective parts is often difficult or impossible or may result in considerable expense. Care must be taken to assure that field failure rates are held to an absolute minimum. The following guidelines should be followed in an effort to achieve this objective.

Electrical Considerations:

Voltage Breakdowns	Device voltages should be limited to 70 per-cent of the maximum rates values.
Current Gain	A margin of 15 to 20 per cent above the required values should be provided to allow for degradation.
Second-Breakdown Energy Tests	Sufficient $I_{s/b}$ protection must be provided for forward-bias conditions and sufficient $E_{s/b}$ protection must be provided for inductive circuits.

Reliability Considerations:

High-Temperature Tests	Such tests are required to guarantee high-temperature performance.
Low-Level Leakage Tests	Test for stability.
Delta Temperature Tests	Adequate heat sinks must be provided so that case temperature is held to a minimum.
Operating Temperature	Device operating temperatures should be limited to 50 to 75 per cent of maximum rated values.
Transistor Protection	Circuits should include provisions to protect power transistors against electrical transients.

Second Breakdown

Second breakdown is a potentially destructive phenomenon that can occur in all power transistors within the maximum current and voltage ratings of the device. A simplified explanation is that localized thermal regeneration occurs, and the transistor exhibits a lower value of breakdown voltage, referred to as the "second breakdown". The lower value of voltage results from thermal generation of charge-carrier pairs (holes and electrons) at high localized temperatures which alter the conductivity of the semiconductor in that vicinity. This localized effect reduces the ability of the transistor to support the applied voltage. Fig. 2-1 shows qualitatively what happens under primary or second breakdown.

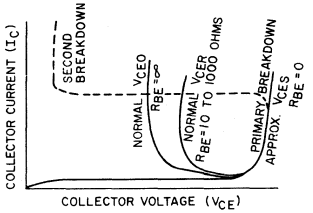


Fig. 2-1– Primary and secondary breakdown voltages.

Reverse-Bias Second Breakdown—Reverse-bias second breakdown is a phenomenon that may occur when the collector current continues to flow under reverse-bias conditions and causes the injected current to be concentrated in the central portions of the emitter, in contrast to the normal edge injection of the current. If the injected current is severely restricted to a very small central area by a large reverse emitter-base bias, the current density can rise to very large levels—in the order of thousands of amperes per square centimeter. If the collector of the transistor is of high-resistivity silicon, the high current density may inject a density of charge carriers that is equal to or greater than the collector impurity density. In this local region, the base widens and the collector depletion layer expands until the injected current density is smaller than the collector impurity density. If the current density is sufficiently high, the collector depletion layer expands to a more heavily doped collector region, such as an epitaxial substate. When the collector depletion layer expands, the collector breakdown voltage is governed by the impurity gradient related to the base doping and the heavily doped collector. The collector breakdown voltage normally supports only a fraction of the original

voltage, and the second-breakdown voltage results. The thermal effects from the large current densities also contribute to the regeneration process. Fig. 2-2 shows the process of reverse-bias second breakdown.

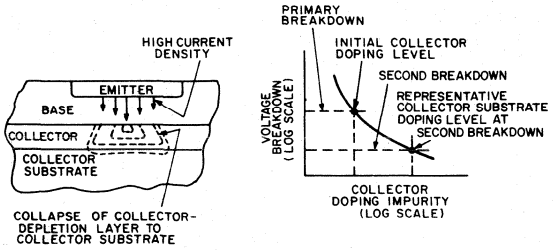


Fig. 2-2– Reverse-bias second breakdown.

In an inductive circuit, a situation exists such that collector current flows in the forward direction while the transistor is being turned off, and a high voltage is induced across the device. As a result, the transistor enters the sustaining region. The hot spot that forms during reverse-bias second breakdown may then be generated by current crowding in the depletion region, as shown in Fig. 2-3.

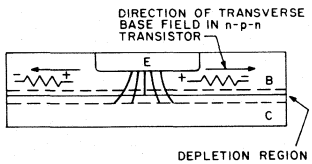


Fig. 2-3– Cross section showing current crowding that occurs during reverse-bias second breakdown.

The reverse base current that flows laterally through the base region creates an electric field. For an n-p-n transistor, electrons flow from the emitter to the collector across the base region. The field causes these carriers to flow mainly from the center of the emitter, because the emitter-base forward bias is greatest at this point. Because the device is in the sustaining region as a result of circuit conditions, a depletion region is present. Carriers (electrons) that flow across this region, which resembles two plates of a capacitor, decrease in potential. Therefore, energy is transformed to heat and causes a hot spot and possibly reverse-bias second breakdown ($E_{S/b}$). Typical examples of this situation are circuits, such as those shown in Fig. 2-4, in which an unclamped inductive load or a non-commutated leakage inductance is present.

Anything that increases the transverse base field aggravates hot-spot formation. Therefore, higher reverse base currents that result from decreased base-drive resistance or higher reverse voltages diminish $E_{S/b}$ capability, as shown in Fig. 2-5. This figure shows the effect of variations in the external base-to-emitter resistance R_{BE}, the reverse base-to-emitter voltage V_{BE}, and the load inductance L.

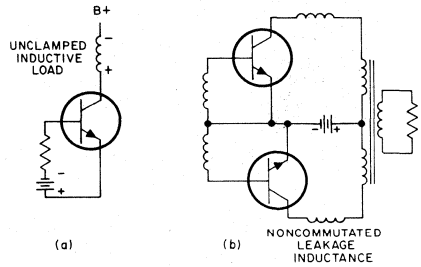


Fig. 2-4– Examples of (a) unclamped inductive loads and (b) uncommutated leakage inductance.

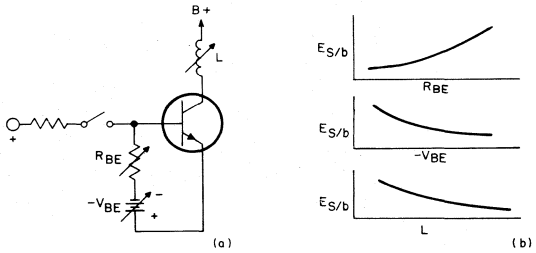


Fig. 2-5– (a) Typical inductive-load circuit and (b) variation of second-breakdown capability as a function of circuit parameters.

A test set which makes the measurement of reverse-bias second breakdown possible and also protects the transistor being tested is shown in Fig. 2-6. A test cycle includes the following steps:

1. The transistor is driven to the desired collector-current level in saturation.
2. The transistor is reverse-biased.
3. The transistor enters the sustaining region, VCEX(sus).
4. Energy is absorbed by the transistor.

If failure occurs, high-frequency noise is sensed at the base of the transistor. A "crowbar" (transistor) in parallel with the transistor being tested is then turned on, and energy is shunted through this "crowbar" to protect the transistor undergoing the test. Fig. 2-7 shows the voltage-current relationship during the reverse-bias second-breakdown ($E_{S/b}$) test.

Forward-Bias Second Breakdown—Forward-bias second breakdown is somewhat different from reverse-bias second breakdown. As shown in Fig. 2-8, the localized heating results because the current density J crosses the depletion region (collector field) V_c to yield a power density P. As P increases, more current

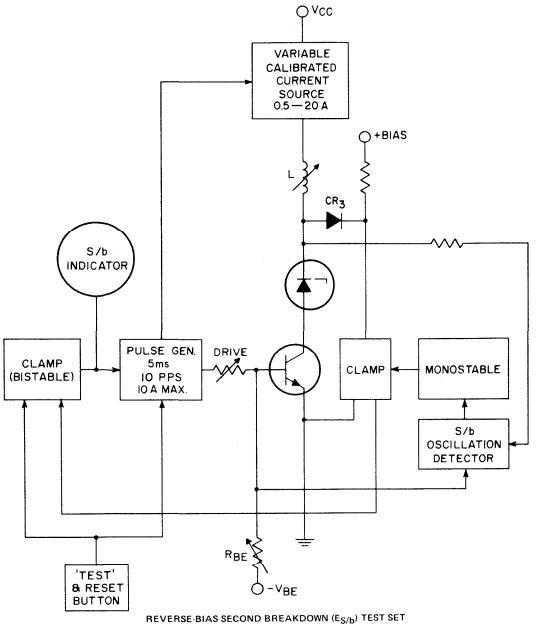


Fig. 2-6– Reverse-bias second-breakdown ($E_{S/b}$) test set.

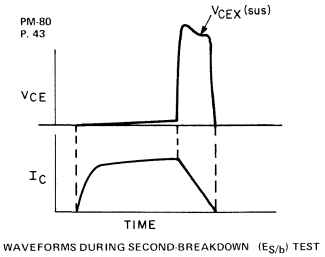


Fig. 2-7– Waveforms during second-breakdown ($E_{S/b}$) test.

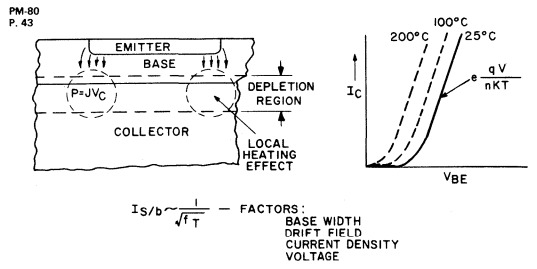


Fig. 2-8– Forward-bias second breakdown.

is injected into the localized area. The increase in current is caused by a decrease in the localized V_{BE}, at an approximate rate of 2 millivolts per °C. The local system becomes regenerative as more heat from the increased power density reduces V_{BE} and thereby increases the current injection.

The forward-bias second-breakdown current, $I_{S/b}$, is defined as the current at the onset of second breakdown, and is closely related to the collector field V_c, the current density J, and other properties of the transistor. Forward-bias second breakdown is also related to charge-carrier transit time across the base region, and is controlled by base width and any accelerating fields that exist in the base. The longer the transit time required for the charge carrier to cross the base, the more lateral diffusion of the charge and thus the greater the reduction in the current density at the edge of the collector depletion layer. This diffusion effect, referred to as "fan-out," is enhanced by wide base widths and homogeneously doped bases. Because the forward-bias second breakdown is related to the base width, it is also related to frequency response. For a given structure, this frequency relationship is expressed by the following empirical equation:

$$I_{S/b} \approx \left(\frac{1}{\sqrt{f_T}}\right)K$$

Operation in the forward-bias region subjects the transistor to simultaneous current and voltage. This condition causes current concentrations as previously discussed. This type of rating must be considered for all linear applications of transistors.

The block diagram of a nondestructive second-breakdown test set is shown in Fig. 2-9. The transistor under test is in series with a pass transistor and is driven by a differential amplifier at a current level selected by the operator. The level selected is independent of transistor current-transfer ratio. The pass transistor is operated out of saturation, so that fast turn-off is possible. A second differential amplifier senses the voltage across the pass transistor and the 1-ohm resistor in series with it. This voltage is held constant throughout the test to improve the accuracy of the second-breakdown voltage reading. The circuit is arranged so that only the collector current of the transistor under test passes through the 1-ohm resistor. The voltage across this resistor, therefore, provides an accurate indication of collector current.

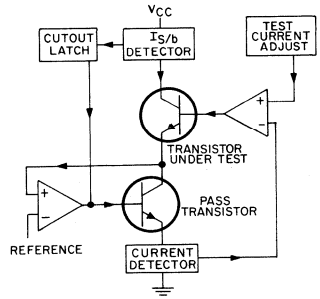


Fig. 2-9– Block diagram of test set for forward-bias second-breakdown current ($I_{S/b}$).

The onset of second breakdown is detected by use of the primary of a pulse transformer connected in series with the collector of the transistor under test. Under second-breakdown conditions, the rapid rate of rise of collector current induces a voltage L(di/dt) in the transformer secondary which is coupled to the input circuit of the series pass transistor. This voltage turns off the series pass transistor in one microsecond. Simultaneously, a voltage is developed across the transformer primary of a polarity that immediately reduces the voltage across the transistor under test. The inductance of the transformer also aids in limiting immediate current rise in the transistor being tested.

The test-set characteristics, together with the protective cutout circuit, prevent damage to the transistor during the second-breakdown test. The complete cutout time of the actual test set is approximately one microsecond; this value is sufficient to prevent destruction of any transistor currently available.

The pulse width of the voltage and current applied to the transistor under test can be varied from 0.5 millisecond to several seconds. For dc second-breakdown tests, a pulse width of 0.5 to 2 seconds is required because the thermal time constant of the power-transistor pellet and mounting block may be several tenths of a second.

A comparison of energy-handling capability for several transistor structures is shown in Table 2-1.

Table 2-1-Comparison of Energy-Handling Capability

	I_C x V_{CEO} (1-Second pulse)	Forward Bias Energy Handling at V_{CEO} Limit J	Reverse-Bias Energy $E_{S/b}$ mJ
	Doped - $\pi\nu$		
2N5240	0.08 x 300	24	1.6
2N5840	0.02 x 350	7.0	0.45
	Double-diffused, double-epitaxial		
2N5038	0.25 x 90	22.5	13
2N5672	0.12 x 120	14.4	20
2N6032	0.05 x 120	6	40
2N3879	0.09 x 75	6.85	1.0
	Hometaxial- Base		
2N5578	1.5 x 70	105	800
2N3055	1.9 x 60	115	170
2N3773	0.6 x 140	84	310

Inductive Voltage-Breakdown Testing

In most practical applications of transistors, the highest voltage that appears across the transistor results from the turn-off of the transistor, because the transistor switches from a high-current "on" state to a "cut-off" state. Inductive testing simulates this condition very closely, as shown in Fig. 2-10. Curve-tracer testing, on the other hand, subjects the transistor to an increasing voltage until the required current is achieved; i.e., the

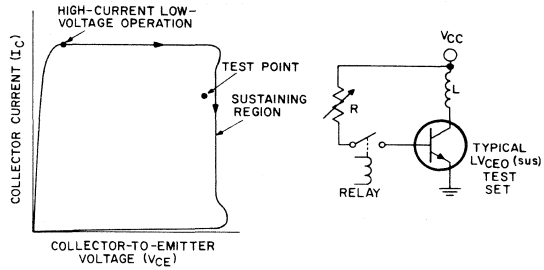


Fig. 2-10– Inductive voltage-breakdown testing of a transistor: (a) load line; (b) test circuit.

high-current, high-voltage measuring point is approached from the other direction with the collector current I_C lagging the collector-to-emitter voltage V_{CE}, as shown in Fig. 2-11. Unless sufficient current is supplied to the place the transistor in the sustaining region, the breakdown voltage measured is artificially high. If this high current is passed through a transistor with a high breakdown voltage, a high dissipation results. This dissipation is not uniformly distributed over the whole junction, but tends to concentrate in the spots with the lowest breakdown. This concentration is further aggravated when the base-to-emitter junction is reverse-biased. The small areas that break down first form hot spots. These hot spots result in further current concentration with time, and possible device destruction. Fig. 2-12 shows the test circuit used in the curve-tracer test.

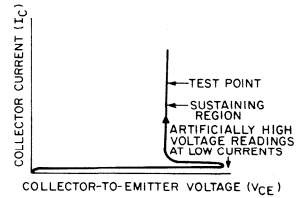


Fig. 2-11– Load line for curve-tracer voltage-breakdown testing.

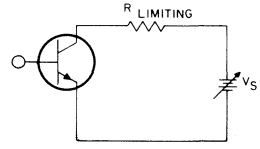


Fig. 2-12– Test setup for curve-tracer voltage-breakdown testing.

The 8-millisecond sweep of a curve tracer is relatively slow compared to inductive sweeping. This sweep allows time for the current to concentrate and to deliver an appreciable and variable amount of energy. Inductive testing, on the other hand, delivers a relatively fixed amount of energy in a short time (0.6 millisecond maximum for the 2N4348 transistor). Less concentration of current is allowed, and the test is potentially less destructive and provides a more realistic rating. Curve-

tracer testing may reject transistors that will operate satisfactorily in any practical application because the opportunity for the occurrence of hot spots is increased, and lower values of V_{CEO} are measured.

Effect of Temperature on Silicon Transistors

The characteristics of transistors vary with changes in temperature. In view of the fact that most circuits operate over a wide range of environments, a good circuit design should compensate for such changes so that operation is not adversely affected by the temperature dependence of the transistors.

Current Gain—The effect of temperature on the gain of a silicon transistor is dependent upon the level of the collector current, as shown in Fig. 2-13. At the lower current levels, the current-gain parameter h_{FE} increases with temperature. At higher currents, however, h_{FE} may increase or decrease with a rise in temperature because it is a complex function of many components.

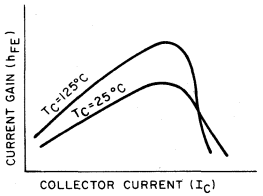


Fig. 2-13– Current gain as a function of collector current at different temperatures.

Base-to-Emitter Voltage—Fig. 2-14 shows the effect of changes in temperature on the base-to-emitter voltage (V_{BE}) of silicon transistors. Two factors, the base resistance ($r_{bb'}$) and the height of the potential barrier at the base-emitter junction ($V_{BE'}$), influence and behavior of the base-to-emitter voltage. As the temperature rises, material resistivity increases; as a result, the value of the base resistance $r_{bb'}$ becomes greater. The barrier potential $V_{BE'}$ of the base-emitter junction, however, decreases with temperature. The following equation shows the relationship between the base-to-emitter voltage and the two temperature-dependent factors:

$$V_{BE} = I_B r_{bb'} + V_{BE'}$$

$$= \frac{I_C}{h_{FE}} r_{bb'} + V_{BE'}$$

As indicated by this equation, the base-to-emitter voltage diminishes with a rise in temperature for low values of collector current, but tends to increase with a rise in temperature for higher values of collector current.

Collector-to-Emitter Saturation Voltage—The collector-to-emitter saturation voltage $V_{CE}(sat)$ is affected primarily by collector resistivity (ρ_C) and the

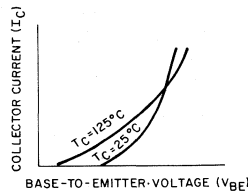


Fig. 2-14– Collector current as a function of base-to-emitter voltage at different temperatures.

amount by which the natural gain of the device (h_{FE}) exceeds the gain with which the circuit drives the device into saturation. This latter gain is known as the forced gain (h_{FEf}).

At lower collector currents, the natural h_{FE} of a transistor increases with temperature, and the IR drop in the transistor is small. The collector-to-emitter saturation voltage, therefore, diminishes with increasing temperature if the circuit continues to maintain the same forced gain. At higher collector currents, however, the IR drop increases, and gain may decrease. This decrease in gain causes the collector-to-emitter saturation voltage to increase and possibly to exceed the room-temperature (25°C) value. Fig. 2-15 shows the effect of temperature on the collector-to-emitter saturation voltage.

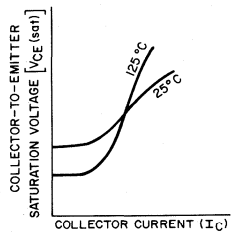


Fig. 2-15– Collector current as a function of collector-to-emitter saturation voltage at different temperatures.

Collector Leakage Currents—Reverse collector current is a resultant of three components, as shown by the following equation:

$$I_R = I_D + I_G + I_S$$

Fig. 2-16 shows the variations of these components with temperature.

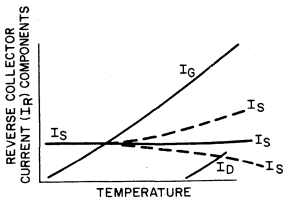


Fig. 2-16– Reverse collector current as a function of temperature.

The diffusion or saturation current I_D is a result of carriers that diffuse to the collector-base junction and are accelerated across the depletion region. This component is small until temperatures near 175°C are reached. The component I_G results from charge-generated carriers that are created by the flow of diffusion carriers across the depletion region. This component increases rapidly with temperature. I_D and I_G are referred to as bulk leakages. The term I_s represents surface leakage which is caused by local inversion, channeling, ions, and moisture. This leakage component is dependent on many factors, and its variations with changes in temperature are difficult to predict.

At low temperatures, either surface or bulk leakage can be the dominant leakage factor, particularly in transistors that employ a mesa structure. At high temperatures, charge-generated carriers and diffusion current are the major causes of leakage in both mesa and planar transistor structures; the current I_G, therefore, is the dominant leakage component. Because of the dominance of surface leakage I_s at low temperatures and the fact that this leakage may vary either directly or inversely with temperature, it is not possible to define a constant ratio of the leakage current at low temperatures to that at high temperatures. In view of the fact that power transistors are normally operated at high junction temperatures, it is more meaningful to compare the leakage characteristics of both mesa and planar transistors at high temperatures. The relative reliability of different types of power transistors, which is in no way related to the magnitude of low-temperature leakage current, is also best compared at high temperatures.

Pulsed Safe-Area Systems

On the basis of the heat storage in the thermal mass of the silicon chip and its mounting system, the peak power-handling capability of transistors increases with decreases in pulse duration. Fig. 2-17 shows normalized thermal resistance N_R as a function of time for a specific transistor and indicates that power substantially higher than rated steady-state values may be applied for short periods of time without exceeding the maximum rated junction temperature. These values of increased power correspond to $(1/N_R)$ $P_{(dc)}$, where $1/N_R$ is the normalized power multiplier and $P_{(dc)}$ is the steady-state power rating at the case temperature of interest.

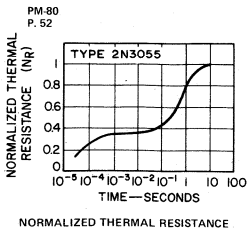


Fig. 2-17– Normalized thermal resistance.

The dissipation-limited region of the pulsed safe-area rating chart shown in Fig. 2-18 is prepared by use of the normalized thermal resistance from the following equation:

$$P_{diss} = [T_{J(max)} - T_C] / \theta_{J\text{-}C}(N_R)$$

This equation indicates a constant-power curve which can be represented on a log-log volt-ampere graph by a straight line that has a slope of -1 (from $I = PV^{-1}$).

The pulsed power curves are usually calculated and then verified by nondestructive tests along the constant-power curves from low to higher voltages. When dissipation is the only limiting factor, the -1 slope is continued to the transistor forward-biased avalanche breakdown voltage rating, at which point $V_{aM} = 1$ and may be approximated by $V_{CEO(sus)}$. When second breakdown ($I_{s/b}$) is the limiting factor, the slope changes from -1 to a higher value, usually between -1.5 and -4, according to the following relationship:

$$I_{S/b} = PV^{-N}$$

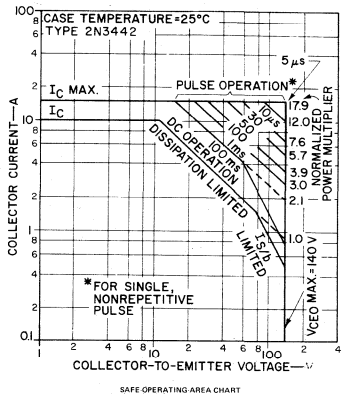


Fig. 2-18– Safe-operating-area chart.

Fig. 2-19 shows the derating curve for operation of a power transistor at case temperatures above 25°C. The $I_{s/b}$ limit is derated less with increasing temperature than the dissipation limit because the concentration of current that results in circuit breakdown is less severe than dissipation factors as temperature increases.

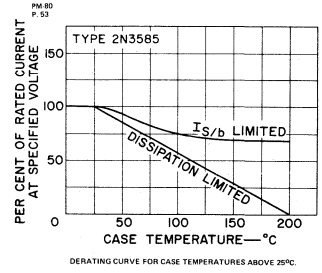


Fig. 2-19– Derating curve for case temperatures above 25°C.

For pulsed operation, the derating factor shown in Fig. 2-19 must be applied to the appropriate curve on the safe-area rating chart. For the derating, the effective case temperature T_C(eff) may be approximated by the average junction temperature T_j(av). The average junction temperature is determined as follows:

$$T_j(av) = T_C + P_{AV}(\theta_{J\text{-}C})$$

This approach results in a conservative rating for the pulsed capability of the transistor. A more accurate determination can be made by computation of actual instantaneous junction temperatures.

Depending upon whether time markers can be placed along the load line, two methods are available to determine whether a transistor will be operated within its safe-area limits in a given circuit.

1. Without Time Markers: The energy of the load line is concentrated at a single point (I_W, V_W) at which the greatest load-line penetration outside the safe area occurs. Multiplication of the waveforms of collector current I_C and the collector-to-emitter voltage V_{CE} yields a waveform of instantaneous power as a function of time. Integration of one cycle of this instantaneous-power waveform results in an energy E. The width (t_p) of an equivalent pulse may be determined as follows:

$$t_p = E/V_W I_W$$

The voltage V_W, the current I_W, and the pulse width t_p are compared to the corresponding values of the pulsed safe area on the derated curves.

2. With Time Markers: If time-marked load lines are available, either through the use of dual-trace waveforms of collector-to-emitter voltage and collector current as a function of time or Z-axis modulation of oscilloscope traces, an alternative approach may be used. The marked load line is sketched on the derated curves. If the transistor is being operated in the safe area, the trace time of the portion of the load line that extends outside a given pulsed safe area should not be greater than the specified pulsed width for that safe area. For example, the load line should not spend more than 1 millisecond outside the 1-millisecond safe area.

Thermal Fatigue

Significant temperature variations occur in power transistors because of changes in ambient temperature and in the power dissipation during operation. These variations in temperature result in cyclic mechanical stresses at the interface of the semiconductor pellet and the metal header to which the pellet is bonded because of the difference in the thermal expansions of these parts. These stresses are a function of the difference in the coefficients of thermal expansion of the semiconductor and metallic materials, of the change in temperature at the interface, and of the dimensions of the interface.

Power transistors are subjected to thermal-cycling stresses in all practical applications. Table 2-2 lists

Table 2-2 — Thermal-Cycling Requirements, for Typical Applications of Power Transistors.

Application	Circuit	P_T (W)	ΔT_C (°C)	Minimum Equipment Life Required (years)	Typical Thermal-Cycling Rating Required (cycles)
Auto radio audio output	Class A	8	75	5	5,000
	Class AB	2	45	5	5,000
Power supply	Series regulator	50	65	5	5,000
	Switching regulator	15	65	5	5,000
Hi-Fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series regulator	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^8
Television	Vertical output	10	75	5	5,000
	Audio output	8	75	5	5,000
Sonar modulator	Linear amplifier	100	55	10	144×10^3

examples of the thermal cycling that a power transistor may be required to withstand in several typical applications. These data show that the thermal-cycling requirements may be very severe even in some of the more common types of applications. The cyclic stresses produced by the continuous thermal cycling may result in dislocation "pile-ups" at points of discontinuity such as may be produced by voids and impurities. Such dislocations cause localized hardening and cracks that may eventually lead to transistor failures. This type of failure may be considered simply as fatigue wearout that results from continuous flexing of materials during thermal cycling.

Effect of Assembly Methods and Package Material on Thermal-Cycling Capability—The thermal-cycling stresses set up at the interface of two dissimilar materials because of the difference in the coefficients of thermal expansion of the materials can be reduced by insertion of a material that has an intermediate expansion coefficient between them. Fig. 2-20(a) illustrates the use of a molybdenum slab as an expansion matcher in a silicon power transistor to reduce the cyclic thermal stresses between the silicon pellet and the copper header. Use of this technique can result in significant improvement in the thermal-cycling capability of power transistors.

Use of silicon-gold eutectic bonding to attach the semiconductor pellet to the header results in a pellet-to-header joint that can withstand a very large number of number of thermal cycles. When this type of hard-solder bonding is used, however, the stress generated because of a thermal mismatch is transmitted to the pellet, which in most power transistors is made of silicon. Because silicon is relatively weak in tensile strength and is highly "notched sensitive," the cyclic thermal stresses may result in the propagation of cracks in the silicon pellet unless either the pellet is very small or an expansion matcher is used.

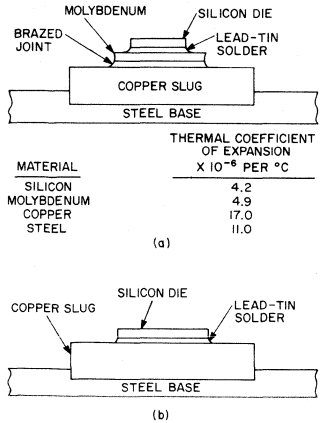


Fig. 2-20– Cross section of a transistor that uses a molybdenum expansion matcher between pellet and header; (b) cross section of a transistor in which pellet is soldered directly to copper.

In most silicon power transistors, lead solder is used to bond the pellet to the header. The cyclic thermal stresses produced at the mounting interface are then absorbed by non-elastic deformation of the soft solder material, and very little stress is transmitted to the pellet. The continuous flexing of the solder, however, may eventually lead to fatigue failure in this material. Any impurities in the solder results in dislocation pile-ups that accelerate the failure. RCA has developed a process that significantly reduces the impurities introduced into the lead solder. Use of this proprietary "controlled solder process" (CSP) makes it possible to avoid microcracks that propagate to cause fatigue failures in power transistors and, therefore, greatly increases the thermal-cycling capability of these devices.

Thermal-Cycling Rating Chart—An equipment manufacturer should make certain that power-transistor circuits are designed so that cyclic thermal stresses are mild enough to assure that no transistor fatigue failures occur during the required operating life of this equipment. Experimental results indicate that the thermal-cycling capability of a power transistor can be predicted by use of the following mechanical-activation energy equation:

$$N = AeY_{\phi}/\Delta T$$

where N is the number of cycles to failure, A is a system constant, γ_{ϕ} is a constant proportional to the mechanical-activation energy required to produce a failure, and ΔT is proportional to the energy supplied as a result of the change in temperature at the mounting interface.

The above equation, together with empirical data, forms the basis for a new thermal-cycling rating system developed by RCA. This rating system, which is the first of this type in the industry, shows the relationship between total transistor power dissipation, the change in case temperature, and the number of thermal cycles that the transistor is rated to withstand.

Fig. 2-21 shows a typical thermal-cycling rating chart. This chart is provided in the form of a log-log presentation in which total transistor power dissipation is denoted by the ordinate and the thermal-cycling capability (number of cycles to failure) is indicated by the abscissa. Rating curves are shown for various magnitudes of change in case temperature. Use of this chart makes it possible for a circuit designer to avoid transistor thermal-fatigue failures during the operating life of this equipment. In general, power dissipation is a fixed system requirement. The designer also knows the number of thermal cycles that a power transistor will be subjected to during the minimum required life of the equipment. For these conditions, the chart indicates the maximum allowable change in case temperature. (If the rating point does not lie exactly on one of the rating curves, the allowable change in case temperature can be approx-

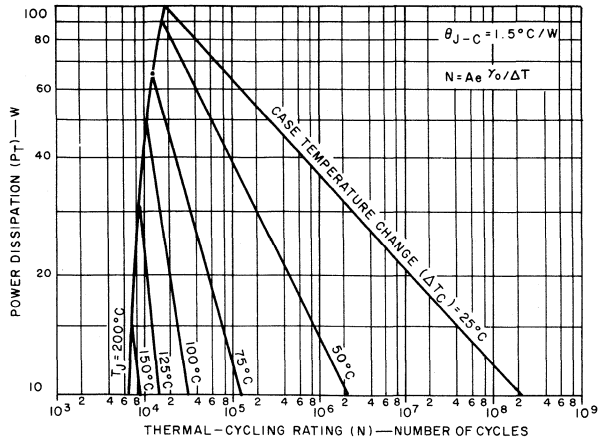


Fig. 2-21– Typical series-regulator power supply.

imated by linear interpolation.) The designer can then determine the minimum size of heat sink required to restrict the change in case temperature within this maximum value.

Thermal-cycling ratings are included in the technical data for all RCA silicon power transistor announced since January 1, 1971. Similar ratings are being added for earlier power transistors as sufficient date are accumulated.

RCA experience in determining thermal-cycling rating has shown that package material is also a very important consideration in relation to thermal fatigue. Comparison data on the RCA steel packages and aluminum packages are given in the RCA Reliability Report, "Evaluation of Aluminum TO-3 Packages Under Thermal-Cycling Conditions" (AN-6071), shown later in the section *Application Notes on Power Transistors*.

These data show that the thermal-cycling capability of RCA's steel package with its glass-to-stem seal, welded cap, and controlled solder process is far superior (more than an order of magnitude better) to that of a similar type aluminum package and hard-solder mounting system.

Thermal-Fatigue Testing—The RCA thermal-cycling ratings allow a circuit designer to use power transistors with assurance that fatigue failures of these devices will not occur during the minimum required life of his equipment. These ratings provide valid indications of the thermal-cycling capability of power transistors for all types of operating conditions. On the basis of these ratings, limiting conditions can be established during circuit design so that the possibility of transistor thermal-fatigue failures are avoided.

Obviously, all individual power transistors cannot be tested to determine their thermal-cycling capability because such tests are expensive, time consuming, and destructive. The validity of the RCA thermal-cycling ratings results from the application of stringent process controls at each step in the manufacture of power transistors and from the testing of a statistically significant number of samples. Thermal-cycling ratings for power transistors provide the same type of assurance that a device will not fail when operated within ratings as that provided by the more familiar voltage, current, and second-breakdown ratings.

During thermal-fatigue testing of power transistors, the operating power for the device is usually equivalent to that expected to be applied during normal operation. The transistor is operated until the rise in case temperature is equal to the maximum value anticipated in the intended application. The case temperature is then reduced to the initial value by use of forced-air or water cooling. The cycle is repeated until failure occurs, as indicated by a significant increase in the transistor thermal resistance. The transistor heat sink and the timing of the temperature-cycling are selected to simulate as closely as possible the actual conditions that the transistor will be subjected to in the actual application. Table 2-3 shows the results of thermal-fatigue tests on several RCA transistors.

Effect of Radiation on RCA Power Transistors

There has been an increasing requirement for modern military systems to be "radiation hard", i.e., resistant to the effects of nuclear radiation. The electronic equipment in these systems must be carefully designed to achieve the required hardness. Solid-state devices have been the subject of particularly close attention.

Nuclear radiation has two major effects on power transistors. First, photocurrents generated by high-intensity irradiation can cause transistor saturation and possible circuit malfunction during the exposure. Second, prolonged exposure to bombardment by heavy particles such as neutrons can cause permanent changes in the transistor characteristics. These changes, which are caused by displacement damage to the semiconductor crystal, are primarily manifested as a decrease in transistor gain and an increase in saturation voltages. Table 2-4 summarizes the basic considerations relative to both displacement damage and photocurrents.

Power transistors must be optimally designed to minimize these radiation effects and maintain the required power-handling capability. The key design parameters are a thin low resistivity, low volume base, and a collector as thin and as low in resistivity as possible consistent with voltage breakdown requirements. Trans-

Table 2-3 — Thermal-Fatigue Performance of some Typical RCA Power Transistors

Type	Pellet Size Mils x Mils		Mounting Material	Material to which Die is Attached	CSP	Change in Case Temp. °C	Power Dissipation Watts	No. of Cycles to 10% Failure
2N3773*	250	250	Lead	Copper	No	42	85	1,000
2N3773	250	250	Lead	Molybdeum	No	42	85	9,600
2N3772	250	250	Lead	Copper	Yes	90	16	34,500**
2N3055	180	180	Lead	Copper	No	65	50	3,500
2N3055	180	180	Lead	Copper	Yes	90	6.7	40,000***
2N6032	230	230	Silicon Gold	Molybdeum	No	53	105	12,793***
2N5298	130	130	Lead	Copper	No	50	18	10,000
2N5240	130	130	Lead	Copper	Yes	42	51	8,500***
2N5039	145	183	Lead	Copper	Yes	73	59	10,000***

* Early design. ** Test still operating. *** Test terminated—less than 10% failure.

Table 2-4 — Effect of Nuclear Radiation on Power Transistors

	Displacement Damage	Photocurrents
Cause	Heavy particles, such as neutrons, bombarding the transistor and creating defects in the semiconductor material. Decreases lifetime in the base and increases collector resistivity.	High-intensity, high-energy radiation such as gamma, X-rays, electrons, neutrons, etc. generating electron-hole pairs.
Result	Semipermanent gain degradation and Increase in $V_{CE(sat)}$, leakage, and V_{CE}. These changes are referred to as semipermanent because annealing at several hundred degrees centigrade for a few hours recovers most of the degradation.	Relatively large currents lasting as long as the transistor is exposed to radiation.
Radiation Parameter	Particles per square centimeter, called fluence, designated by the symbol Φ. The commonly used unit for this parameter is neutrons per square centimeter (n/cm^2).	Radiation is usually defined in terms of rad(Si), where one rad(Si), identified by the symbol γ (gamma) is the amount of radiation required to deposit 100 ergs in one gram of silicon. $\dot{\gamma}$ (gamma dot) is defined as the dose rate in rad(Si) per second.
Relationship at Different Radiation Levels	Formula commonly used to extrapolate gain degradation results from one fluence level to another. $1/h_{FE2} = (1/h_{FE1}) + K^1\Phi$ where h_{FE2} = post-radiation gain, h_{FE1} = pre-radiation gain, K^1 = damage constant in cm^2/n, Φ = fluence in n/cm^2	
General		Collector-base photocurrents (I_{pp}) and emitter-base photocurrents (I_{ee}) are variously plotted as amperes versus $\dot{\gamma}$, or coulombs versus γ (coul/rad). At low dose rates, photocurrents are generally quite well-behaved and reasonably predictable from the formula $I=G\gamma$ where G is a function of the effective volume of the junction. (At relatively high dose rates, some transistors exhibit a departure from the assumed linear dose-rate dependence.)

istors that meet these design criteria are typified by high f_T, fast switching speeds, and moderate breakdown voltages.

RCA has developed power transistors which offer an optimized performance trade-off of radiation hardness, voltage, safe area, and power capability. For example, both photocurrent and voltage breakdown increase with increased collector resistivity because carrier lifetime is a function of resistivity. Collector resistivity, therefore, is fine-tuned to provide the maximum voltage breakdown possible with acceptable photocurrent performance. Post-radiation beta degradation is a function of base width, as is the frequency cutoff. Both of these characteristics are enhanced with decreasing base width. However, the safe-area capability is also a function of base width. Consequently, this parameter is fine-tuned to achieve optimum electrical performance and radiation hardness. Other techniques can be employed to enhance safe-area capability, such as the introduction of various amounts of ballasting.

Processing and Screening

RCA offers a number of power transistors that have been qualified as JAN and/or JANTX devices in accordance with MIL-S-19500. These devices, which include hometaxial-base types, high-voltage types, and high-speed types, together with the detailed electrical (slash-sheet) specification number for them, are listed in Table 2-5.

Table 2-5 — JAN and JANTX RCA Power Transistors

Basic Device Type Nos.	Detailed Electrical Specification
Hometaxial-Base Types	
2N1479, 2N1480, 2N1481, 2N1482	MIL-S-19500/207
2N1483, 2N1484, 2N1485, 2N1486	MIL-S-19500/180
2N1487, 2N1488, 2N1489, 2N1490	MIL-S-19500/208
2N2015, 2N2016	MIL-S-19500/248
2N3055	MIL-S-19500/407
2N3441	MIL-S-19500/369
2N3442	MIL-S-19500/370
2N3771, 2N3772	MIL-S-19500/413
High-Voltage Types	
2N3584, 2N3585	MIL-S-19500/384
2N6211, 2N6212, 2N6213	MIL-S-19500/461*
2N3439, 2N3440	MIL-S-19500/368
2N5415, 2N5416	MIL-S-19500/485*
2N5838, 2N5839, 2N5840	MIL-S-19500/487
High-Speed Types	
2N5038, 2N5039	MIL-S-19500/439
2N5671, 2N5672	MIL-S-19500/488*

* In process of Qualification by RCA

MIL-S-19500 detailed electrical specifications for JAN and JANTX devices can be obtained from the *Naval Publications and Forms Center,* 5801 Tabor Avenue, Philadelphia, Pa.

Fig. 2-22 shows the processing requirements specified by MIL-S-19500 for JAN and JANTX power transistors.

In addition to JAN and JANTX types, many other RCA power transistors that are subjected to high-reliability preconditioning and screening in accordance with the Group A, B, and C Sampling Tests as specified in MIL-STD-750 or special customer requirements can be obtained on a custom basis. These power transistors can be supplied to four basic reliability levels. The preconditioning and screening for Level 1 is the same as that for JANTXV devices (i.e., JANTX preconditioning plus pre-cap visual inspection) and, in addition, includes X-ray inspection. Level 2 corresponds directly to the JANTXV level. Level 3 devices are equivalent to JANTX devices. For RCA Level 4 devices, the preconditioning consists of burn-in only.

Fig. 2-23 shows the basic processing steps required for RCA high-reliability power transistors for each reliability level, and Table 2-6 lists the screening tests to which these devices are subjected. Tables 2-7, 2-8, and 2-9 list the Groups A, B, and C Sampling Tests and the test methods specified by MIL-STD-750. The lot-sampling plans used for RCA high-reliability power transistors, as defined by MIL-S-19500 and MIL-STD-105D, are shown in Tables 2-10, 2-11, and 2-12.

The electrical ratings and characteristics and special features of JAN and JANTX types and of other RCA power transistors for which high-reliability versions can be obtained are shown in the section *Technical Data on RCA High-Reliability Power Transistors*.

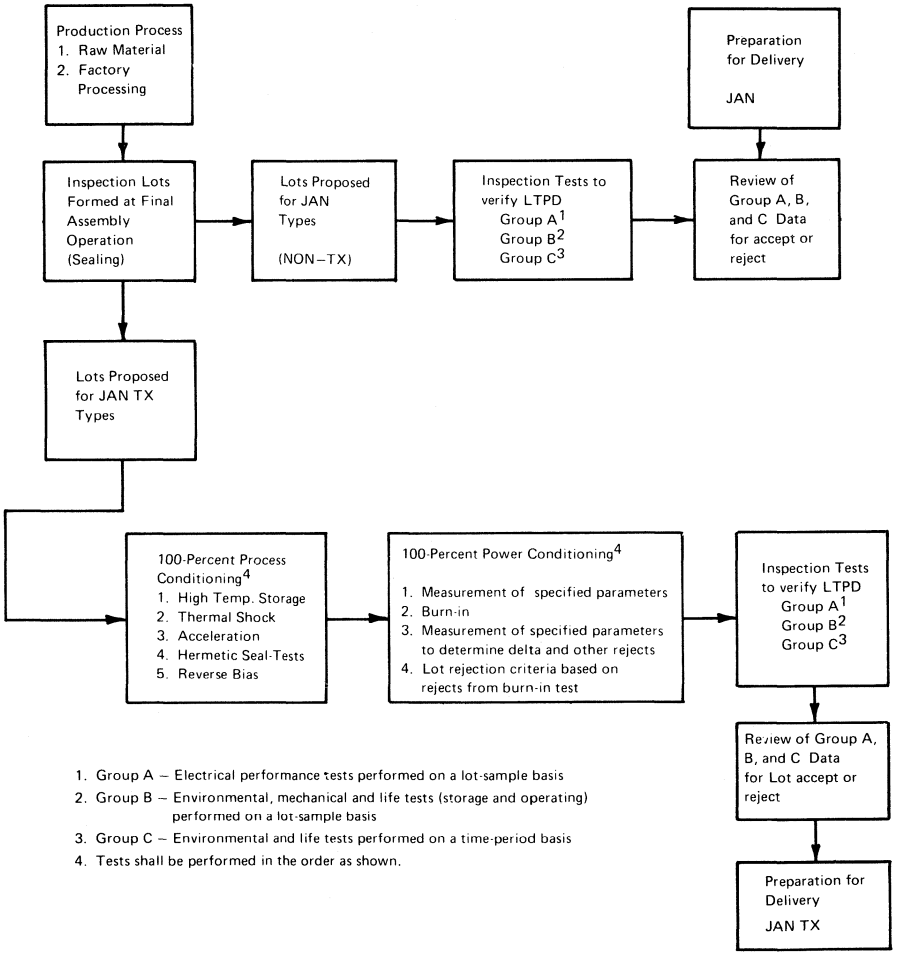


Fig. 2-22– Order of procedure diagram for JAN and JANTX power transistors.

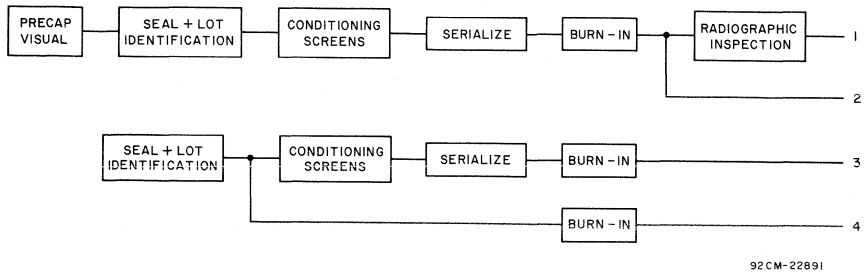


Fig. 2-23– Process-flow chart for four reliability levels of RCA high-reliability power transistors.

Table 2-6— Screening Tests for RCA High-Reliability Power Transistors

Test	Conditions	MIL-STD-750 Method	MIL-STD-750 Conditions	Screening Levels 1	2	3	4
1. Precap Visual		2072		X	X		
2. Seal and Lot Identification				X	X	X	X
3. High Temp Storage	24 hrs at 200°C			X	X	X	
4. Temperature Cycling	10 cycles	1051	C	X	X	X	
5. Acceleration	Y_1 direction	2006		X	X	X	
6. Fine Leak		1071	G or H	X	X	X	
7. Gross Leak		1071	A,C,D or F	X	X	X	
8. Reverse Bias	24 hrs at 150°C	1039	A	X	X	X	
9. Serialize				X	X	X	
10. Pre Burn-in Electrical				X	X	X	
11. Burn-in	168 hrs at 25°C	1039	B	X	X	X	X
12. Post Burn-in Electrical				X	X	X	
13. Final Electrical				X	X	X	X
14. Radiographic Inspection		2076		X			
15. External Visual		2071		X	X	X	

Specific test conditions and limits determined by each type of transistor.

Table 2-7 — Group A Inspections

Subgroup	Test	MIL-STD-750 Method
1	Visual & Mech Examination	2071
2	B_{VCEO}, B_{VCER}, or B_{VCEX}	3011
	I_{CEO}, I_{CER}, or I_{CEX}	3041
	I_{EBO}	3061
3	h_{FE}	3076
	$V_{CE(sat)}$	3071
	V_{BE}	3066
4	h_{FE}	3306
	C_{obo}	3236
	t_{on}	3251
	t_{off}	3251
5	150°C I_{CEX}	3041
	−65°C h_{FE}	3076

Table 2-8 — Group B Inspections

Subgroup	Test	MIL-STD-750 Method
1	Physical dimensions	2066
2	Solderability	2026
	Temperature Cycling	1051
	Moisture Resistance	1021
3	Shock	2016
	Vibration, Variable Frequency	2056
	Constant Accleration	2066
4	Safe Operating Area	3051
5	High Temperature Life	1031
6	Steady-State Operation Life	1026

Table 2-9 — Group C Inspections

Subgroup	Test	MIL-STD-750 Method
1	Barometric Pressure	1001
2	Salt Atmosphere	1041

TABLE 2-10 — LTPD sampling plans 1/ 2/ 3/

Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample).

Max. Percent Defective (LTPD) or λ	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3
Acceptance Number (c) (r = c + 1)	Minimum Sample Sizes (For device-hours required for life test, multiply by 1000)											
0	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)
1	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)
2	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)
3	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)
4	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)
5	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)
6	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)
7	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)
8	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)
9	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)
10	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)

1/ Sample sizes are based upon the Poisson exponential binomial limit.
2/ The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.
3/ This sampling plan is derived from Table C-1 in Appendix C of MIL-S-19500.

TABLE 2-11 — Sample Size Code Letters*

Lot or batch size	General inspection levels		
	I	II	III
2 to 8	A	A	B
9 to 15	A	B	C
16 to 25	B	C	D
26 to 50	C	D	E
51 to 90	C	E	F
91 to 150	D	F	G
151 to 280	E	G	H
281 to 500	F	H	J
501 to 1200	G	J	K
1201 to 3200	H	K	L
3201 to 10000	J	L	M
10001 to 35000	K	M	N
35001 to 150000	L	N	P
150001 to 500000	M	P	Q
500001 and over	N	Q	R

* Derived from Table I of MIL-STD-105D

TABLE 2-12 — Single Sampling Plans for Normal Inspection*

Sample size code letter	Sample size	Acceptable Quality Levels (normal inspection)																							
		0.010		0.015		0.025		0.040		0.065		0.10		0.15		0.25		0.40		0.65		1.0		1.5		2.5		4.0		6.5		10		15		25	
		Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re
A	2	⇩		⇩		⇩		⇩		⇩		⇩		⇩		⇩		⇩		⇩		⇩		⇩		⇩		⇩		0	1	⇩		⇩		1	2
B	3																													0	1	⇩		⇩		1	2	2	3
C	5																							⇩		0	1	⇩		⇩		1	2	2	3	3	4
D	8																							0	1	⇩		⇩		1	2	2	3	3	4	5	6
E	13																					0	1	⇧	⇩	⇩		1	2	2	3	3	4	5	6	7	8
F	20																			0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11
G	32																	0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15
H	50															0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22
J	80													0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	⇩	
K	125											0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	⇧	⇩		
L	200									0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	⇧	⇩				
M	315							0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	⇧	⇩						
N	500					0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	⇧	⇩								
P	800			0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	⇧	⇩										
Q	1250	0	1	⇧	⇩	⇧	⇩	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	⇧	⇩												
R	2000	⇧		⇧		1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	⇧	⇩														

⇩ = Use first sampling plan below arrow. If sample size equals, or exceeds, lot or batch size, do 100 percent inspection

⇧ = Use first sampling plan above arrow.

Ac = Acceptance number.

Re = Rejection number.

* Derived from Table II-A of MIL-STD-105D

JAN2N1482

Hometaxial-Base Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/207
Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-5
Maximum Ratings: V_{CEO} = 55 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 5 mA, V_{CE} = 28 V	600	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 200 mA, V_{CE} = 4 V	35	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 200 mA, I_B = 10 mA	–	0.75	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 200 mA	–	25	μs
Turn-off	t_{OFF}	I_C = 200 mA	–	25	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 135.

JAN2N1486
JANTX2N1486

Hometaxial-Base Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/180
Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-8
Maximum Ratings: V_{CEO} = 55 V, P_T = 1.75 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 5 mA, V_{CE} = 28 V	600	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 750 mA, V_{CE} = 4 V	35	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 750 mA, I_B = 40 mA	–	0.75	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 750 mA	–	25	μs
Turn-off	t_{OFF}	I_C = 750 mA	–	25	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 137.

JAN2N1490

Hometaxial-Base Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/208
Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 55V, P_T = 75 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 100 mA, V_{CE} = 12 V	500	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1.5 A, V_{CE} = 4 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1.5 A, I_B = 100 mA	–	1	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 1.5 A	–	25	μs
Turn-off	t_{OFF}	I_C = 1.5 A	–	25	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 139.

JAN2N2016

Hometaxial-Base Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/248
Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-36
Maximum Ratings: V_{CEO} = 65 V, P_T = 150 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 5 A, V_{CE} = 4 V	800	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 5 A, V_{CE} = 4 V	15	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 5 A, I_B = 0.5 A	–	1.25	V

For characteristics curves and test conditions, refer to published data for basic type in File No. 12.

JAN2N3055
JANTX2N3055

Hometaxial-Base Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/407
Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 70 V, P_T = 117 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 4 V	800	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 4 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4 A, I_B = 0.4 A	–	0.75	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 70 V, t = 1 s	1.67	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 4 A	–	6	μs
Turn-off	t_{OFF}	I_C = 4 A	–	12	μs
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	3×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 524.

JAN2N3439
JANTX2N3439

High-Voltage Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/368
Structure: Double-diffused epitaxial
Applications: High-voltage amplifiers, inverters, regulators
System Usage: Military
Package: JEDEC TO-39 (2N3439S) or JEDEC TO-5 (2N3439L)
Maximum Ratings: V_{CEO} = 350 V, P_T = 0.8 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 20 mA, V_{CE} = 10 V	40	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 50 mA, I_B = 4 mA	–	0.5	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 200 V, t = 1 s	50	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 20 mA	–	1	μs
Turn-off	t_{OFF}	I_C = 20 mA	–	10	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 64.

JAN2N3441
JANTX2N3441

High-Voltage Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/369
Structure: Hometaxial-base
Applications: High-voltage power switching, amplifiers
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = 140 V, P_T = 25 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 4 V	400	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 0.5 A, V_{CE} = 4 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 0.5 A, I_B = 0.05A	–	1	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 30 V, t = 1 s	833	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 0.5 A	–	8	μs
Turn-off	t_{OFF}	I_C = 0.5 A	–	15	μs
Thermal-Cycling Rating		P_T = 4 W, ΔT_C = 50°C	5×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 529.

JAN2N3442

High-Voltage Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/370
Structure: Hometaxial-base
Applications: High-voltage power switching, amplifiers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 140 V, P_T = 117 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 3 A, V_{CE} = 4 V	100	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 3 A, V_{CE} = 4 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 3 A, I_B = 0.3 A	–	1	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	$V_{CE} \geqslant 8$ V, t = 1 s	1.5	–	A
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	3×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 528.

JAN2N3585
JANTX2N3585

High-Voltage Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/384
Structure: Double-diffused epitaxial collector
Applications: High-voltage amplifiers, inverters, regulators
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = 300 V, P_T = 35 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 10 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 1 A, I_B = 0.125 A	–	0.75	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 2 A, L = 100 μH, R_{BE} = 20Ω	200	–	μJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 100 V, t = 1 s	350	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 1 A	–	3	μs
Turn-off	t_{OFF}	I_C = 1 A	–	7	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 138.

JAN2N3772
JANTX2N3772

High-Current Silicon N-P-N Power Transistor

JAN Electrical Spacification: MIL-S-19500/413
Structure: Hometaxial-base
Applications: Power-switching, amplifiers, inverters
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 60 V, P_T = 150 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 4 V	600	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 A, V_{CE} = 4 V	15	–	
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10 A, I_B = 1 A	–	1.2	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 5 A, L = 40 mH, R_{BE} = 100Ω	500	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 60 V, t = 1 s	2.5	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 10 A	–	8	μs
Turn-off	t_{OFF}	I_C = 10 A	–	10	μs
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	4×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 525.

JAN2N5038
JANTX2N5038

High-Speed Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/439
Structure: Multiple-emitter sites, double-diffused epitaxial collector
Applications: Switching regulators, inverters, amplifiers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 90 V, P_T = 140 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 2 A, V_{CE} = 10 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 12 A, V_{CE} = 5 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 12 A, I_B = 1.2 A	–	1	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 12 A, L = 180 μH, R_{BE} = 20Ω	13	–	mJ
Second Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 45 V, t = 1 s	0.9	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 12 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = 12 A	–	2	μs
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	4×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 367.

JAN2N5416
JANTX2N5416

High-Voltage Silicon P-N-P Power Transistor

JAN Electrical Specification: MIL-S-19500/485
Structure: Double-diffused epitaxial
Applications: High-voltage amplifiers, inverters, regulators
System Usage: Military
Package: JEDEC TO-5
Maximum Ratings: V_{CEO} = −300 V, P_T = 0.75 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = −10 mA, V_{CE} = −10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −50 mA, V_{CE} = −10 V	30	–	
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = −50 mA, I_B = −5 mA	–	−2	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = −100V, t = 1 s	−100	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = −50 mA	–	1	μs
Turn-off	t_{OFF}	I_C = −50 mA	–	10	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 336.

JAN2N5672
JANTX2N5672

High-Speed Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/488
Structure: Double-diffused epitaxial collector
Applications: Switching regulators, amplifiers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 120 V, P_T = 140 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 2 A, V_{CE} = 10 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 15 A, V_{CE} = 2 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 15 A, I_B = 1.2 A	–	0.75	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 15 A, L = 180 μH R_{BE} = 20Ω	20	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 45 V, t = 1 s	0.9	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 15 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = 15 A	–	2	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 383.

JAN2N5840
JANTX2N5840

High-Voltage Silicon N-P-N Power Transistor

JAN Electrical Specification: MIL-S-19500/487
Structure: Double-diffused, epitaxial-base
Applications: High-voltage switching regulators, inverters
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 350 V, P_T = 100 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 2 A, V_{CE} = 3 V	10	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 2 A, I_B = 0.2 A	–	1.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 3 A, L = 100 μH R_{BE} = 50Ω	0.45	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 40 V, t = 1 s	2.5	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 2 A	–	1.75	μs
Turn-off	t_{OFF}	I_C = 2 A	–	4.5	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 410.

JAN2N6213
JANTX2N6213

High-Voltage Silicon P-N-P Power Transistor

JAN Electrical Specification: MIL-S-19500/461
Structure: Double-diffused epitaxial collector
Applications: High-voltage amplifiers, inverters, regulators
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = −350 V, P_T = 35 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -0.2 A, V_{CE} = -10 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -1 A, V_{CE} = -4 V	10	–	
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = -1 A, I_B = -0.125 A	–	-2	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = -40 V, t = 1 s	-0.875	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = -1 A	–	0.6	μs
Turn-off	t_{OFF}	I_C = -1 A	–	3.1	μs
Thermal-Cycling Rating		P_T = 2 W, ΔT_C = 50°C	7×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 507.

2N2102

High-Speed, Medium-Power Silicon N-P-N Power Transistor

Structure: Planar, Double-diffused epitaxial collector
Applications: Small-signal and medium-power general usage
System Usage: NASA SATURN
Package: JEDEC TO-39 (2N2102S) or JEDEC TO-5 (2N2102L)
Maximum Ratings: V_{CEO} = 65 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 10 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 150 mA, V_{CE} = 10 V	40	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	1.5	V

For characteristics curves and test conditions, refer to published data for basic type in File No. 106.

2N3054

Hometaxial-Base Silicon N-P-N Power Transistor

Structure: Hometaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = 55 V, P_T = 25 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 4 V	800	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 0.5 A, V_{CE} = 4 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 0.5 A, I_B = 0.05 A	–	1	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 55 V, t = 1 s	0.455	–	A
Thermal-Cycling Rating		P_T = 4 W, ΔT_C = 50°C	5×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 527.

2N3263 — High-Power, High-Speed, High-Current Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: High-speed switching, amplifiers, inverters
System Usage: Minuteman, SRAM
Package: Radial, hermetic
Maximum Ratings: V_{CEO} = 90 V, P_T = 84 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 3 A, V_{CE} = 10 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 15 A, V_{CE} = 3 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 15 A, I_B = 1.2 A	–	0.75	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 10 A, L = 40 μH R_{BE} = 20Ω	2	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 75 V, t = 250 μs	350	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 15 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = 15 A	–	2	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 54.

2N3265 — High-Power, High-Speed, High-Current Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: High-speed switching, amplifiers, inverters
System Usage: Minuteman, SRAM
Package: JEDEC TO-63
Maximum Ratings: V_{CEO} = 90 V, P_T = 125 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 3 A, V_{CE} = 10 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 15 A, V_{CE} = 3 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 15 A, I_B = 1.2 A	–	0.75	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 10 A, L = 40 μH R_{BE} = 20Ω	2	–	mJ
Second Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 75 V, t =250 μs	350	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 15 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = 15 A	–	2	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 54.

2N3773

High-Voltage Silicon N-P-N Power Transistor

Structure: Hometaxial-base
Applications: High-voltage inverters, amplifiers, hammer drivers
System Usage: VIKING
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 140 V, P_T = 150 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 4 V	200	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 8 A, V_{CE} = 4 V	15	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 8 A, I_B = 0.8 A	–	1.4	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 2.5 A, L = 40 mH R_{BE} = 100Ω	0.125	–	J
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 100 V, t = 1 s	1.5	–	A
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	4×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 526.

2N3879

High-Current, High-Speed Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: High-current, high-speed switching
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = 75 V, P_T = 35 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 10 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 5 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4 A, I_B = 0.4 A	–	1.2	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 4 A, L = 125 μH R_{BE} = 50Ω	1	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 40 V, t = 1 s	500	–	mA
Saturated Switching Time: Turn-on	t_{ON}	I_C = 4 A	–	440	ns
Turn-off	t_{OFF}	I_C = 4 A	–	1200	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 299.

2N4036

Medium-Power Silicon P-N-P Power Transistor

Structure: Planar, double-diffused epitaxial collector
Applications: Small-signal, medium-power amplifiers
System Usage: Military
Package: JEDEC TO-39 (2N4036S) or JEDEC TO-5 (2N4036L)
Maximum Ratings: V_{CEO} = -65 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -50 mA, V_{CE} = -10 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -150 mA, V_{CE} = -10 V	40	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = -150 mA, I_B = -15 mA	–	-0.65	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = -150 mA	–	110	ns
Turn-off	t_{OFF}	I_C = -150 mA	–	700	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 216.

2N5240

High-Voltage, High-Power Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: Series regulators, power amplifiers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 300 V, P_T = 100 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 2 A, V_{CE} = 10 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 2 A, I_B = 0.25 A	–	2.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 4 A, L = 0.2 mH, R_{BE} = 50Ω	1.6	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 150 V, t = 1 s	0.67	–	A

For characteristics curves and test conditions, refer to published data for basic type in File No. 321.

2N5262

High-Speed Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial
Applications: Core drivers, high-speed amplifiers
System Usage: AEGIS
Package: Low-profile TO-39
Maximum Ratings: V_{CEO} = 50 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 10 V	250	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 1 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1 A, I_B = 0.1 A	–	0.8	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 1 A	–	30	ns
Turn-off	t_{OFF}	I_C = 1 A	–	60	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 313.

2N5320

High-Speed Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: Small-signal and medium-power amplifiers
System Usage: Military
Package: JEDEC TO-39 (2N5320S) or JEDEC TO-5 (2N5320L)
Maximum Ratings: V_{CEO} = 75 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 500 mA, V_{CE} = 4 V	30	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 500 mA, I_B = 50 mA	–	0.5	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 500 mA	–	80	ns
Turn-off	t_{OFF}	I_C = 500 mA	–	800	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 325.

2N5322

High-Speed Silicon P-N-P Power Transistor

Structure: Double-diffused epitaxial collector
Applications: Small-signal, medium-power amplifiers
System Usage: Military
Package: JEDEC TO-39 (2N5322S) or JEDEC TO-5 (2N5322L)
Maximum Ratings: V_{CEO} = -75 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -50 mA, V_{CE} = -4 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -500 mA, V_{CE} = -4 V	30	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = -500 mA, I_B = -50 mA	–	-0.7	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = -500 mA	–	100	ns
Turn-off	t_{OFF}	I_C = -500 mA	–	1000	ns

For characteristics curves and test conditions, refer to published data for basic type in File No. 325.

2N5578

High-Current, High-Power Silicon N-P-N Power Transistor

Structure: Multiple-emitter sites, hometaxial-base
Applications: High-current, high-power amplifiers and switching
System Usage: TOW, Sonobuoy
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 70 V, P_T = 300 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 10 A, V_{CE} = 4 V	400	–	kHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 40 A, V_{CE} = 4 V	10	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 40 A, I_B = 4 A	–	1.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 7A, L = 33 mH R_{BE} = 10Ω	0.8	–	J
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 25 V, t = 1 s	12	–	A

For characteristics curves and test conditions, refer to published data for basic type in File No. 359.

2N5781

High-Speed Silicon P-N-P Power Transistor

Structure: Epitaxial-base
Applications: Medium-power switching and amplifiers
System Usage: Military
Package: JEDEC TO-5
Maximum Ratings: V_{CEO} = -65 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -0.1 A, V_{CE} = -2 V	8	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -1 A, V_{CE} = -2 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = - 1 A, I_B = -0.1 A	–	-0.5	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = -1 A	–	0.5	μs
Turn-off	t_{OFF}	I_C = -1 A	–	2.5	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 413.

2N5784

Hometaxial-Base Silicon N-P-N Power Transistor

Structure: Hometaxial-base
Applications: Medium-power switching, amplifiers
System Usage: Military
Package: JEDEC TO-5
Maximum Ratings: V_{CEO} = 65 V, P_T = 1 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.1 A, V_{CE} = 2 V	1	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 2 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1 A, I_B = 0.1 A	–	0.5	V
Saturated Switching Time:					
Turn-on	t_{ON}	I_C = 1A	–	5	μs
Turn-off	t_{OFF}	I_C = 1A	–	15	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 413.

2N5954

High-Speed, Medium-Power Silicon P-N-P Power Transistor

Structure: Epitaxial-base
Applications: Power-switching, amplifiers
System Usage: Military
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = -80 V, P_T = 40 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -1 A, V_{CE} = -4 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -2 A, V_{CE} = -4 V	20		
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = -2 A, I_B = -0.2 A	–	-1	V

For characteristics curves and test conditions refer to published data for basic type in File No. 675.

2N6033

High-Current, High-Speed, High-Power Silicon N-P-N Power Transistor

Structure: Double-diffused epitaxial collector
Applications: High-current, fast switching
System Usage: SAFEGUARD
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 120 V, P_T = 140 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 2 A, V_{CE} = 10 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 40 A, V_{CE} = 2 V	10	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 40 A, I_B = 4 A	–	1	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 20 A, L = 310 μH R_{BE} = 5Ω	62	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 40 V, t = 1 s	0.9	–	A
Saturated Switching Time: Turn-on	t_{ON}	I_C = 40 A	–	1	μs
Turn-off	t_{OFF}	I_C = 40 A	–	2	μs

For characteristics curves and test conditions, refer to published data for basic type in File No. 462.

2N6056

Darlington
Silicon N-P-N Power Transistor

Structure: Monolithic, epitaxial-base
Applications: Power-switching, amplifiers, hammer drivers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 80 V, P_T = 100 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 3 A, V_{CE} = 3 V	4	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 3 V	750	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4 A, I_B = 16 mA	–	2	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 5 A, L = 12 mH R_{BE} = 100Ω	150	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 40 V, t = 1 s	2	–	A
Thermal-Cycling Rating		P_T = 10 W, ΔT_C = 50°C	8×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 563.

2N6079

High-Voltage, High-Power
Silicon N-P-N Power Transistor

Structure: Multiple-emitter sites, double-diffused epitaxial
Applications: High-voltage inverters
System Usage: SAFEGUARD
Package: JEDEC TO-66
Maximum Ratings: V_{CEO} = 350 V, P_T = 45 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	1	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1.2 A, V_{CE} = 1 V	12	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1.2 A, I_B = 0.2 A	–	0.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 3 A, L = 100 μH R_{BE} = 50Ω	0.45	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 50 V, t = 1 s	0.9	–	A

For characteristics curves and test conditions, refer to published data for basic type in File No. 492.

2N6248

High-Speed, High-Power Silicon P-N-P Power Transistor

Structure: Epitaxial-base
Applications: Power-switching
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = -100 V, P_T = 125 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = -1 A, V_{CE} = -4 V	10	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = -5 A, V_{CE} = -4 V	20	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = -5 A, I_B = -0.5 A	–	-1.3	V
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = -42 V, t = 1 s	-1.25	–	A
Thermal-Cycling Rating		P_T = 10 W, ΔT_C = 50°	1.5×10^6	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 541.

2N6251

High-Voltage Silicon N-P-N Power Transistor

Structure: Multiple-epitaxial
Applications: High-voltage inverters
System Usage: MARK-48, P-3-C
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 350 V, P_T = 175 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 10 V	2.5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 A, V_{CE} = 3 V	6	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 10 A, I_B = 1.67 A	–	1.5	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 10 A, L = 50 μH, R_{BE} = 100Ω	2.5	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 30 V, t = 1 s	5.8	–	A
Thermal-Cycling Rating		P_T = 20 W, ΔT_C = 50°C	2×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 523.

2N6385

Darlington
Silicon N-P-N Power Transistor

Structure: Monolithic, epitaxial-base
Applications: Power-switching, amplifiers, hammer drivers
System Usage: Military
Package: JEDEC TO-3
Maximum Ratings: V_{CEO} = 80 V, P_T = 100 W

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Gain-Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 5 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 5 A, V_{CE} = 3 V	1000	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 5 A, I_B = 0.01 A	–	2	V
Second-Breakdown Energy: With base reverse-biased	$E_{S/b}$	I_C = 4.5 A, L = 12 mH R_{BE} = 100Ω	120	–	mJ
Second-Breakdown Collector Current: With base forward-biased	$I_{S/b}$	V_{CE} = 75 V, t = 1 s	0.22	–	A
Thermal-Cycling Rating		P_T = 10 W, ΔT_C = 50°C	8×10^5	–	Thermal Cycles

For characteristics curves and test conditions, refer to published data for basic type in File No. 609.

2N6479 2N6481 2N6480 2N6482

Radiation-Hardened Silicon N-P-N Power Transistor

Epitaxial-Planar Types for Aerospace and Military Applications

Rated for Operation in Radiation Environments with Neutron Fluence Levels to 1 x 10^{14} Neutrons/cm^2 and Gamma Exposure up to 1x10^8 Rad (Si)/s

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*
PRE-RADIATION

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS				UNITS
			VOLTAGE V dc			CURRENT A dc			2N6479 2N6481		2N6480 2N6482		
			V_{CB}	V_{CE}	V_{EB}	I_E	I_B	I_C	MIN.	MAX.	MIN.	MAX.	
	Collector Cutoff Current: With emitter open	I_{CBO}	100						–	1	–	1	mA
*	With base-emitter junction reverse-biased	I_{CEV}		100	0				–	1	–	1	mA
*	At T_C = 100°C			60	0				–	1	–	1	
*	Emitter Cutoff Current	I_{EBO}			6				–	2	–	2	mA
	Emitter-to-Base Voltage	V_{EBO}				0.002			6	–	6	–	V
	Collector-to-Emitter Sustaining Voltage:												
*	With base open	$V_{CEO(sus)}$						0.2[a]	60	–	80	–	V
	With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER(sus)}$						0.2[b]	80	–	100	–	
*	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$					1.2	12[a]	–	0.75	–	0.75	V
*	Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$					1.2	12[a]	–	1.5	–	1.5	V
*	DC Forward Current Transfer Ratio	h_{FE}		2				12[a]	20	300	20	300	
	Second Breakdown Collector Current: With base forward-biased, t = 1 s	$I_{S/b}$		12					7.3	–	7.3	–	A
*	Saturated Switching Time												
	Rise	t_r		V_{CC} =			1.2[c]	12	–	400	–	400	ns
	Storage	t_s		30			1.2[c]	12	–	800	–	800	
	Fall	t_f					1.2[c]	12	–	200	–	200	
*	Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (f = 10 MHz)	$\lvert h_{fe} \rvert$		5				1	10	–	10	–	
									2N6479 2N6480		2N6481 2N6482		
	Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$		10				5	–	2	–	1.5	°C/W

* In accordance with JEDEC registration data format JS-6 RDF-1.
a Pulsed; pulse duration ≤ 350 μs, duty factor ≤ 2%.
c $I_{B_1} = I_{B_2}$

POST-NEUTRON-RADIATION ELECTRICAL CHARACTERISTICS
AFTER EXPOSURE TO 5 x 10^{13} NEUTRONS/cm^2 (1 MeV equiv.), *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		VOLTAGE V dc			CURRENT A dc		For all Types		
		V_{CE}	V_{BE}	V_{EB}	I_C	I_B	MIN.	MAX.	
* Collector Cutoff Current: With base-emitter junction reverse-biased	I_{CEV}	100	0				–	1.2	mA
* Emitter Cutoff Current	I_{EBO}			5			–	2.2	mA
* Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO(sus)}$				0.2 0.2	0.05 0.05	80[b] 60[c]	– –	V
* Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				7[a]	1.4	–	1.5	V
* Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$				7[a]	1.4	–	1.5	V
* DC Forward Current Transfer Ratio	h_{FE}	5			7[a]		12	–	
Magnitude of Common Emitter, Small-Signal Short Circuit Forward Current Transfer Ratio (f = 10 MHz)	$\lvert h_{fe} \rvert$	5			1		10	–	
* Damage Constant	K▲						–	9×10^{-16}	

* In accordance with JEDEC registration data format JS-6 RDF-1.

[a] Pulsed; pulse duration $\leq$ 350 μs, duty factor $\leq$ 2%.

[b] For types 2N6480, 2N6482.

[c] For types 2N6479, 2N6481.

▲Damage constant $K = \dfrac{\frac{1}{h_{FE_2}} - \frac{1}{h_{FE_1}}}{\phi}$

Where h_{FE_1} = Beta prior to exposure

h_{FE_2} = Beta after exposure

ϕ = Neutron fluence (1 MeV equiv.)

Knowing K, h_{FE_2} may be calculated for other fluences using the relationship:

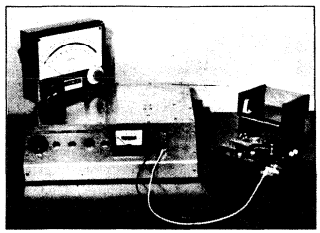
$$h_{FE_2} = \frac{1}{K\phi + \frac{1}{h_{FE_1}}}$$

TYPICAL CHARACTERISTIC DURING GAMMA EXPOSURE FOR DOSE RATES OF LESS THAN 1 x 10^8 RAD(Si)/sec

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS	UNITS
		VOLTAGE – V dc		For all Types	
		V_{CB}	V_{BE}	TYPICAL	
Collector-to-Base Charge Generation Constant	(C)	20	0	5×10^{-8}	$\frac{\text{Coulomb}}{\text{Rad}}$

The charge generated in the depletion region of a transistor is proportional to the volume of the depletion region, the total dose, and the energy of the gamma radiation.

The primary base-collector photo current $[I_{pp(base)}] = (C)\dot{\gamma}$, where $\dot{\gamma}$ is the gamma dose rate in Rad(Si)/s.



Testing for Forward-Bias Second Breakdown in Power Transistors

by D. A. Moe

The addition of "safe-operating-area" curves to power-switching transistor data for JEDEC registration and to manufacturers' data sheets has made necessary the development of non-destructive forward-bias second-breakdown test facilities. This Note describes the design of a test facility which determines the forward-bias second-breakdown safe operating locus for power transistors and shows detailed schematic diagrams of test circuits which can be used for devices with collector-current ratings up to 2.5 amperes and sustaining collector-to-emitter voltage $V_{CEO}(sus)$ ratings up to 300 volts, or with ratings to 5 amperes and 100 volts.

Causes of Second Breakdown

The safe operating area of a power transistor is bounded by a locus divided into four discrete segments, each representing a particular limiting condition. As shown in Fig. 1, the limiting factors are the maximum continuous-collector-current rating of the transistor, the maximum power-dissipation rating, second breakdown, and the sustaining voltage $V_{CEO}(sus)$ of the device.

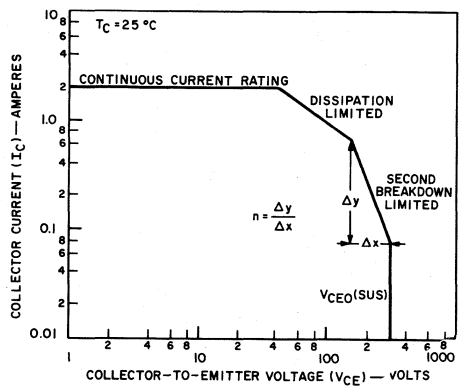


Fig. 1— A typical safe-operating-area curve.

Forward-bias second breakdown ($I_{S/b}$) in a power device is manifested by localized heating of the transistor pellet, as shown in Fig. 2. The average collector-junction temperature, T_J, of a power transistor may be calculated as follows:

$$T_J = T_C + P_{avg}\theta_{J\text{-}C}$$

where T_C is the case temperature in °C, P_{avg} is the average power dissipation in watts, and $\theta_{J\text{-}C}$ is the junction-to-case thermal resistance in °C per watt. However, the actual junction temperature can vary from point to point on the chip as a result of current-crowding that causes higher isolated dissipation. As a result, a localized thermal runaway may occur. In the forward-biased mode, such local heating is most likely to occur at the emitter edge because, under forward-bias conditions, lateral base current creates an electric field or voltage gradient in the base, as shown in Fig. 2. The direction of this voltage gradient causes greater forward bias at the emitter periphery than at the center. Therefore most injection occurs at the periphery, and the current density is greater. As the concentrated current flows across the depletion region, local power dissipation occurs and causes local heating. If the current density exceeds a

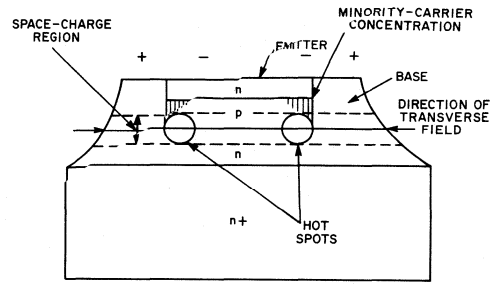


Fig. 2— Cross-section of a power transistor showing development of hot spots under forward bias.

critical level, the heat that is generated causes the local base-to-emitter voltage to decrease to a level that causes further injection, and collector-to-emitter current flow becomes regenerative. If this regenerative process is allowed to continue, device destruction follows. The current crowding may be aggravated by a non-homogeneous collector-base junction or by mounting-system imperfections such as solder voids.

A Second-Breakdown Test Facility

Fig. 3 shows a simplified schematic of a test set designed to determine the forward-bias second-breakdown safe operating locus for power transistors. This test facility is capable of determining this locus non-destructively, and therefore can be used to perform 100-per-cent tests of transistor capability in production without destroying transistors. This type of production test is usually made at one point of the second-breakdown locus shown on the published data. Determination of the second-breakdown limit for registration of a new device of a particular structure and geometry previously required the destructive finding of the $I_{S/b}$ limit of many individual transistors. Although each device would yield one data point, the points would not necessarily be on the same second-breakdown locus because the relative second-breakdown capability would vary from device to device. This procedure would therefore not yield accurate information about the actual shape of the $I_{S/b}$ locus. It has been found that the slope, n, of the forward-bias second-breakdown locus ($I = KV^{-n}$) plotted on log-log coordinates is essentially constant for a particular device structure and geometry.

The second-breakdown test set shown in Fig. 3 operates in either of two modes: "normal" operation or "shut-down" operation. There are two feedback drive amplifiers in the circuit. One drives the transistor under test to the magnitude of collector current programmed by adjustment of a potentiometer. The current-sensing feedback loop is arranged so that only actual collector current flows through the sensing resistor; no base current flows in the mesh common to that resistor. The second amplifier compares the collector-to-emitter voltage of a transistor in series with the one being tested to a reference voltage and maintains the pass-transistor voltage constant at six volts, independent of test-current magnitude.

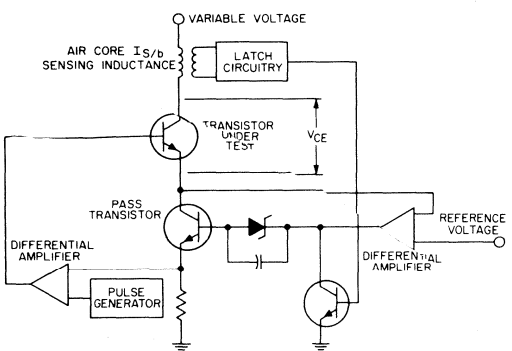


Fig. 3– Simplified schematic of test set for second-breakdown current ($I_{S/b}$).

The test voltage, V_{CE}, is varied by adjustment of the power-supply voltage across the transistor under test, the series pass transistor, and a one-ohm sensing resistor. During a normal test, the pulse generator applies an essentially square pulse of current through the transistor under test; the relatively short rise and fall times can be neglected. The current through the pass transistor tracks the current through the transistor under test. If the device being tested is operating within its safe area, no anomalies in transistor current or voltage occur and no degradation results during the test.

If the transistor is operated beyond its safe operating area, distinct changes occur in current and voltage at the initiation of second breakdown. The collector-to-emitter voltage of the transistor suddenly drops to a low value, while the current rises sharply. The second-breakdown test method shown in Fig. 3 takes advantage of this rapid rise in collector current.

For detection of second breakdown, an air-core inductor is placed in series with collector of the transistor under test. During normal operation of the test set, the voltage developed across this inductor is small because of the relatively long test-current-pulse rise time. During second breakdown, however, the rapidly rising collector current creates a high voltage across the inductor. A secondary winding then ac couples this voltage to a detection circuit which reverse-biases the series pass transistor. The inductive-detection approach is independent of test-current magnitude and reacts instead to the magnitude of its first derivative.

The 2.5-Ampere/300-Volt and 5-Ampere/100-Volt Test Circuits

Two forward-bias second-breakdown facilities are shown in Fig. 4. The first is capable of making second-breakdown tests at collector-current levels to 2.5 amperes and collector-to-emitter voltage levels to 300 volts; the second makes similar tests to 5 amperes and 100 volts.

In both facilities a voltmeter V is placed across the Current-Level-Adjust potentiometer during setting of the test conditions. The drive amplifier is disconnected so that no current flows through the transistor under test. The test transistor must not be preheated before the actual test voltage is applied because the second-breakdown limit decreases with increasing temperature. While the test is being performed, the voltmeter V is switched across the one-ohm sensing resistor and monitors actual test current.

A test is initiated by application of a pulse to the gate of a 2N3228 SCR, Q1, which begins to conduct and closes a mercury relay. A unijunction transistor fires to end the test. The pulse-width potentiometer can be varied to obtain test conditions varying from dc (2 seconds) to a short pulse (100

milliseconds). The setting of the Current-Level-Adjust potentiometer determines the amplitude of the test current during the pulse. The capacitor connected across this potentiometer maintains the rise time of the pulse applied to the differential-drive amplifier at approximately 25 milliseconds, as shown in Fig. 5. If the rise time were too short, the inductive detector would trigger the latch circuitry at the beginning of a pulse and would incorrectly indicate second breakdown.

The pass-transistor regulator maintains a constant voltage across the transistor under test. The series pass transistor is always operated in the active region so that it can turn off the transistor under test within one microsecond if second breakdown occurs.

The two differential amplifiers are stabilized by means of capacitors located at several points. Stabilization of these test facilities is difficult because they are required to perform tests on devices having gain-bandwidth products f_T up to 100 MHz and at all test currents and voltages within the test-set ratings. The problem is compounded by the fact that f_T is a function of collector voltage and current and may vary for individual devices at different test conditions.

Particular care is necessary in the physical layout of a second-breakdown test facility to avoid oscillation. High-frequency oscillations may then incorrectly appear to the inductive detector as second-breakdown failures and cause the protection circuitry to be triggered. Leads should be as short as possible.

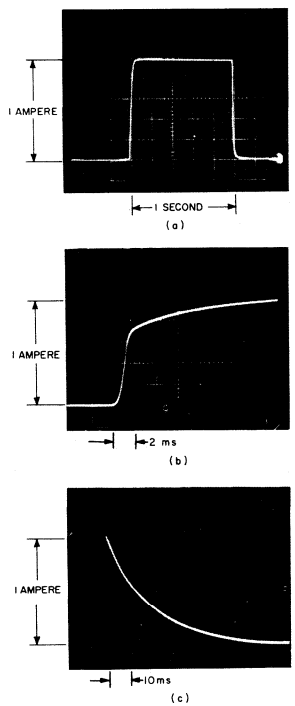


Fig. 5— Waveforms for $I_{S/b}$ test circuits of Fig. 4: (a) applied pulse; (b) turn-on time; (c) turn-off time.

In the event of second breakdown, the large current change di/dt causes a voltage to be coupled to the second-breakdown latch circuitry, Q24 and Q25. This regenerative circuitry drives the pass-transistor regulator, Q16, which then applies instantaneous negative voltage at the base of the pass transistor to interrupt the test current. A light on the front panel of the test set indicates second breakdown. The coupling capacitor in the reset circuitry for the latch is selected so that it cannot override a pulse from the second-breakdown-sensing transformer. If a shorted transistor is placed in the test socket and the reset button is depressed, the resulting instantaneous rise in primary current triggers the latch. Therefore, it is impossible to reset the facility with a shorted transistor in the socket. Although the primary inductance of the sensing transformer is very small, it helps to keep collector current from rising instantly during second breakdown. A diode clamp is employed to damp ringing voltages that might otherwise exceed the avalanche breakdown voltage of the transistor under test.

If the transistor under test has large leakage current, or if a slow thermal runaway occurs, the collector current does not rise fast enough to trigger Q24 and Q25. The latch is then triggered by back-up circuitry. The back-up circuit, which consists of Q21, Q22, and Q23, is a Schmitt trigger set to switch at a collector test current ten per cent higher than the rated value of the test facility. In this case, a relatively long time may be needed to exceed this rating.

Transistor Characterization for Forward-Bias Second Breakdown

Actual second-breakdown measurements for the RCA-2N5240 are shown in Fig. 6. The three curves indicate differences in second-breakdown capability at different case temperatures, but show that the second-breakdown loci have essentially identical slopes. The 2N5240 is a double-diffused triple epitaxial silicon power transistor having eight separate emitter sites. A small ballast is provided in series with each emitter to extend second-breakdown limits.

Characterization of a transistor for second breakdown and power handling is performed in two steps. First, the dc and pulsed power-dissipation capability of the device are calculated on the basis of its steady-state and transient thermal resistance. These curves are then checked empirically to determine at what value of collector-to-emitter voltage second breakdown begins to dominate.

To obtain a single point on the curve, the desired collector-to-emitter voltage V_{CE} is applied to the transistor under test, and a test is performed at a test-current magnitude below the expected capability of the device. If failure does not occur, the test-current magnitude is increased in steps until failure does occur. This procedure is repeated at several values of V_{CE}. During each trial, the transistor case must be at the temperature for which second-breakdown capability is being determined. Usually a

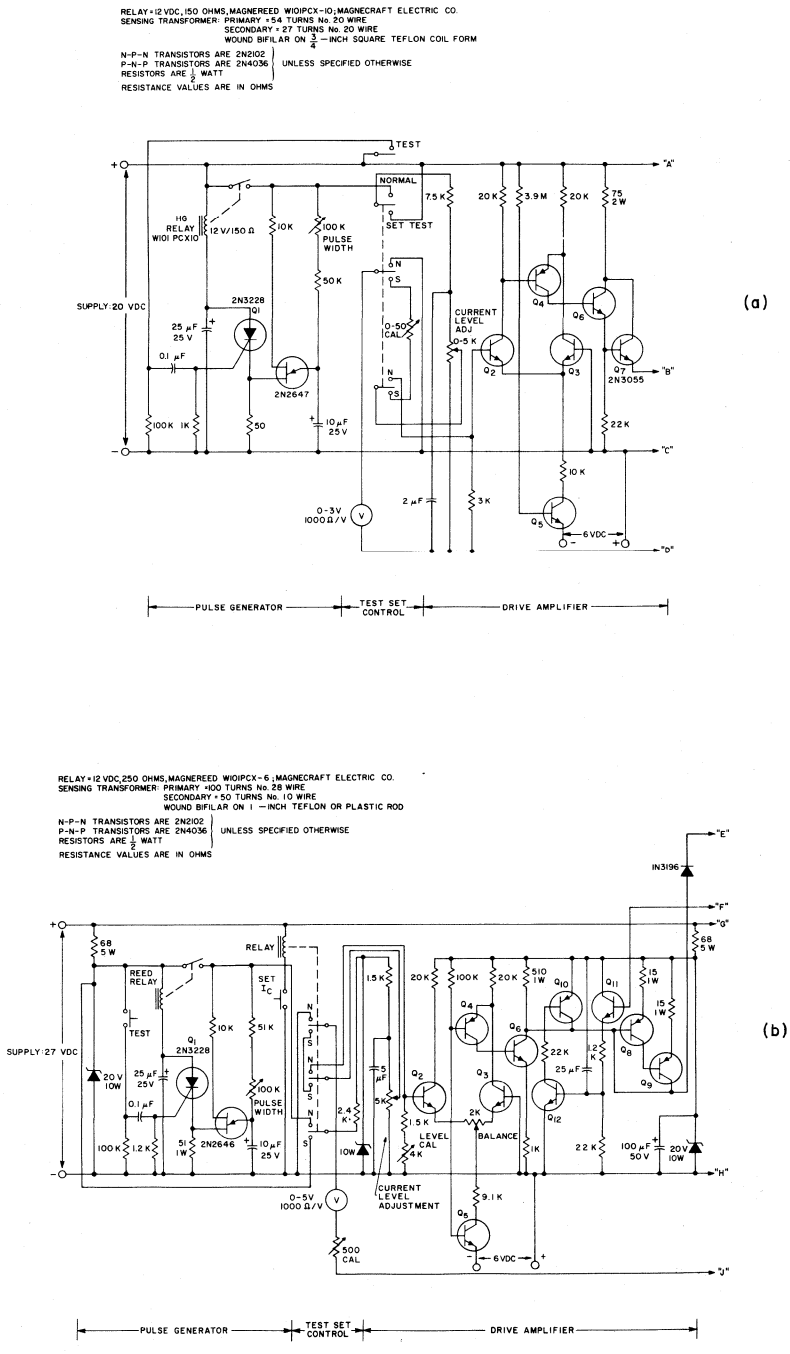


Fig. 4— Schematic diagram of $I_{S/b}$ test facilities for (a) currents to 2.5 amperes and voltages to 300 volts, and (b) currents to 5 amperes and voltages to 100 volts.

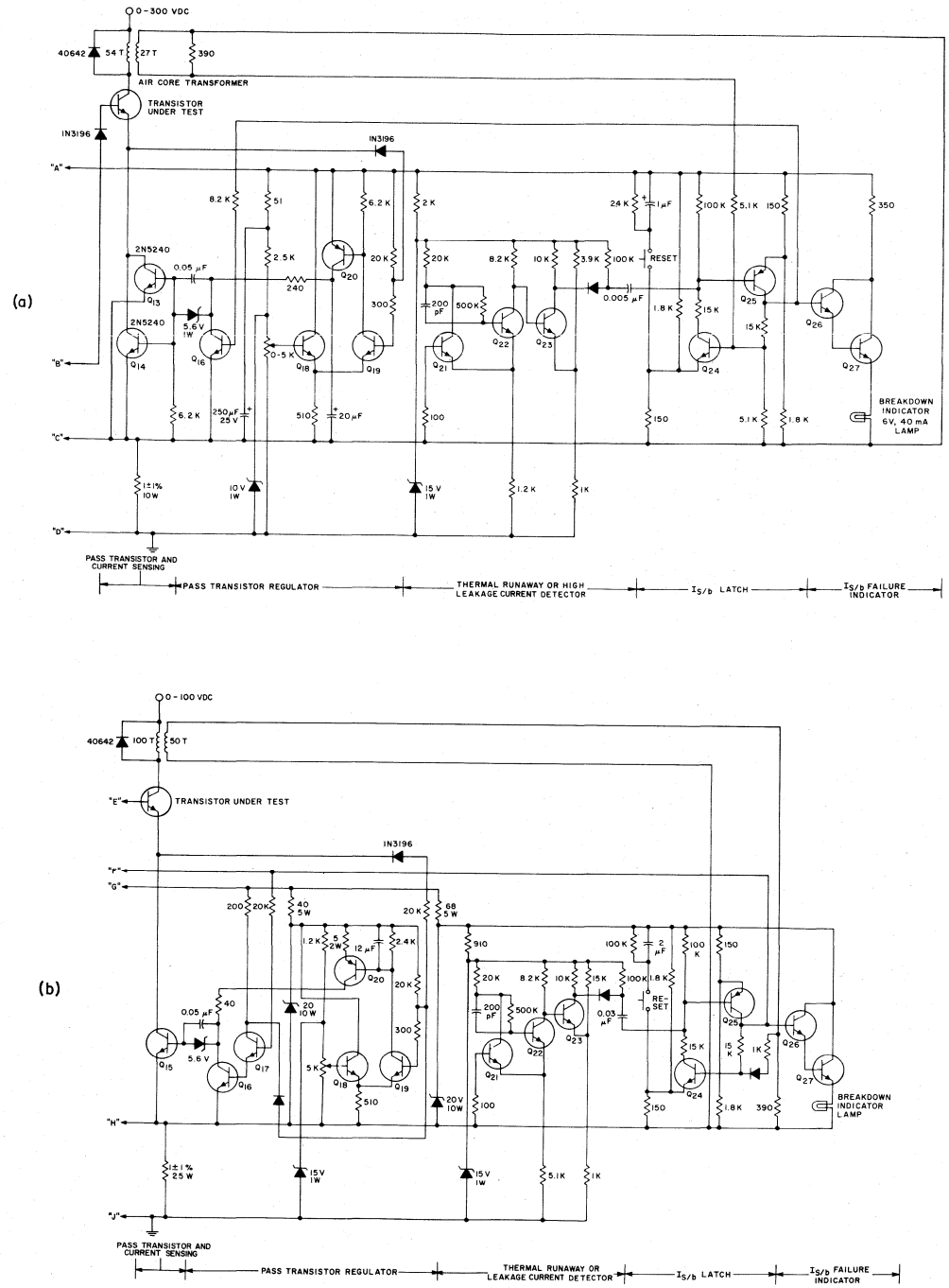


Fig. 4— Schematic diagram of $I_{S/b}$ test facilities for (a) currents to 2.5 amperes and voltages to 300 volts, and (b) currents to 5 amperes and voltages to 100 volts.

heat sink having a large thermal capacity is used. An approximate test for degradation may be made by repeating the second-breakdown test at the current level just preceding device failure; the device should pass this test. Another method is to measure changes in collector cutoff current I_{CBO} after second-breakdown failure.

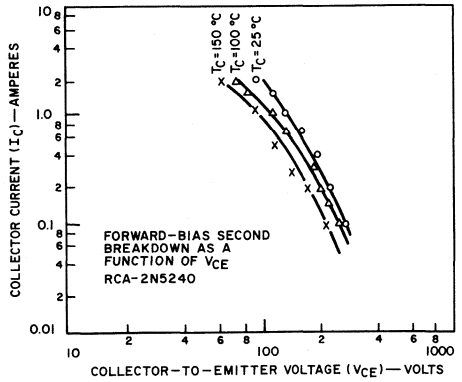


Fig. 6— Forward-bias second breakdown of RCA-2N5240 as a function of collector-to-emitter voltage for different case temperatures.

The final second-breakdown curve plotted to characterize the device for registration, which is shown in the table of device characteristics on the data sheet, has a slope greater than that of the family of devices represented. To guarantee this published curve, a 100-per-cent test is performed in production at the $I_{S/b}$ specification point.

It should be noted that there is not an abrupt change in power-handling capability along the safe-area locus, but rather a gradual change in the slope of the curve. The slope becomes less at lower collector-to-emitter voltages because the electrical base width in the transistor varies as a function of voltage. As V_{CE} decreases, the depletion-region width decreases and the electrical base width increases. These changes have the effect of decreasing current density because the minority carriers in the base have a greater distance over which to diffuse outward laterally, as shown in Fig. 2.

Thermal-Cycling Rating System for Silicon Power Transistors

by W. D. Williams

Thermal fatigue is a wear-out type of failure that may occur in silicon power transistors as a result of the thermal cycling produced by changes in power dissipation or in the ambient temperature. When a transistor is alternately heated and allowed to cool, cyclic mechanical stresses are produced within the device because of differences in the thermal expansion of the silicon pellet and the metallic materials to which the pellet is attached. In the past, the effect of such stresses has been almost completely ignored in the design of power-transistor circuits. The circuit designer should realize, however, that, just as a wire that is continuously flexed at one point will eventually break because of metal fatigue, cyclic thermal stresses can similarly lead to fatigue failures in power transistors.

This Note briefly analyzes the basic causes of thermal fatigue in silicon power transistors and describes a rating chart that makes it possible for a circuit designer to avoid such failures during the operating life of his equipment. Examples are provided on the use of this chart to determine the transistor operating conditions required to assure a desired thermal-cycling capability and to determine whether the thermal-cycling capability of a transistor is adequate for the requirements of a given application.

Analysis of Thermal Fatigue in Silicon Power Transistors

Power transistors are subjected to some thermal stresses in all practical circuits in which they may be employed. In many common applications, these stresses are very severe, as indicated by the examples of the thermal-cycling requirements of several typical applications listed in Table I. The cyclic stresses may eventually result in physical damage to the semiconductor pellet or the mounting interface.

In most silicon power transistors, the small silicon pellet is bonded to a copper header. The coefficient of thermal expansion for silicon (3×10^{-6}) is much less than that of copper (17.5×10^{-6}). Temperature variations within the transistor, therefore, result in cyclic stresses at the mounting interface of the silicon pellet and the copper header because of the difference in the thermal expansions of these parts. If a hard solder, such as silicon gold, is used to bond the pellet to the header, these stresses are transmitted to the silicon pellet. Silicon is relatively weak in tensile strength and is highly "notch sensitive." Such stresses therefore, often result in pellet fractures. In general, however, lead solder is used to bond the silicon pellet to the copper header. The cyclic thermal stresses then are absorbed by non-elastic deformation of the soft lead solder, and very little stress is transmitted to the pellet.

The continuous flexing that results from cyclic temperature changes in the transistor may eventually cause fatigue failures in the lead solder. Such failures are a function of the amount of change in temperature at the mounting interface, the difference in the thermal-expansion coefficients of the silicon pellet and the material to which the pellet is attached, and the maximum dimensions of the mounting interface.[1] Fatigue failures occur whenever the cyclic stresses damage the solder to the point at which the transfer of heat between the pellet and the surface to which it is mounted becomes impaired. This condition may exist in only a small portion of the pellet. This portion, however, overheats, and transistor failure results because of conditions that very closely approximate those encountered during second breakdown.[2]

Thermal-fatigue failures in power transistors are accelerated because of dislocation "pile-ups" that result from impurities in the lead solder.[3] RCA has developed a process that substantially reduces the amount of impurities introduced into the solder. Use of this proprietary "controlled solder process" (CSP) makes it possible to avoid the microcracks that propagate to cause fatigue failure in power transistors and, therefore, greatly increases the thermal-cycling capability of these devices.[4]

Thermal-Cycling Rating Chart

The mathematical relationship among the factors that affect fatigue failure in silicon power transistors can be expressed, in terms of the number of thermal cycles to failure N, as follows:[1]

$$N = Ae^{\psi_o / [\triangle T(\alpha_A - \alpha_B) L]}$$

Table I - Thermal-Cycling Requirements for Typical Applications of Power Transistors

Application	Circuit	P_T (W)	ΔT_C (°C)	Minimum Equipment Life Required (years)	Typical Thermal-Cycling Rating Required (cycles)
Auto radio audio output	Class A	8	75	5	5,000
	Class AB	2	45	5	5,000
Power supply	Series regulator	50	65	5	5,000
	Switching regulator	15	65	5	5,000
Hi-Fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series regulator	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^8
Television	Vertical output	10	75	5	5,000
	Audio output	8	75	5	5,000
Sonar modulator	Linear amplifier	100	55	10	144×10^3

where A is a constant determined by the mounting system, ΔT is the change in temperature at the mounting interface, α_A and α_B are the thermal-expansion coefficients of the silicon and the metal under the solder joint, ψ_O is a material constant proportional to the change in temperature ΔT and the difference in the thermal-expansion coefficients α_A and α_B, and L is the maximum length of the solder joint under the pellet.

For a given transistor, the only variable in the thermal-cycling equation that can be controlled by the circuit designer is the change in temperature at the interface of the silicon pellet and the material to which the pellet is mounted. This change in temperature ΔT is, of course, less than the change in transistor junction temperature ΔT_J, but is greater than the change in case temperature ΔT_C.

RCA has devised a rating chart that relates the thermal-cycling capability of a silicon power transistor to total device dissipation and the change in case temperature. This chart is presented in the form of a log-log presentation in which power dissipation is shown on the vertical axis and the number of thermal cycles is shown on the horizontal axis. Rating curves are shown for various magnitudes of case-temperature swings. Fig. 1 shows an example of a typical rating chart of this type.

A circuit designer may use the rating chart to define the limiting value to which the change in case temperature must be restricted to assure that a power transistor is capable of operation at a specified power dissipation over the number of thermal cycles required in a given application. Conversely, if the power dissipation and the change in case temperature are known, the designer may use the rating chart to determine whether the thermal-cycling capability of the transistor is adequate for the application. These uses of the rating chart are illustrated by examples on the chart shown in Fig. 1.

The chart shows the thermal-cycling ratings for an experimental silicon power transistor that has a thermal

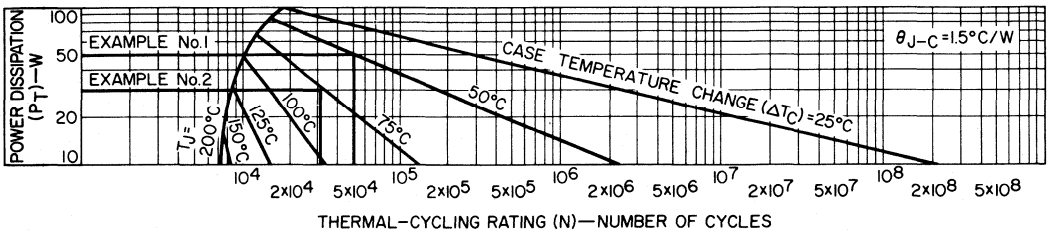


Fig. 1– Thermal cycling rating chart

resistance from junction to case of 1.5°C per watt. If a designer wishes to determine the maximum allowable change in the case temperature of this transistor for the thermal-cycling requirements of a given application, he simply plots the point of intersection of a horizontal projection of the total device dissipation with a vertical projection of the total number of thermal cycles required in the application. If this point lies exactly on one of the power-dissipation curves, the maximum allowable change in case temperature can be read directly from the chart; if not, the allowable temperature change can be approximated by linear interpolation. This use of the rating chart is illustrated by example No. 1 in Fig. 1.

For this example, it is assumed that the transistor is to be operated intermittently at a power dissipation level of 50 watts and that a thermal-cycling capability of 5.0×10^4 cycles is required to assure that the life of the transistor exceeds that of the equipment in which it is to be used. The point of intersection of line projections of the power dissipation and the required number of thermal cycles indicates that the change in case temperature must be restricted to a maximum value of 50°C per thermal cycle. This value determines the requirements of the transistor heat sink. If the thermal cycles are long in comparison to the thermal time constant of the heat sink, the total thermal resistance from case to ambient should not exceed 1°C per watt. If the thermal cycles are short relative to the thermal time constant, a higher thermal resistance is permissible provided that the thermal capacitance of the heat sink is sufficient to assure that the change in case temperature does not exceed 50°C during the thermal cycle.

Example No. 2 in Fig. 1 illustrates the use of the rating chart to determine whether the thermal-cycling capability of a transistor is adequate for a given application. In this example, a transistor dissipation of 30 watts and a case-temperature swing (measured) of 75°C are assumed. A vertical projection of the 30-watt point on the $\triangle T_C = 75°C$ power-dissipation curve indicates that, for these operating conditions, the transistor has a thermal-cycling rating of 3.2×10^4 cycles. If this rating is not adequate for the intended application, either the power dissipation must be reduced or a larger heat sink must be used so that a smaller change in case temperature will result during a thermal cycle.

In many applications, a power transistor may be subjected to thermal cycles that differ in both duration and magnitude. In such instances, the fractional amount of the thermal-cycling life of the transistor used by the total number of thermal cycles of each type during the required life of the equipment must be separately determined and then added together to ascertain whether the thermal-cycling rating of the transistor will be exceeded in the application. The ratio of the total number of cycles of each type to which the transistor will be subjected during the life of the equipment to the total number of cycles of the same type that the transistor is rated to withstand before fatigue failure is obtained for all the dissimilar thermal cycles. If the sum of these ratios is less than unity, the transistor is obviously operated within ratings in the application. If the sum is greater than unity, the thermal-cycling rating of the transistor is exceeded in the application, and device failure may occur during the operating life of the equipment.

The technique used to determine whether the thermal-cycling ratings of a transistor are exceeded in a specific application in which the transistor is subjected to different types of thermal cycles can be illustrated by use of the examples of different operating conditions shown in Fig. 1. If the transistor is assumed to be subjected to the conditions specified for examplele No. 1 for 2.5×10^4 thermal cycles and to the conditions specified for example No. 2 for 1.6×10^4 thermal cycles, the following summation is made to determine whether the transistor will be operated within its thermal-cycling ratings:

$$\frac{2.5 \times 10^4}{5.0 \times 10^4} + \frac{1.6 \times 10^4}{3.2 \times 10^4} = 1$$

This summation indicates that, for the conditions assumed, the transistor is operated exactly to the limit of its thermal-cycling rating.

The RCA thermal-cycling ratings allow a circuit designer to use silicon power transistors with assurance that no fatigue failures of these devices will occur during the operating life of his equipment. These ratings provide valid indications of the thermal-cycling capability of silicon power transistors for all types of operating conditions and, therefore, enable the circuit designer to "design out" the possibility of transistor thermal-fatigue failures.

Obviously, all power transistors cannot be tested to determine their thermal-cycling capability because such tests are expensive, time consuming, and destructive. The validity of the thermal-cycling ratings results from the application of stringent process controls at each step in the manufacture of the transistors and from the testings of a statistically significant number of samples. Thermal-cycling ratings for silicon power transistors provide the same type of assurance that a device will not fail when operated within ratings as that provided by the more familiar voltage, current, and second-breakdown ratings.

Bibliography

1. G.A. Lang, et al, "Thermal Fatigue in Silicon Power Transistors," *IEEE Transactions on Electron Devices,* pp. 787-793, Sept. 1970.
2. C.R. Turner, "Carl Turner of RCA Speaks Out on Second Breakdown," *EEE,* Vol. 15, No. 7, July 1967.
3. J.J. Gilman, "Dislocation Mobility in Crystals," *J. Appl. Phys.*, Vol. 36, pp. 3195-3206, October 1965.
4. *RCA High-Speed, High-Voltage, High Current Power Transistors,* Technical Series PM-80, RCA Solid State Division, Somerville, N.J., May 1970.

Evaluation of Hermeticity of Aluminum TO-3 Packages Under Thermal-Cycling Conditions (Reliability Report)

A program that continually upgrades product and develops meaningful rating systems is a requirement in the power-semiconductor business. RCA's program has played a major role in the development of products and has led to the specification of IS/b, ES/b, and thermal-cycling ratings. RCA's experience in determining the thermal-cycling ratings of power transistors has shown that package material and assembly systems must be looked at very carefully from a thermal-fatigue viewpoint. This report evaluates the thermal capabilities of our competitors' aluminum TO-3 package with soldered-in leads against the RCA steel TO-3 package with glass-sealed leads.

Failure Data

In conjunction with its ongoing thermal-cycling rating program, RCA continually evaluates product from its major competitors. The results of this evaluation are quite significant in the case of the aluminum TO-3 package. Type 2N3055 product in the aluminum TO-3 package from three major competitors has been evaluated and the results compared to those achieved with RCA's steel TO-3 package. None of the competitors' product tested passed RCA's thermal-cycling criteria, and, in addition, all of the product demonstrated early failures in thermal-fatigue tests for hermeticity. It is RCA's opinion that the aluminum package as it is now manufactured is unacceptable, and that, in addition, it has some fundamental engineering problems that indicate that it may never be a viable hermetic-package system. Tables I and II show typical examples of the data gathered during tests of Type 2N3055 devices in aluminum TO-3 packages. Tables III and IV show additional data on a second, recently announced transistor type housed in the aluminum TO-3 package. Note that most failures occurred before 5000 cycles.

Failure Analysis

Helium Leak Test — Before and after each test, all units were checked by submitting them to a four-hour helium bomb and then to a helium-leak detector.

Freon Bubble — The freon-bubble test is a gross-leak test in which the units are freon-bombed overnight (in FC-78 helium) and then submerged in hot freon (FC-43) and checked for bubble exodus. Analysis of the leakers showed that the devices lost hermeticity at the glass eyelet assemblies (emitter and base leads) that are soldered into the aluminum header after the number of thermal cycles indicated. Note that no RCA devices failed the thermal-cycling test. RCA steel TO-3 devices were included in these tests only as controls; the life of the RCA steel-packaged 2N3055 on the 16-W thermal-cycling test is typically well beyond 100,000 cycles before first failures.

Table I — Results of 16-W Thermal-Cycling Test of 2N3055 — 10,000 Cycles
(T_C = 40 to 130°C, No. of Units = 10

TEST	NO. OF FAILURES ALUM. TO-3 Mfr. A	Mfr. B	Mfr. C	STEEL TO-3 RCA
Helium Leak — Fine	8	4	3	0
Freon Bubble — Gross	2	5	0	0
Total	10	9	3	0
Cumulative Electrical Failures for 10,000 Cycles	7 Short	5 Short 1 θ_{jc}*	1 Open 4 Short	0

*θ_{jc} increased more than 25 percent

Table II — Results of Temperature-Cycling Test of 2N3055 — 75 Cycles
(T_C = −65 to +150°C, No. of units = 15)

TEST	NO. OF FAILURES ALUM. TO-3 Mfr. A	Mfr. B	Mrf. C	STEEL TO-3 RCA
Helium Leak — Fine	9	14	5	0
Freon Bubble — Gross	0	1	1	0
Total	9	15	6	0

Table III – Results of 16-W Thermal-Cycling Test on Second Device – 3000 Cycles

(T_C = 40 to 130°C, No. of units = 12)

TEST	NO. OF FAILURES ALUM. TO-3 MANUFACTURER A
Helium Leak – Fine	0
Freon Bubble – Gross	9
Total	9

Table IV – Results of Temperature Cycling Test on Second Device – 25 Cycles

(T_C = –65 to +150°C, No. of units = 12)

TEST	NO. OF FAILURES ALUM. TO-3 MANUFACTURER A
Helium Leak – Fine	0
Freon Bubble – Gross	3
Total	3

Engineering Problem

Fig. 1 shows an exploded view of the aluminum TO-3 package; all three competitors use lead eyelet assemblies that are soldered into the aluminum flange. The cyclic heating and cooling of the aluminum package cause expansion and contraction of the flange with respect to the eyelet assembly and propagate microcracks that ultimately cause leaks. Contamination of the solder holding the eyelet assembly probably initiates the problem.

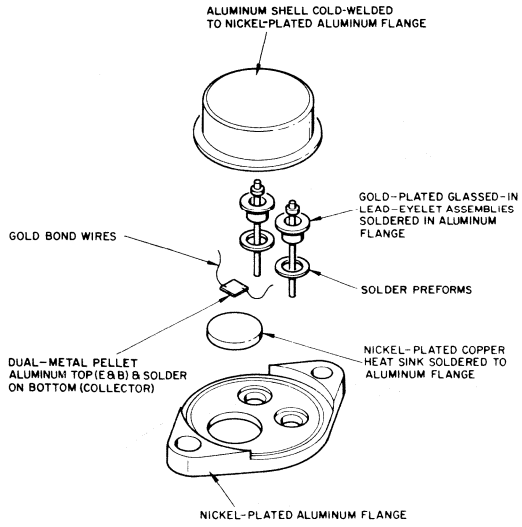


Fig. 1– Aluminum TO-3 package.

Fig. 2 shows the RCA steel TO-3 package. Note the glass-to-stem seal with no solder interface. This configuration is possible with the steel package because the melting point of steel is far higher than the melting point of glass. It is not possible to use the same system with the aluminum header because the melting point of aluminum is below that of the glass used in the seal. Consequently, manufacturers who use aluminum packages are forced to use a soldered-in assembly.

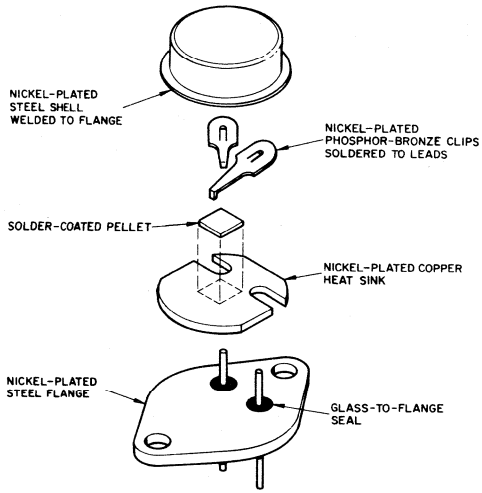


Fig.2– RCA steel TO-3 package.

Conclusion

RCA's competitors have proclaimed the attributes of aluminum packages and hard-solder power (the power available from a package in which the pellet has been mounted by the use of a hard-solder method). We believe that the soldered-in eyelet associated with the aluminum package has serious reliability and fundamental engineering problems. This is also true of their so-called "hard-solder" packages, which use the same type of soldered-in eyelet assemblies. RCA's steel package with its glass-to-stem seal, welded cap, and controlled solder process, is far superior to the aluminum package and hard-solder mounting system-over an order of magnitude better. The aluminum package has a long way to go to compete. The customer who buys a device in a TO-3 package may think he is buying long-term hermeticity; he may have a serious problem if it's aluminum.

Quantitative Measurement of Thermal-Cycling Capability of Silicon Power Transistors

by L. J. Gallace

This Application Note discusses the methods used to test the thermal-cycling capability of power transistors. A brief description of thermal fatigue, application requirements, and rating charts is given. A detailed discussion of the practical design of thermal-cycling racks is also included along with actual test conditions for various power-transistor types. Acceleration factors, failure indicators, failure mechanisms, and real-time control of thermal-cycling capability of factory product are discussed. Some information is also given on hermetic versus plastic-package thermal-cycling reliability.

In silicon power-transistor applications, thermal cycling of transistors may activate a failure mechanism called thermal fatigue. This phenomenon is caused by the mechanical stresses set up by the differentials in thermal expansion of the various materials used in the transistor assembly and heat sink. Thermal fatigue often causes the silicon pellet to crack or to fail at the silicon/mounting interface.

The number of cycles to failure in terms of device characteristics and operating conditions has been expressed as:

$$N = Ae^{\frac{\psi_0}{(\alpha_1 - \alpha_2)\,\Delta T\,L}}$$

where A and ψ_0 are constants for a given power structure, $(\alpha_1 - \alpha_2)$ is the difference in thermal expansion between the silicon die and the material on which it is mounted, ΔT is the change in temperature at the interface between the silicon chip and the material to which it is mounted, and L is the maximum dimension of the silicon chip.

APPLICATION REQUIREMENTS

Table I shows typical applications of power transistors and the number of cycles or cycle life required of transistors used in equipment in each application to allow the equipment to fulfill its life expectancy. The importance of cycle life can be shown by examining the following simple expression of the failure-rate equation, which characterizes device failure rates:

$$\lambda = \lambda_T\,\pi_Q\,\pi_E\,\pi_L\,\pi_P + \lambda_{\Delta T_C}$$

where λ = failure rate
λ_T = base failure rate due to temperature (Arrenhius)
π_Q = quality factor
π_E = environmental factor
π_L = learning curve
π_P = package factor
$\lambda_{\Delta T_C}$ = change in case temperature

Table I reflects the increasing demand for more thermal-cycle-life capability from equipment manufacturers because of their lengthening warranty periods. This lengthening of warranty period has greatly increased the demand on power-transistor manufacturers to test and ensure product capability over a longer period of time. RCA has developed a rating chart, Fig. 1, that relates the thermal-cycling capability of silicon power transistors to total device dissipation and the change in case temperature. A circuit designer may use the rating chart to define a limiting value below which power dissipation and change in case temperature are not factors in the failure rate equation; i.e., *within this rating chart, the failure rate for power transistors is independent of cycle life.* This statement does not imply that failures will not occur; it does imply, however, that the last term in the failure-rate equation is small enough to be insignificant. Since the change in case temperature is a major consideration in many applications, product with superior capability in this parameter will produce lower field-failure rates.

FAILURE ANALYSIS

Soft-Solder Devices

In soft-solder devices, the metal interfaces between the emitter, base, and collector contacts consist of nickel-lead-tin metals which expand and contract at different rates during thermal cycling, and, consequently, strain occurs. Because of the difference in coefficients of expansion of these materials, an appreciable amount of shearing takes place that causes

TABLE I – THERMAL-CYCLING REQUIREMENTS FOR TYPICAL APPLICATIONS OF POWER TRANSISTORS

APPLICATION	CIRCUIT	P_T (W)	ΔT_C (°C)	MINIMUM EQUIPMENT LIFE REQUIRED (YEARS)	TYPICAL THERMAL-CYCLING-RATING REQUIRED (CYCLES)
Auto radio	Class A	8	75	5	5,000
Audio output	Class AB	2	45	5	5,000
Power supply	Series regulator	50	65	5	10,000
	Switching regulator	15	65	5	10,000
Hi-Fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series regulator	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^8
Television	Vertical output	10	75	5	7,500
	Audio output	8	75	5	7,500
Sonar modulator	Linear amplifier	100	55	10	144×10^3

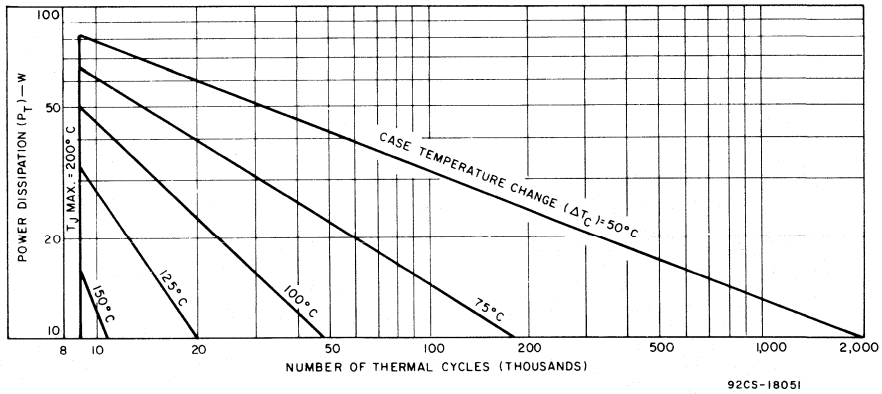


Fig. 1 – Thermal-cycling rating chart for an RCA hermetic power transistor.

fatigue failure at the contact point. The longer the stress continues, the more the solder moves to relieve the stress. If the movement continues long enough, the joints will rupture, and actual physical displacement of the silicon pellet will occur; this displacement is called pellet "walk." Linear movements of as much as 20 mils have occurred.

Hard Solder

The predominant failure mechanism in hard-solder devices is failure in the silicon crystal. Since no plastic flow occurs in hard solder, invariably the silicon must take up some of the strain in the system. Cracks in the silicon, generally under the bonding-wire area, are the most common failure mechanism.

PRACTICAL TESTING

Although analytical techniques have been most helpful in developing an understanding of thermal cycling as a failure producer, testing, the experimental approach, must still be used to determine the ultimate thermal-cycling capability of a power transistor.

Fig. 2 is a schematic diagram of the basic test circuit. Depending on the frequency response of the transistor to be tested, this circuit is modified to avoid parasitic oscillation. Modification generally takes the form of capacitors, usually connected collector-to-emitter, or ferrite beads on the emitter and base leads.

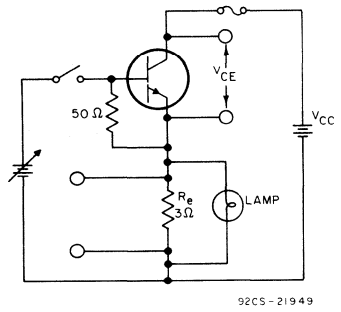


Fig. 2– Test circuit.

Fig. 3 is a photograph of a typical test rack without the associated power supplies. The Appendix contains a complete parts list and mechanical layout for this thermal-cycling rack. In addition, the Appendix shows a layout and parts lists for sockets that accommodate both TO-220 VERSAWATT (plastic) and TO-3 hermetic transistors.

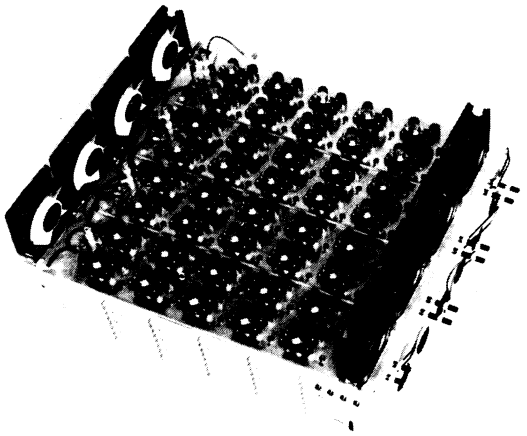


Fig. 3– Test rack used in thermal-fatigue testing.

The design of the test rack stresses simplicity and universal use. By interchanging sockets, 40 devices including almost all power-transistor types can be tested. Eight fans are used to cool the devices on the off cycle. Most tests can be conducted under free-air conditions; however, if heat sinks are used, power levels up to 56 watts per socket can be handled.

Under these higher-power conditions, a temperature gradient will exist across the rack with the highest temperature at the center. A simple method to compensate for this gradient is to increase the size of the heat sink on the sockets as the distance from the fans increases.

Mechanical timers are used to control the on-off cycle time. For very fast cycle time (40 seconds or less), high-torque motors are recommended for longer timer life. Solid-state timers have also been used.

A thermocouple is used to monitor the cycle temperature continuously. For more important tests, when equipment failure cannot be tolerated, over-temperature controls set 5 to 10°C above the maximum temperatures of the test are used. When activated, the control will open the base drive circuit and keep it open until manually reset. This method may also be used to cycle the tests on and off, but the cost is higher than when mechanical timers are used.

Jacks are provided on the front panel of the rack for monitoring emitter current. The light bulb connected across the emitter resistor is a visual aid to help detect intermittent emitter-base contacts. The number of test cycles is automatically recorded on a counter.

Since thermal cycling of power transistors requires high-current power supplies (50 to 100 amperes), consideration must be given to thermal-fatigue-induced power-supply failures. If 50-per-cent duty cycles are used, then switching can be arranged so that there is a constant load on the power supply. For duty cycles other than 50 per cent, resistive loads can be switched in during the transistor off cycle. Multiple timers driven from the same motor can be used to service up to three racks from one collector power supply when more than one rack uses the same cycle time.

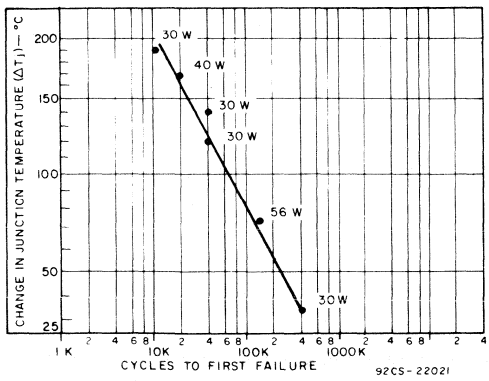
TEST CONDITIONS

A thermal-fatigue test is basically a cyclical, operating-life test. For room-ambient testing, the important test parameters are:

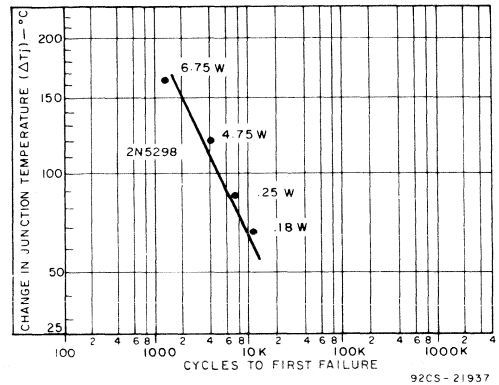
P_d, collector dissipation;
ΔT_c, change in case temperature;
ΔT_j, change in junction temperature;
T_{jmax}, maximum junction temperature;
θ_{jc}, junction-to-case thermal resistance; and cycle time.

In empirically determining the power-cycling capability of a power transistor, it was found that the single most important parameter was ΔT_j. Although T_{jmax} and cycle time were also significant factors, it was shown that most of the predictive methods and acceleration factors could be based on ΔT_j; 70 per cent of the experimental data could be explained by this one parameter as long as the power range for ΔT_j did not exceed a maximum of 3 to 1.

Fig. 4 shows plots of ΔT_j as a function of cycles-to-first-failure on Arrenhius-type paper for a 2N3055 transistor in a hermetic TO-3 package and a 2N5298 transistor in a TO-220 VERSAWATT package. The data show a "good" fit relatively independent of power. These curves can be used to predict power-cycling capability at lower ΔT_j values with good accuracy.



(a) 2N3055



(b) 2N5298

Fig.4 – Change in junction temperature as a function of cycles-to-first-failure for a 2N3055 transistor in a hermitic TO-3 package and a 2N5298 transistor in a TO-220 VERSAWATT package.

Some recommended test conditions for evaluating product to the published rating curves are shown in Table II. All of the test conditions given can be achieved on the test rack shown in Fig. 3 and described in the Appendix.

Although most failures are detected while a device is under operation on the thermal-cycling test racks, sufficient down-period readings should be recorded to indicate shifts in parameters that are indicators of changes in the device metallurgical system. The most critical parameters to record as variables data are thermal resistance (junction to case), beta, V_{BE}, $V_{CE(sat)}$, and I_{CEO}.

Package Differences (Hermetic vs. Plastic)

The thermal-cycling capability of a plastic-packaged device is generally less than that of its hermetically packaged counterpart even though the maximum ratings of the devices are substantially different (150°C plastic, 200°C hermetic). This difference in capability is attributed to the condition which, in the plastic package, allows the emitter and base leads, embedded in the plastic mold, to be continually moved across the silicon chip during thermal cycling, thus causing eventual failure as a result of open contacts. Fig. 5 shows rating curves for the same pellet (2N3055) in both the plastic VERSAWATT and TO-3 hermetic packages.

TABLE II – RECOMMENDED TEST CONDITIONS

PACKAGE TYPE	POWER (WATTS)	T_C(°C)	ΔT_C(°C)	t_{on}	t_{off}	HEAT SINK
TO-220 VERSAWATT	18	55 to 110	55	3 min.	3 min.	3°C/W
	4.75	35 to 155	120	50s	100s	Free Air
TO-3 Hermetic	16	40 to 130	90	50s	100s	Free Air
	56	70 to 120	50	15s	25s	6.3°C/W
TO-66 Hermetic	8.5	35 to 155	120	50s	100s	Free Air
RCA "TO-5" Plastic	1.5	35 to 135	100	60s	90s	Free Air
TO-5 Hermetic	1.5	30 to 115	85	60s	90s	Free Air

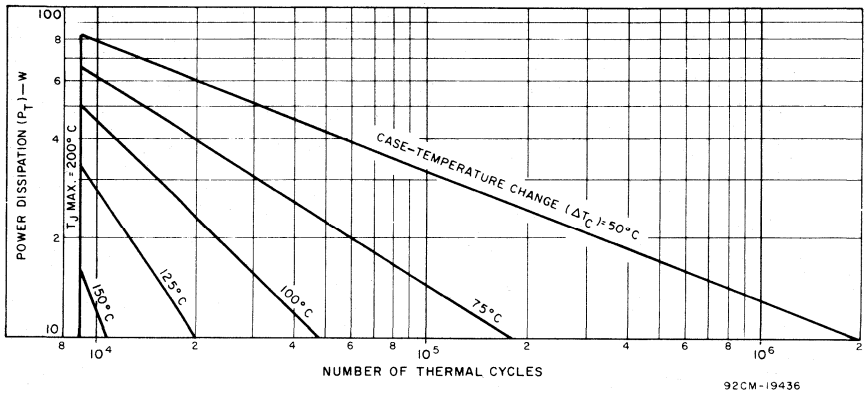


Fig. 5a – Thermal-cycling rating curves for a 2N3055 pellet in a TO-3 hermetic package.

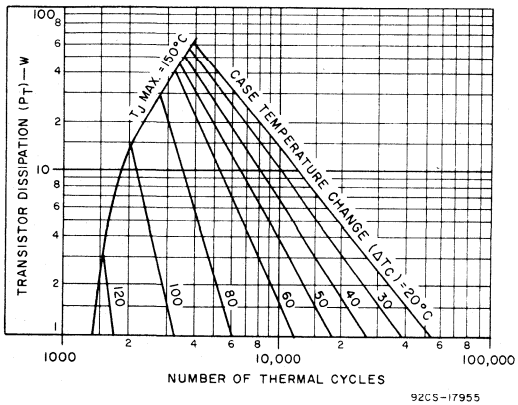


Fig. 5b – Thermal-cycling rating curves for a 2N3055 pellet in a plastic VERSAWATT package (2N6103).

There are also cases where performance of a plastic package may be superior to some types of hermetic-package designs. For example, some aluminum TO-3 packages with solder-in emitter-base feedthroughs have shown substantially less capability on thermal cycling than their plastic VERSAWATT counterparts. In addition, the aluminum packages that have been measured become nonhermetic after a relatively low number of thermal cycles (less than 5000). Obviously then, care must be exercised in the selection of power transistors to avoid basing the choice upon package categories as general as "plastic" and "hermetic."

Real-Time Controls (RTC)

A major innovation in using the methods described to test for thermal-cycling capability is to monitor the thermal-cycling capability of factory product on a lot-by-lot basis. Essentially, real-time control, or RTC, makes a continuous acceptance test and interpolation of thermal-cycling data against some established criteria. Information generated internally by RTC on thermal cycling has unquestioned validity because conditions of tests are well controlled and all ambiguities have been removed. Current as well as historical and projected operating information is generated for analysis.

The types of tests which are used in RTC are designed to produce information in three days for providing process control data. Typical examples of real-time control conditions are shown in Table III.

TABLE III – TYPICAL EXAMPLES OF REAL-TIME CONTROL CONDITIONS

TYPE	POWER (WATTS)	T_C(°C)	ΔT_C(°C)	CYCLES/DAY	N	TEST DURATION	AC NO.
TO-220	4.75	35 to 155	120	576	40	1700	0
VERSAWATT						3000	1
TO-3	56	70 to 120	50	2200	40	4400	0
Hermetic						6600	1

APPENDIX

Thermal-Cycling Test Rack Parts List (Figs. A1, A2, A3, A4)

2	Counters	ITT General Controls CE600BS 602 120 V 60 Hz
2	Relays	Potter & Bromfield PR11AY - DPDT - 120 V AC
40	L–10/20 Rated for 10 V Lamps	Mura Corp. Great Neck, N. Y. With Red Lens Cap
8	Fans	IMC Magnetics Corp. Boxer Fan Model No. BS2107F
4	Barrier Blocks	Three Contacts, Thru-Panel Solder Lugs Cinch-Jones - Series 3–142–Y
81	Fuse Holders	Little Fuse Type 342012
1	AC Line Cord	Belden No. 17419 9 Ft. No. 16–3 Type SJ Rubber
4	Switches	SP/ST Cutler-Hammer No. 7580K7
8	Neon Lamps	American Pamcor Paoli, Pa. No. 380627–2
40	3 Ohms - 25 W Resistors	Ohmite No. 0200L Style 270–25
40	Banana Jacks	Red - E.F.Johnson - No. 108–902
80	Banana Jacks	Green - E.F.Johnson - No. 108–904
40	Banana Jacks	Blue - E.F.Johnson - No. 108–910
4	Binding Posts	Blue - E.F.Johnson - No. 111–110
2	Binding Posts	White - E.F.Johnson - No. 111–101
2	Binding Posts	Black - E.F.Johnson - No. 111–103
40	Fuses	4 A Littelfuse 312 004
40	Fuses	½ A Littelfuse 312 500
2	Fuses	2 A Littelfuse 312 002

Cycling Control Box

1	Timer	Industrial Timer Corporation Parsippany, New Jersey MC1 with Two Switches (Cycle Time: 4 to 36 secs.) High-Torque Motor With A-36 Gear Rack (115 V - 60 Cycle)
1	Neon Lamp	American Pamcor Paoli, Pa., No. 380627–2
2	Banana Jacks	Red - E.F. Johnson - No. 108–902
2	Banana Jacks	Green - E.F. Johnson - No. 108–904
2	Banana Jacks	Blue - E.F. Johnson - No. 108–910
1	Switch	SP/ST Cutler-Hammer No. 7580K7
1	AC Line Cord	Belden No. 17419 9 Ft. No. 16–3 Type SJ
1	Chassis	Bud - Aluminum 4 x 5 x 6 in. No. AU–1029

Sockets

80	TO-3	6/32 Screws 3/4 in. long
80	TO-3	6/32 Nuts 1/4W x 3/32H
80	TO-3	6/32 Nuts 1/4W x 1/2H
80	TO-3	6 Lock Washers
40	TO-220	Socket Base Pomona Electronics Company Pomona, California Model 2095
40	TO-220	Sockets Jettron Products, Inc. Hanover, N. J. CD 74-104
	TO-220	See Assembly Drawing (Fig. A5)
40	TO-66	Tektronix, Inc. No. 013-0070-01
40	TO-3	Cover Plate for Pomona Socket See Detailed Drawing (Fig. A6)
40	TO-3	Socket Base Pomona Electronics Company Pomona, California Model 2095
40	TO-3	Socket – E B Y No. 9866-15-1
	TO-3	Heat Sink: Wakefield Engineering Delta Division
16	TO-3	NC-631-3 (Wakefield Engineering, Delta Division)
16	TO-3	NC-632-3 (Wakefield Engineering, Delta Division)
8	TO-3	Fabricate – See Detailed Drawing (Figs. A6, A7)

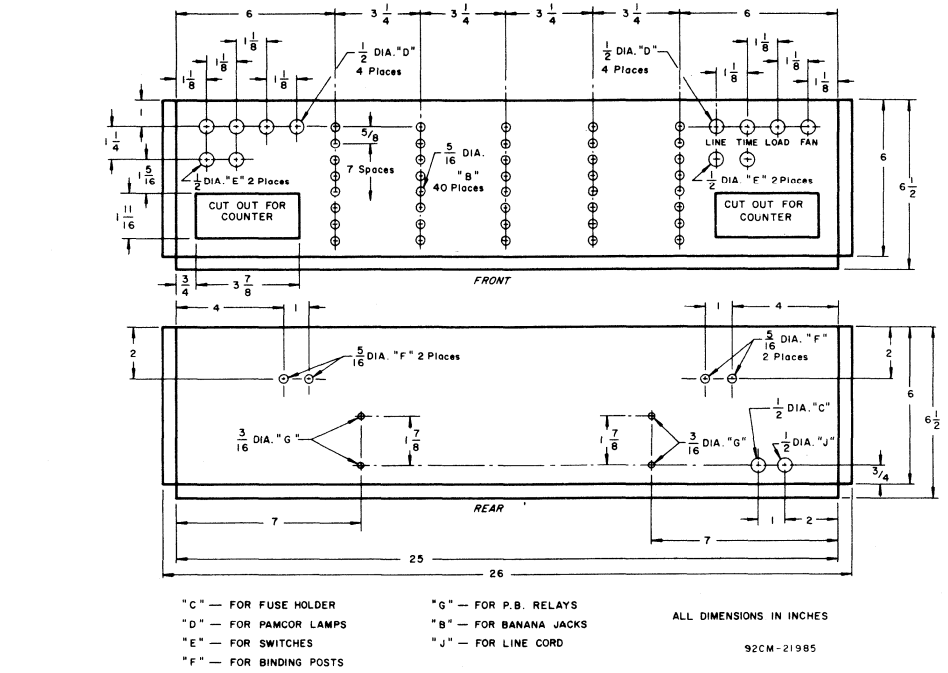

6
3 1/4
3 1/4
3 1/4
3 1/4
6
1/2 DIA. "D" 4 Places
1/2 DIA. "D" 4 Places
LINE TIME LOAD FAN
1/2 DIA. "E" 2 Places
7 Spaces
5/16 DIA. "B" 40 Places
1/2 DIA. "F" 2 Places
CUT OUT FOR COUNTER
CUT OUT FOR COUNTER
FRONT
5/16 DIA. "F" 2 Places
5/16 DIA. "F" 2 Places
1/2 DIA. "C"
3/16 DIA. "G"
3/16 DIA. "G"
1/2 DIA. "J"
REAR
25
26
ALL DIMENSIONS IN INCHES
92CM-21985
"C" — FOR FUSE HOLDER
"D" — FOR PAMCOR LAMPS
"E" — FOR SWITCHES
"F" — FOR BINDING POSTS
"G" — FOR P.B. RELAYS
"B" — FOR BANANA JACKS
"J" — FOR LINE CORD

Fig. A1

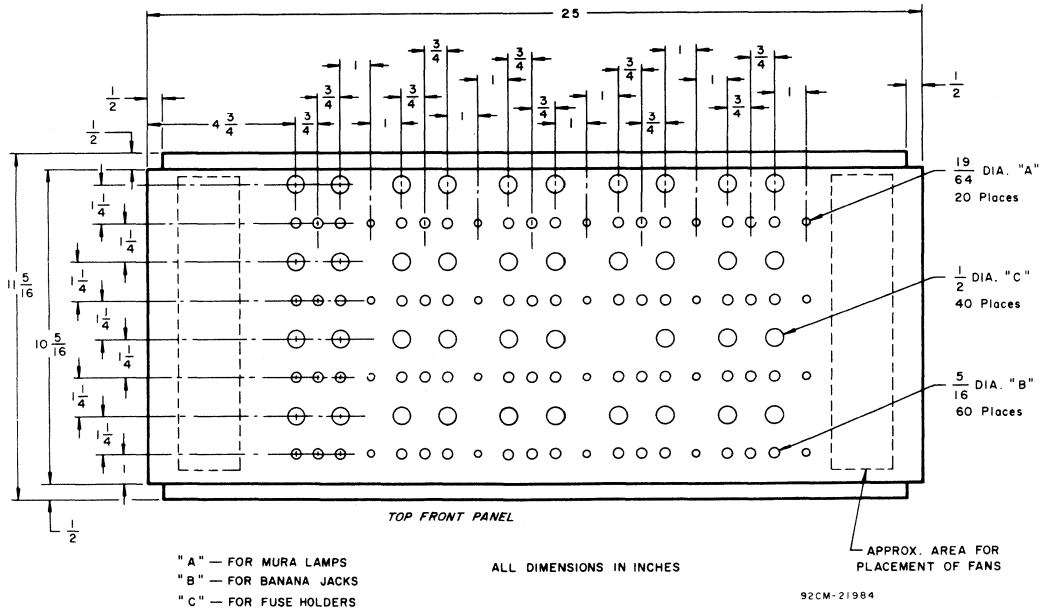

25
4 3/4
19/64 DIA. "A" 20 Places
1/2 DIA. "C" 40 Places
5/16 DIA. "B" 60 Places
TOP FRONT PANEL
APPROX. AREA FOR PLACEMENT OF FANS
"A" — FOR MURA LAMPS
"B" — FOR BANANA JACKS
"C" — FOR FUSE HOLDERS
ALL DIMENSIONS IN INCHES
92CM-21984

Fig. A2

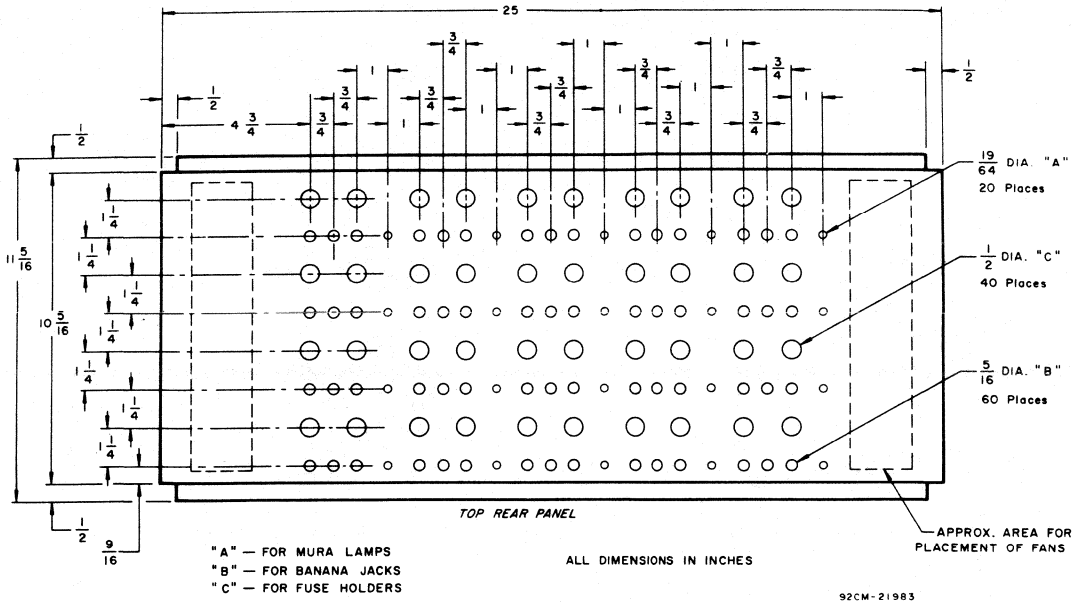

25
19/64 DIA. "A"
20 Places
1/2 DIA. "C"
40 Places
5/16 DIA. "B"
60 Places
TOP REAR PANEL
APPROX. AREA FOR
PLACEMENT OF FANS
"A" — FOR MURA LAMPS
"B" — FOR BANANA JACKS
"C" — FOR FUSE HOLDERS
ALL DIMENSIONS IN INCHES
92CM-21983

Fig. A3

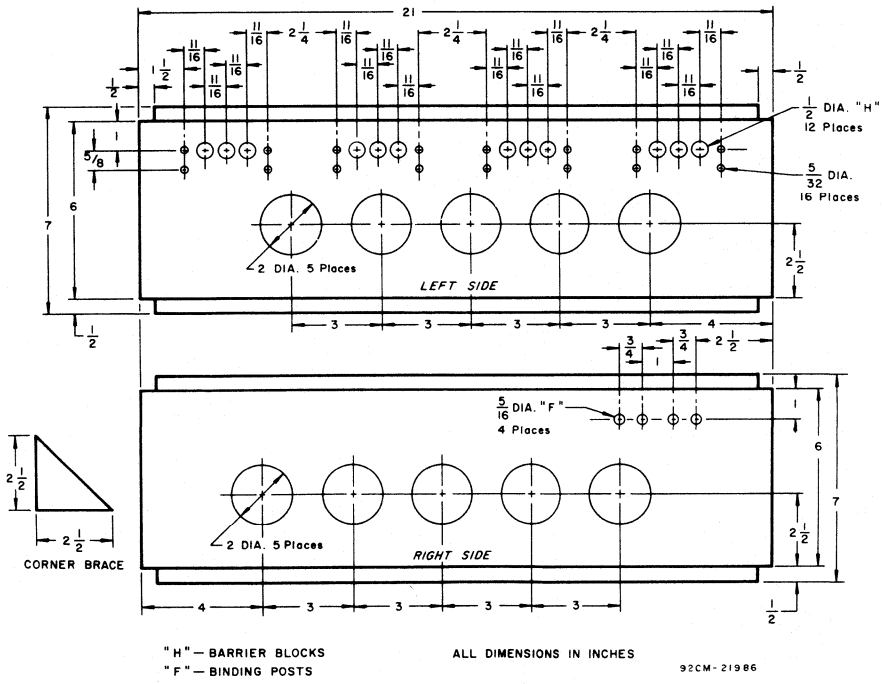
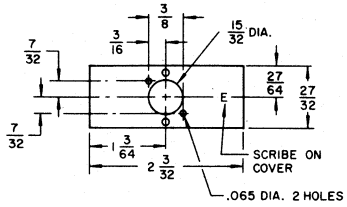
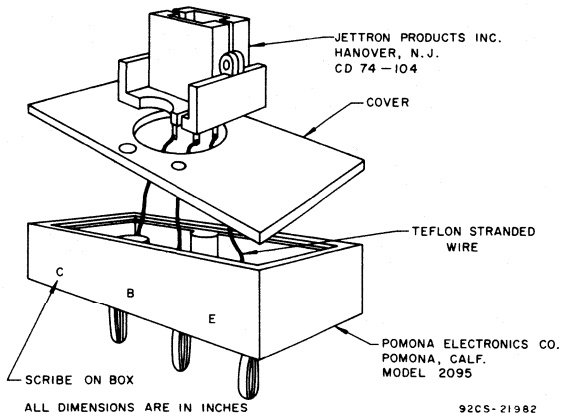

21
1/2 DIA. "H"
12 Places
5/32 DIA.
16 Places
2 DIA. 5 Places
LEFT SIDE
5/16 DIA. "F"
4 Places
2 DIA. 5 Places
RIGHT SIDE
CORNER BRACE
"H" — BARRIER BLOCKS
"F" — BINDING POSTS
ALL DIMENSIONS IN INCHES
92CM-21986

Fig. A4



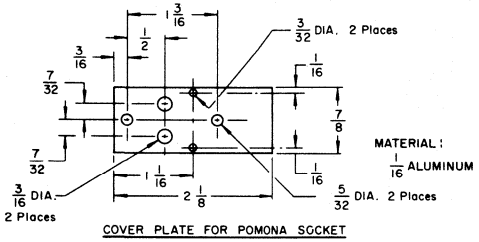
BLANK COVER SUPPLIED WITH POMONA BOX



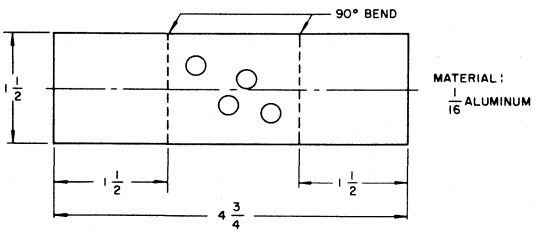
ALL DIMENSIONS ARE IN INCHES

92CS-21982

Fig. A5

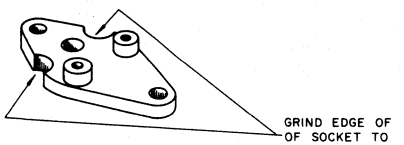


COVER PLATE FOR POMONA SOCKET



HOLE LAYOUT AS PER COMMERCIAL SOCKET NC-631-3-P
WAKEFIELD ENGINEERING — DELTA DIVISION

TO-3 — HEAT SINK

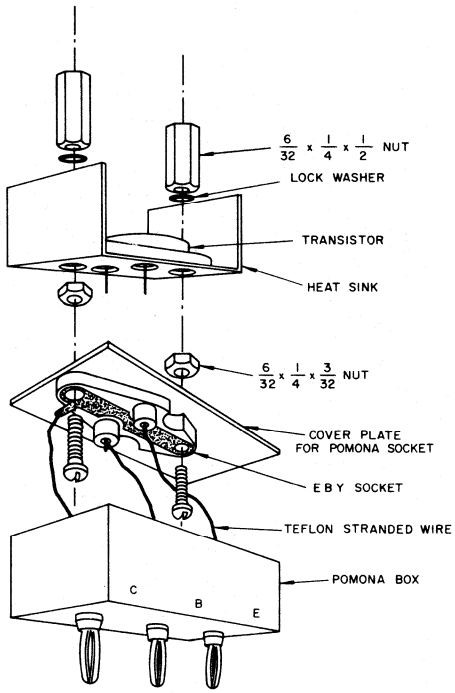


EBY SOCKET Nº. 9866-15-1

ALL DIMENSIONS ARE INCHES

92CS-21981

Fig. A6



92CS-21980

Fig. A7

High-Reliability RF Power Devices

High-Reliability RF Power Transistors

During the past several years, the RCA Solid State Division has conducted intensive programs to improve the quality and reliability of rf power transistors. The significant technological improvements that have resulted from these programs have advanced rf power transistors to the point that such devices are now used with confidence in numerous equipments in which high reliability is a prime requisite.

Design Features

The recent technological advances in RCA rf power transistors are extensions of the RCA overlay-transistor concept. Table 3-1 summarizes some of the major design features of RCA rf power transistors.

Overlay Transistor Structure—The RCA overlay design,* the basic type of structure used for RCA high-reliability rf power transistors, employs a unique emitter construction that makes possible exceptional power-frequency capabilities. The emitter is separated into many discrete sites that are connected in parallel to provide the increased current-handling capability required at high power levels. This type of emitter structure provides the high ratio of emitter periphery to base area that is essential to the generation of high power levels at high frequencies. In addition, the overlay construction makes possible current densities in the emitter mentallizing fingers that are significantly less than those in other high-frequency transistor structures. The adverse effect of high current density on transistor reliability, particularly with respect to failures caused by aluminum migration, is discussed subsequently.

The reduced emitter current density in overlay transistors can be attributed primarily to the relatively broad metal fingers used to interconnect the discrete emitter sites. These fingers are typically an order of magnitude wider than the ones used in interdigitated or mesh types of transistor structures. In addition, the separation between the emitter and base metallized fingers is 3 to 4 times greater than that in other types of high-frequency transistor structures. This increased separation permits the deposition of thicker metallizing layers and, therefore, results in a further reduction in current densities.

Emitter-Site Ballasting—A major technological development in the evolution of rf power transistors is a unique process in which an integral series resistor is introduced directly above each emitter site of an overlay transistor structure. RCA uses this process, which is referred to as emitter-site ballasting, to achieve rugged and reliable fine-line precise-geometry rf power transistors without sacrifice in high-frequency performance.

In overlay transistors, additional conducting and insulating layers can be readily introduced between the aluminum metallization and the shallow diffused emitter sites (shallow emitter diffusion is a requirement for good microwave performance). RCA has developed a technique in which a polycrystalline silicon layer (PSL) is interspersed between these regions. This interlayer, the resistivity of which can be accurately controlled by impurity doping, is used as the medium for the emitter-site ballasting of RCA microwave power transistors. Fig. 3-1 shows a cross-sectional diagram of an overlay transistor structure that includes the poloycrystalline silicon layer.

The resistivity of the polycrystalline silicon layer and the geometry of the contacting aluminum are controlled to form a ballast resistor in series with each emitter site. This ballasting has proved very effective in the reduction of hot spots, i.e., localized heated areas that result when the emitter-to-collector current is allowed to concentrate within small regions of the transistor pellet. Such current

* U.S. Patent No. 3,434,019, March 18, 1969

Table 3-1 — Design Features

Feature	Advantages
Overlay structure	Reduces current density Minimizes aluminum migration
Emitter-site ballasting	Reduces formation of isolated hot spots Improves safe operating area Improves transistor resistance to failure under high VSWR conditions
Polycrystalline silicon layer (PSL)	Minimizes "alloy spike" failures Minimizes dielectric failures
Glass-passivated aluminum metallizing	Minimizes aluminum migration
Hermetic package	Improves resistance to moisture Results in rugged mechanical construction Features low inductances and low parasitic capacitances Provided in both stripline and coaxial configurations

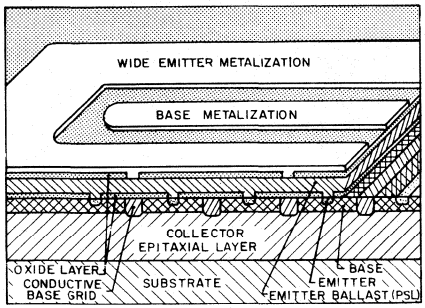


Fig. 3-1– Cross-section of an overlay transistor structure that contains the polycrystalline silicon layer (PSL).

concentrations may occur when a large number of transistor elements are interconnected electrically, but are not coupled thermally. The formation of such hot spots can result in a regenerative condition that leads to localized thermal runaway and the consequent destruction of the transistor.

The ballast resistors connected in series with each emitter site provide internal biasing control to prevent excessive current in any portion of the transistor. The formation of hot spots is thereby significantly reduced. Because the overlay construction results in an emitter that is segmented into many separate sites connected in parallel, each hot spot may be isolated and controlled so that the injection of charge carriers across the transistor chip is made more uniform.

The emitter-site ballasting results in a more uniform current distribution and, therefore, makes possible more effective utilization of emitter periphery. Consequently, transistor power-output and overdrive capabilities are increased, and the forward-bias safe-operating area (determined by infrared measurements) is enlarged. This latter factor is important for linear applications of high-frequency power transistors.

The formation of transistor hot spots under rf conditions increases as the output VSWR increases. Transistor failures caused by high VSWR conditions are often related to forward-bias second breakdown, which is characterized by extremely high localized currents. Emitter-site-ballasted transistors, therefore, have a substantially greater immunity to failure produced by high VSWR conditions such as those encountered in some broadband amplifiers. This immunity is particularly demonstrated by the RCA 2-GHz series of microwave power transistors. For example, the RCA-2N6265, 2N6266, RCA2003, and RCA2005 2-GHz transistors are characterized to withstand an infinite VSWR at rated power levels and the specified frequency. Higher-power types included in the 2-GHz series, such as the 2N6267 and the RCA2010, are characterized to withstand a VSWR of 10 to 1 at rated power levels and the specified frequency.

Polycrystalline Silicon Layer—In addition to its use as a medium for emitter-site ballasting, the polycrystalline silicon layer (PSL) also helps to minimize two other thermally induced failure modes that occur in high-frequency power transistors. As shown in Fig. 3-1, this layer forms a barrier between the aluminum metallization and the shallow diffused emitter region and, therefore, substantially reduces the possibility of "alloy spike" failures, i.e., emitter-to-base shorts caused by intermetallic formations of silicon and aluminum that may occur under severe hot-spot conditions.

The polycrystalline silicon layer also provides a barrier between the aluminum emitter finger and the silicon-dioxide insulating layer over the base. This barrier minimizes the possibility of emitter-to-base shorts caused by dielectric failures that result from an interaction between the aluminum and the silicon dioxide.

Recent reliability studies of high-frequency transistors operated under overstress conditions (i.e., at junction temperatures greater than 200°C) demonstrated an order of magnitude improvement in the mean time between failures for types that contain the polycrystalline silicon layer over that of similar types in which this layer is not used. These results verify that the PSL technique contributes substantially to over-all device reliability and therefore is an important feature in the construction of high-frequency power transistors.

Glass-Passivated Aluminum—In RCA rf power transistors, a silicon dioxide layer is deposited over the aluminum metallization. This deposition results in an increase of 40 per cent in the activation energy required for the initiation of aluminum migration. The mean time between failure of large crystalline aluminum passivated in this way is increased by approximately four times at a current density of 1×10^5 amperes/centimeter^2. The silicon dioxide layer also protects the aluminum from contamination and from damage that may result because of scratches or smears during device assembly.

RCA has recently concluded a study on electron-migration failure mechanisms in rf power transistors. The RCA-2N6267, a 10-watt, 2-GHz transistor that has the highest current density of any RCA microwave power type, was used as the test device in this study. The median time to failure (MTF) was determined for more than one-hundred 2N6267 transistors that were dc-biased to simulate high-current-density and high-junction-temperature operating conditions. The effects of hot-spot junction temperatures over the range from 230°C to 300°C, as determined from infrared scanning, and of current densities in the metallization of 1×10^5 amperes/centimeter^2 to 3×10^5 amperes/centimeter^2 were observed. On the basis of the results obtained, the MTF of the transistors at the typical operating current density of 1×10^5 amperes/centimeter and the typical operating junction temperature of 150°C was predicted to be 100 years. Even at an operating junction temperature equal to twice the typical value (i.e., at 2×10^5 amperes/centimeter^2), an MTF of 12 years is predicted for operation of the transistors at a junction temperature

of 150°C. These results indicate that, under normal conditions, migration failures should not be a factor for RCA rf power transistors.

Hermetic Transistor Packages—The package of a power transistor used in microwave applications becomes an integral circuit element that has a critical bearing on over-all circuit performance. A suitable package for a microwave power transistor should have good thermal properties and low parasitic reactances. Package parasitic reactances and resistive losses significantly affect circuit performance characteristics such as power gain, bandwidth, and stability. The most critical parasitics are the inductances of the emitter and base leads. The higher the power capabilities of the transistor, the lower the device impedances, particularly at the input. For high-power high-frequency transistors, the input impedance is determined primarily by the package, rather than by the transistor pellet. Consequently, such transistors should be encased in well-designed and well-constructed packages.

All RCA high-reliability of power transistors are supplied in metal-ceramic or laminated-ceramic packages. These packages, which are sealed with metallized ceramic interfaces, provide a true hermetic enclosure that can withstand thermal cycling from 65°C to + 200°C and power cycling such as may be encountered in transmitter service. In addition, these packages are mechanically rugged and are essentially impervious to moisture and other external contaminants.

Fig. 3-2 shows photographs of packages used for RCA high-reliability rf power transistors. These RCA hermetic transistor packages are specially designed to have extremely good thermal properties. For example, in the metal-ceramic packages, such as the HF-11, HF-21, and HF-28, the transistor pellet is mounted on a silver block or stud which is connected to the collector terminal. In the HF-46, a laminated-ceramic package, the pellet is mounted directly on a beryllium-oxide substrate. In each case, the initial heat spreader, i.e., the silver block or beryllium-oxide substrate, is a material that has a high thermal conductivity.

The RCA microwave-transistor packages, in addition to being mechanically rugged hermetic designs with excellent thermal properties, also have very low values of parasitic reactances and excellent isolation between input and output.

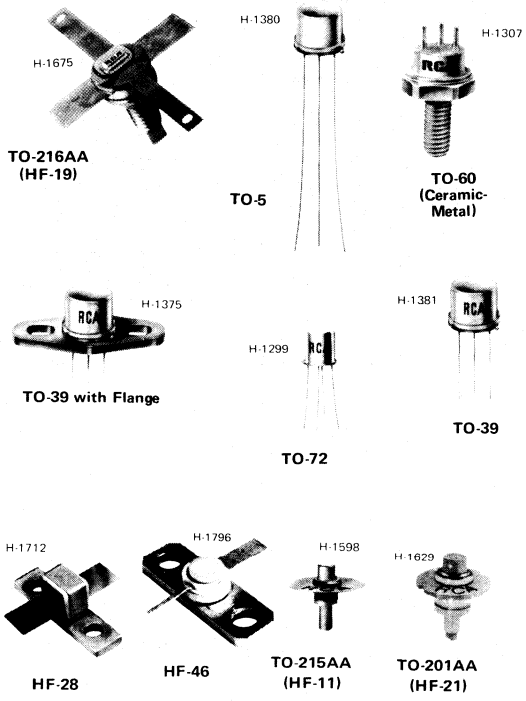


Fig. 3-2– Packages used for RCA high-reliability rf power transistors

Special Rating Concepts

Unlike low-frequency high-power transistors, many rf devices can fail within the dissipation limits set by the classical junction-to-case thermal resistance during operation under conditions of high load VSWR, high collector supply voltage, or linear (Class A or AB) operation. Failure can be caused by hotspotting, which results from local current concentration in the active areas of the device, and may appear as a long-term parameter degradation. Localized hotspotting can also lead to catastrophic thermal runaway.

The presence of hotspots can make virtually useless the present method of calculating junction temperature by measurements of average thermal resistance, case temperature, and power dissipation. However, by use of an infrared microscope, the spot temperature of a small portion of an rf transistor pellet can be determined accurately under actual or simulated device operating conditions. The resultant peak-temperature information is used to characterize the device thermally in terms of junction-to-case hotspot thermal resistance, $\theta_{S\text{-}C}$.

The use of hotspot thermal resistance improves the accuracy of junction temperature and related reliability predictions, particularly for devices involved in linear or mismatch service.

DC Safe Area—The safe area determined by infrared techniques represents the locus of all current and voltage combinations within the maximum ratings of a device that produce a specified spot temperature (usually 200°C) at a fixed case temperature. The shape of this safe area is very similar to the conventional safe area in that there are four regions, as shown in Fig. 3-3: constant

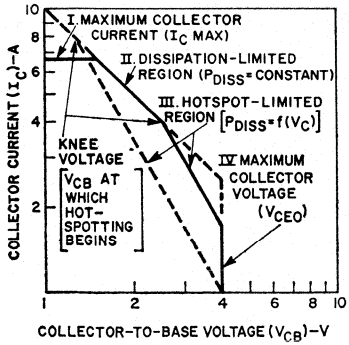


Figure 3-3. Safe-area curve for an rf power transistor determined by infrared techniques.

current, constant power, derating power, and constant voltage.

Regions I and IV, the constant-current and constant-voltage regions, respectively, are determined by the maximum collector current and V_{CEO} ratings of the device. Region II is dissipation-limited; in the classical safe area curve, this region is determined by the following relationship:

$$P_{max} = \frac{T_J(max) - T_C}{\theta_{J-C}}$$

where T_C is the case temperature.

This relationship holds true for the infrared safe area; P_{max} may be slightly lower because the reference temperature $T_{J(max)}$ is a peak value rather than an average value. The hotspot thermal resistance (θ_{JS-C}) may be calculated from the infrared safe area by use of the following definition:

$$\Theta_{JS-C} = \frac{T_{JS} - T_C}{P}$$

where T_{JS} is highest spot temperature [$T_{J(max)}$ for the safe area] and P is the dissipated power (= I × V product in Region II).

The collector voltage at which regions II and III intersect, called the knee voltage V_K, indicates the collector voltage at which power constriction and resulting hotspot formation begins. For voltage levels above V_K, the allowable power decreases. Region III is very similar to the second-breakdown region in the classical safe area curve except for magnitude. For many rf power transistors, the hotspot-limited region can be significantly lower than the second-breakdown locus. Generally V_K decreases as the size of the device is increased.

Fig. 3-4 shows the temperature profiles of two transistors with identical junction geometrics that operate at the same dc power level. If devices are operated on the dissipation-limited line of their classical safe areas, the profiles show that the temperature of the unballasted device rises to values 130°C in excess of the 200°C rating. Temperatures of this magnitude, although not necessarily destructive, seriously reduce the lifetime of the device.

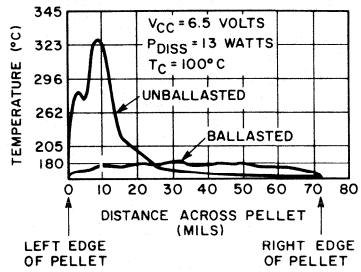


Figure 3-4. Thermal profiles of a ballasted and an unballasted power transistor during dc operation.

Effect of Emitter Ballasting—The profiles shown in Fig. 3-4 also demonstrate the effectiveness of emitter ballasting in the reduction of power (current) constriction. In the ballasted device, a biasing resistor is introduced in series with each emitter or small groups of emitters. If one region draws too much current, it will be biased towards cutoff, allowing a redistribution of current to other areas of the device.

The amount of ballasting affects the knee voltage, V_K, as shown in Fig. 3-5. A point of diminishing returns is reached as V_K approaches V_{CEO}.

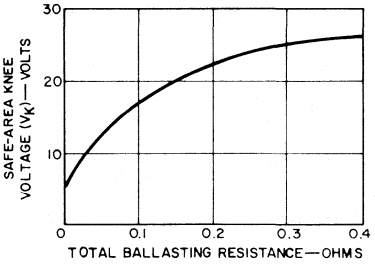


Figure 3-5. Safe-area voltage for an rf power transistor as a function of total ballasting resistance.

RF Operation—In normal class C rf operation, the hotspot thermal resistance is approximately equal to the classical average thermal resistance. If the proper collector loading (match) is maintained, θ_{JS-C} is independent of output power at values below the saturated- or slumping-power level, and is independent of collector supply voltage at values within + 30 per cent of the recommended operating level.

Power constriction in rf service normally occurs only for collector load VSWR's greater than 1.0. A transistor that has a mismatched load experiences temperatures far in excess of device ratings, as shown in Fig. 3-6(a) for VSWR = 3.0. For comparison, the temperature profile for the matched condition is shown in Fig. 3-6(b).

Fig. 3-7 is a typical family of thermal-resistance curves that indicate the response of a device to various

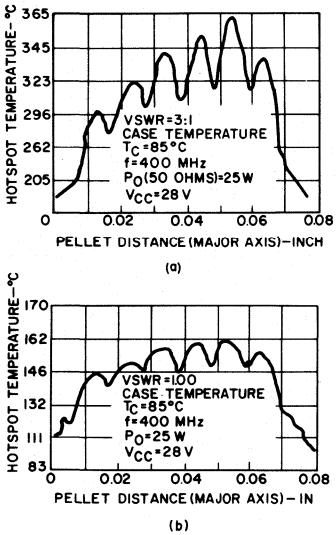


Figure 3-6. Thermal profile of a power transistor during rf operation: (a) under mismatched conditions; (b) under matched conditions.

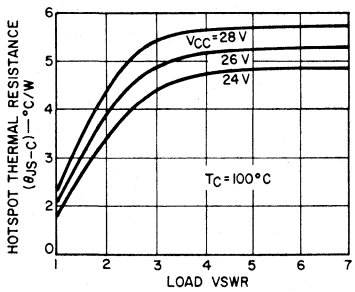


Figure 3-7. Mismatch-stress thermal characteristics for the 2N5071.

levels of VSWR and collector supply voltage. θ_{JS-C} responds to even slight increases in VSWR above 1.0 and saturates at a VSWR in the range of 3 to 6. The saturated level increases with increasing supply voltage. Devices with high knee voltages tend to show smaller changes of θ_{JS-C} with VSWR and supply voltage. θ_{JS-C} under mismatch is independent of frequency and power level, and reaches its highest values at load angles that produce maximum collector current. Power level does, however, influence the temperature rise and probability of failure.

Device failure can also occur at a load angle that produces minimum collector current. Under this condition, collector voltage swing is near its maximum, and an avalanche breakdown can result. This mechanism is sensitive to frequency and power level, and becomes predominant at lower frequencies because of the decreasing rf-breakdown capability of the device.

Collector mismatch can be caused by the following conditions:

1. Antenna loading changes in mobile applications when the vehicle passes near a metallic structure.
2. Antenna damage.
3. Transmission-line failure because of line, connector, or switch defects.
4. Variable loading caused by nonlinear input characteristics of a following transistor (particularly broadband) or varactor stage.
5. Supply-voltage changes that reflect different load-line requirements in class C.
6. Tolerance variations on fixed-tuned or stripline circuits.
7. Matching network variations in broadband service.

Case-Temperature Effects—The thermal resistance of both silicon and beryllium oxide, two materials that are commonly used in rf power transistors, increases about 70 per cent as the temperature increases from 25 to 200°C. Other package materials such as steel, kovar, copper, or silver, exhibit only minor increases in thermal resistance (about 5 per cent). The over-all increase in θ_{JS-C} of a device depends on the relative amounts of these materials used in the thermal path of the device; typically the increase of θ_{JS-C} ranges from 5 per cent to 70 per cent. Fig. 3-8 shows the rf and dc thermal resistance coeffi-

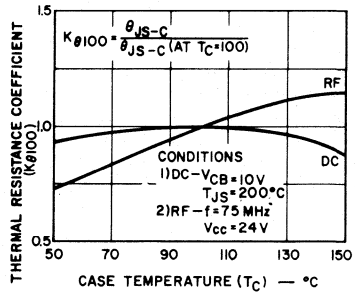


Figure 3-8. Thermal-resistance coefficient for the 2N5071.

cients for a typical rf transistor. For both cases, the coefficient is referenced to a 100°C case and is defined as follows:

$$K_{\theta 100} = \frac{\theta_{JS-C}}{\theta_{JS-C} \text{ at } T_C = 100°C}$$

The rf coefficient changes more than the dc coefficient, because of the power constriction that occurs in rf operation at elevated case temperature.

RF Avalanche Breakdown Voltage—The voltage breakdown mechanism is a time dependent phenomenon; and, therefore, breakdown voltages under pulsed and rf conditions are higher than the dc values. This is obviously true when the time during which the device is subject to fields of breakdown intensity is short with respect to the mechanism time constant and the off-time

is sufficiently long to permit the relaxation of this mechanism. Under these conditions, a catastrophic level cannot be reached during a single pulse, and the accumulative effect of several pulses is prevented by the off-time relaxation. Tests have demonstrated that a device that has a dc breakdown voltage (BV_{CBO}) of between 60 and 80 volts can often withstand about 135 volts (collector to base) under pulse lengths shorter than 0.25 microsecond. RF performance (particularly classes B and C) is analogous to pulsed operation in the sense that the instantaneous rf voltages are at their peak value for only a fraction of the cycle. (For example, at 1.3 GHz, the period of a cycle is 0.77 nanosecond and the voltage is peaked for less than ¼ cycle. Therefore, the high-intensity fields exist for less than 0.19 nanosecond.

The increased rf breakdown-voltage capability has been shown empirically. RF breakdown voltages approximately twice that at low frequencies have been achieved. One possible theoretical explanation is based on the following relationship between rf breakdown and current gain which in effect expresses the relationship at one operating frequency in terms of the alpha and beta cut-off frequencies of the device.

$$\frac{V_{CBO}^{(RF)}}{V_{CBO}} = \left\{\left[1 + \left(\frac{\omega}{\omega_\beta}\right)^2\right] \times \left[1 + 2M\left(\frac{\omega}{\omega_\beta}\right)^2\right]\right\}^{1/2n}$$

where M = "excess phase" factor, ω_β = beta cut-off frequency = ω_τ / β, η = empirical constant ranging from 2 to 10, and ω = operating frequency

In reality ω_O/ω_β is a relationship between the device transit times (i.e., time constants) and the operating frequency, for example:

$$\frac{\omega_o}{\omega_\beta} = \frac{2\pi fo}{\frac{1}{\tau_\beta}} = \frac{2\pi}{\frac{\tau_\beta}{\tau_o}}$$

where $\tau = \frac{1}{\omega_\beta}$ = beta transit time

and $\tau_o = \frac{1}{f_o}$ = period (time of one cycle)

The ratio $\omega/\omega\beta$, therefore, normalizes the time (duration) of voltage stress to the time of transit of the device.

The curve of this function is shown in Fig. 3-9. This curve indicates that a transistor operating at its cutoff frequency ω_t could theoretically have a breakdown voltage equal to six times the dc breakdown voltage. More typically, two to three times the dc breakdown voltage has been observed. A further increase in safety factor is obtained from the fact that the V_{CEsat} is greater under rf conditions because the instantaneous peak voltage is given by

$$\begin{aligned} V \text{ inst.} &= V_{CC} + (V_{RF} \text{ peak}) \\ &= V_{CC} + (V_{CC} - V_{CE}sat) \\ &= 2\,V_{CC} - V_{CE}sat \end{aligned}$$

$V_{CE}sat$ increases with operating frequency; the maximum instantaneous voltage, therefore, is lower at the higher frequencies further increasing the safety factor.

Both theoretical and empirical evidence support the contention that rf breakdown voltage can be considerably higher than BV_{CBO} (static). Therefore, reliable operation can be obtained even though V_{CC} is more than one-half BV_{CBO} (static).

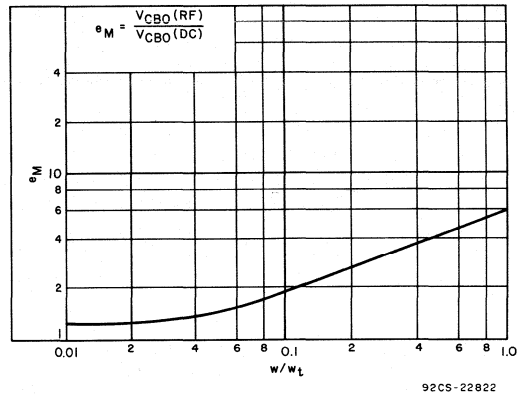


Fig. 3-9– Relationship of rf voltage breakdown to dc voltage breakdown as a function of frequency.

Reliability as a Function of Current Density and Junction Temperature

Questions are frequently asked concerning the life of rf power transistors that use an aluminum metallization system in connection with electromigration-related failure modes. Electromigration of the aluminum has been shown to occur in the presence of high current densities and elevated temperatures. This condition results from the mass transport of metal by momentum exchange between thermally activated metal ions and conducting electrons. As a consequence, the original uniform aluminum film is reconstructed to form thin conductor regions and extruded appearing hilocks.

The process can be accompanied by the solid-state dissolution of silicon in the aluminum. This latter effect usually occurs to a limited extent in transistor-manufacturing heat treatments until the aluminum-silicon saturation point is reached. As a result, only a very small additional amount of silicon dissolves during normal operation of the device. At high current densities and elevated temperatures, however, the electromigration process can act to transport the thermally diffused silicon ions away from the silicon-aluminum interface, and silicon diffusion into the aluminum is then allowed to continue until eventually failure of the transistor junctions occurs.

Test Conditions—The effects of electromigration on the lifetime of RCA rf power transistors in relation to various current densities and junction temperatures were evaluated in an accelerated-operating-life test program. DC current-voltage conditions were used because electromigration is responsive to the dc components of the total wave form used in rf applications, i.e., electromigration is effected by the unidirectional components of the field. Tests were conducted at three different emitter stripe current densities (J_E). The tests at each current density, in turn, were conducted at three different peak junction temperatures (T_j), all of which were accelerated above normal use conditions. Peak junction temperature was determined by infrared scanning of the transistor pellet at each life-test condition. Table 3-2 shows the matrix of test conditions. The sample size per test condition ranged from 10 to 15 units.

Test Vehicle—The RCA 2N6267 was used as the test vehicle because it is required to withstand one of the highest current of densities of any RCA rf power transistor (this transistor, therefore, represents a "worst-case" candidate). All the transistors used in the test were standard-product commercial devices, i.e., they were not subjected to conventional high-reliability screening prior to life testing.

Failure Mode—The accelerated test conditions produced failures that resulted from electromigration of aluminum and silicon. The failure indicator was degradation of the transistor junctions. RF power output measured at frequent life-test down periods prior to device junction failure exhibited only slight degradation (typically 8%); this degradation is extremely small in view of the severity of the test conditions.

Test Data—An Arrhenious plot (1/T-log scale) of the log-normal median time to failure (MTF) obtained from each test is shown in Fig. 3-10. The curves shown are extrapolated down from the data points in order to enable prediction of the MTF at operating junction temperatures below the maximum rated value of 200°C. An MTF of 9.5 x 10^5 hours (or greater than 100 years) is estimated for the 2N6267 test vehicle at its typical application current density of 8.5 x 10^4 A/cm² and junction temperature of 150°C.

Points from each curve in the Arrhenious plot were taken in the temperature range of 200°C to 100°C and replotted on a log-log scale, shown in Fig. 3-11, for extrapolation over various current densities. Fig. 3-11 represents general curves of MTF as a function of emitter current density and peak junction temperature. These curves can be used to estimate the MTF of an rf power transistor at its typical operating current density. Table 3-3 lists several RCA transistors designed to operate at microwave frequencies and shows the predicted MTF of

Table 3-2 Accelerated Life-Test Conditions

Collector Current (A)	Emitter Current (A)	Emitter Stripe Current Density (A/cm²)	Peak Junction Temperature in Degrees Centigrade* T_j1	T_j2	T_j3
1	1.02	8.5 x 10^4	300	280	154
2	2.07	1.7 x 10^5	283	258	230
3	3.22	2.7 x 10^5	300	273	240

* Represents peak temperature as averaged over several devices at each life-test condition. External heat-sink size is adjusted to achieve the differences in junction temperature on the life test.

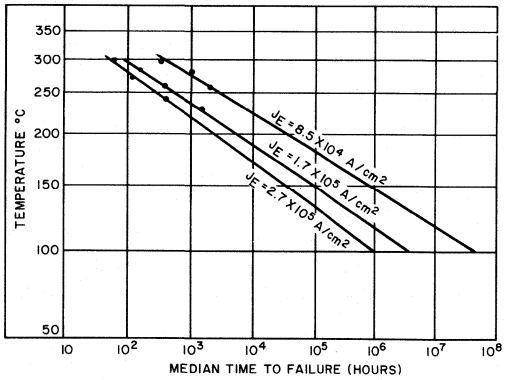


Fig. 3-10– Arrhenious plot showing extrapolation to lower temperatures from the life-test MTF points.

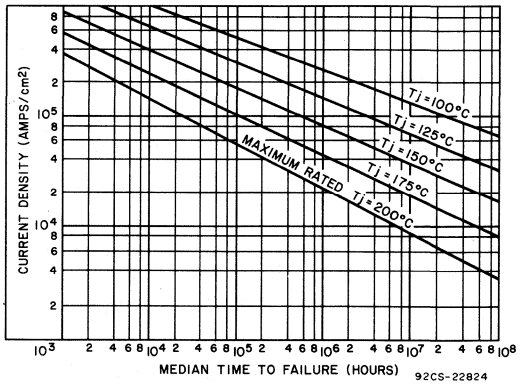


Fig. 3-11– MTF as a function of current density and junction temperature.

Table 3-3 — Estimated MTF for Glass-Passivated RF Power Transistors at Typical-Application Current Densities

Type	IE(Amps)	J_E (104A/CM²)	MTF (10^6 Hours) T_j=150°C
2N5470	0.119	5.2	4
2N5920	0.180	5.5	3.5
2N5921	0.450	3.5	12 x10^7
2N6265	0.215	6.5	2
2N6266	0.540	4.2	7
2N6267	1.10	8.5	.95
2N6268	0.275	8.3	1
2N6269	0.920	7.2	1.5
RCA2003	0.300	9	.8
RCA2005	0.540	4.2	7
RCA2010	1.10	8.5	.95
RCA3001	0.120	3.8	10
RCA3003	0.300	9	.8
RCA3005	0.540	8	1.1

these devices for typical application values of collector current, emitter stripe current density, and peak junction temperature. The microwave transistors are glass-passivated devices. It has been shown that the MTF of devices in which the glass passivation is not used is reduced by a factor of 10. Table 3-4 shows the MTF for non-glass-passivated rf devices predicted by use of this acceleration factor.

Table 3-4 — Estimated MTF for Non-Glass-Passivated Devices at Typical-Application Current Densities.

Type	Typical I_E (mA)	J_E (10^4 amps/cm²)	MTF T_j = 150°C (10^6 hours)
2N1493	25	2.5	3.5
2N2631	375	2.7	2.5
2N2857	1.5	0.72	15.0
2N2876	500	3.5	1.3
2N3118	50	5.1	0.4
2N3375	350	2.4	2.8
2N3553	150	1.0	12.0
2N3632	600	2.1	6.0
2N3866	70	3.8	1.0
2N5016	900	4.5	.6
2N5071	1300	3.7	1.2
2N5090	85	4.6	.58
2N5109	50	2.7	2.5
2N5916	120	5.7	0.3
2N5918	480	5.7	0.3
2N5919A	800	4.0	0.8
2N5994	2400	7.2	0.15
2N6093	5100	4.8	.5
2N6105	1350	4.4	.7
41024	100	5.4	.35

RCA JAN, JANTX, and JANTXV RF Power Transistors

RCA can supply a number of rf power transistors that have been qualified as JAN, JANTX, and/or JANTXV types in accordance with MIL-S-19500. These transistors, together with the MIL-S-19500 detailed electrical (slash-sheet) specifications for them, are listed below:

Basic Device Type No.	Electrical Specification No.*
2N918	MIL-S-19500/301
2N1493	MIL-S-19500/247
2N2857	MIL-S-19500/343
2N3375, 2N3553, 2N4440	MIL-S-19500/341
2N3866	MIL-S-19500/398
2N5071	MIL-S-19500/442
2N5109	MIL-S-19500/453
2N5918	MIL-S-19500/473

* MIL-S-19500 detailed electrical specifications for JAN, JANTX, and JANTXV devices can be obtained from the *Naval Publications and Forms Center,* 5801 Tabor Avenue, Philadelphia, Pa.

Maximum ratings and electrical characteristics for RCA JAN, JANTX, and JANTXV rf power transistors are included in the section *Technical Data on RCA RF Power Transistors.*

RCA HR-Series RF Power Transistors— Processing and Screening

RCA HR-series types are high-reliability rf and microwave power transistors intended for applications in aerospace, military, and industrial equipment. These transistors are supplied to three screening levels (/1, /2, /3) which meet the electrical mechanical, and environmental test, methods, and procedures established for power transistors in MIL-STD-750. Table 3-5 defines these reliability levels in terms of system-application usage.

RCA can provide on request SEM (Scanning Electron Microscope) inspection photographs to NASA-Goddard Specification GSFC-S-311-P-12A for each wafer lot tested to level /1. Precap Visual Inspection is conducted in conformance with Method 2072 of MIL-STD-750.

Table 3-5— Reliability Levels for RCA High-Reliability RF and Microwave Transistor

RCA Level	Application	Description
/1	Satellite and Aerospace	For devices intended for applications in which maintenance and replacement are extremely difficult or impossible, and Reliability is imperative.
/2	Military and Industrial (For example in Airborne Electronics)	For devices intended for applications in which maintenance and replacement can be performed, but are difficult and expensive.
/3	Military and Industrial (For example in Ground Based Electronics)	For devices intended for applications in which replacement can readily be accomplished.

HR-series transistors are available in RCA HF-28 and HF-46 and JEDEC TO-60, TO-201AA, TO-215AA, TO-216AA TO-5, TO-39, and TO-72 packages. The product-flow diagram shown in Fig. 3-12 lists a summary of processing, screening, tests, and sampling procedures followed in the manufacture of these transistors.

Table 3-6 provides detailed information for the screening tests included in the product-flow diagram. Table 3-7 gives pre-burn-in and post-burn-in electrical tests and delta limits for critical test parameters.

When ordering HR-series types, the appropriate reliability level should be indicated by addition of the suffix /1, /2, or /3 to the type number. For example, the 2N6265 processed to level /3 requirements should be marked HR2N6265/3.

The parameters listed in Table 3-7 are tested before and after burn-in, and the data are recorded for all devices in the lot. The parameters measured shall not have changed during burn-in from the initial value by more than the specified delta (Δ) limit or beyond the end-point limits given in Table 3-7.

All devices that exceed these limits are removed from the inspection lot, and the quality removed are noted in the lot history. If the quantity removed after burn-in exceeds 10 per cent of the devices subjected to burn-in, the entire lot is rejected.

RCA Premium- and Ultra-High-Reliability RF Power Transistors

RCA also supplies several transistors referred to as premium- or ultra-high-reliability types. Processing and screening requirements and ratings and electrical characteristics for these transistors are shown in the section *Technical Data on RCA High-Reliability RF Power Transistors*.

Table 3-6— Description of Total Lot Screening for HR-Series rf power transistors*

Test	Conditions	MIL-STD-750 or -202 Method	Cond.	Screening Levels● /1	/2	/3
Wafer Lot Identification	—	—	—	X	—	—
SEM Inspection	—	GSFC-S-311-P-12A■		S	—	—
Precap Visual	—	2072	—	X	X	—
Seal and Lot Identification	—	—	—	X	X	X
Stabilization Bake	24 hrs min at 200°C	—	—	X	X	X
Temperature Cycling	10 cycles	1051/107C	—	X	X	X
Centrifuge	20,000G, Y_1 direction	2006	—	X	X	X
Fine Leak	—	112	CIII	X	X	X
Gross Leak	—	112	A or B	X	X	X
HTRB (High-Temperature Reverse Bias)	80% V_{CB}, 150°C min	—	—	X	X	X
Serialize	—	—	—	X	X	X
Pre-Burn-in Electrical	See detail Specification			X	X	X
Burn-In				X	X	X
Post-Burn-in Electrical				X	X	X
Final Group A				X	X	X

* Data on specific HR-Series types given in following pages show test conditions and limits.
● × = 100% Testing; S = Sample of 5 (random selection from each wafer); – = not performed.
■ This specification, which was written by NASA Goddard Space Flight Center, is the industry standard.

Table 3-7— Burn-In Test Measurements

Test	MIL-STD-750 Method	Conditions & Limits	Symbol	Δ Limits
Collector cutoff current	3041	Per Detailed Electrical Specification	—	100% of pre-burn-in value or 10% of Group -A Limit whichever is greater
Forward-current transfer ratio	3076		h_{FE}	± 20% of pre-burn-in value
Power output	—		P_{out}	

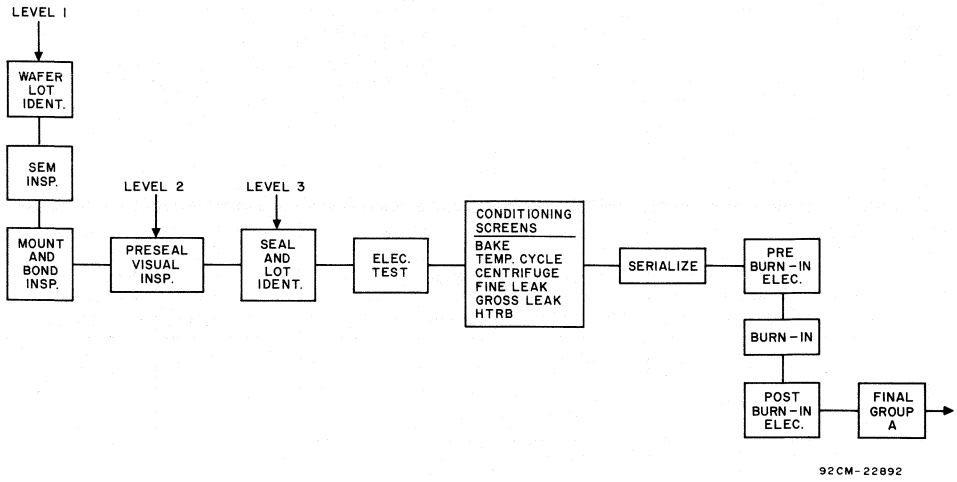


Fig. 3-12– Product Flow Diagram for RCA HR-Series rf power transistors (See Tables 3-6 and 3-7 for additional details)

JAN2N918 Silicon Epitaxial Planar VHF Transistor

JAN Electrical Specifications: MIL-S-19500/301A
Package: JEDEC TO-72

Maximum Ratings

P_T		V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_J	T_{stg}
$T_C = 25°C$ [1]	$T_A = 25°C$ [2]						
mW	mW	Vdc	Vdc	Vdc	mAdc	°C	°C
300	200	30	3	15	50	+200	-65 to +200

[1] Derate linearly 1.71 mW/°C for $T_C > 25°C$.
[2] Derate linearly 1.14 mW/°C for $T_A > 25°C$.

Primary Electrical Characteristics

Limits	h_{FE} I_C = 3 mAdc V_{CE} = 1 Vdc	h_{fe} I_C = 4 mAdc V_{CE} = 10 Vdc f = 100 MHz	$r_b' C_c$ I_E = -4.0 mAdc V_{CB} = 10 Vdc f = 79.8 MHz	C_{obo} V_{CB} = 10 Vdc I_E = 0 100 kHz ≤ f ≤ 1 MHz	NF V_{CE} = 6 Vdc I_C = 1 mAdc f = 60 MHz g_s = 2.5 mmho	G_{PE} V_{CB} = 12 Vdc I_C = 6.0 mAdc f = 200 MHz
			psec	pF	dB	dB
Min	20	6.0	–	–	–	15
Max	200	–	25	1.7	6.0	–

For characteristic curves and test conditions, refer to data on basic type in File No. 83.

JAN2N1493 Silicon N-P-N VHF Transistor

JAN Electrical Specification: MIL-S-19500/247
Package: JEDEC TO-39

Maximum Ratings

P_T [1]	V_{CBO}	V_{CEX}	V_{EBO}	$R_{\theta JC}$	T_J	T_{stg}
W	Vdc	Vdc	Vdc	°C/W	°C	°C
3.5	100	100	4.5	50	+200	-65 to +200

[1] This power-dissipation rating is for 1,000 hours expected life at $T_A = +25° \pm 3°C$.

Primary Electrical Characteristics

Limits	PG (at: f = 70 MHz V_{CC} = 50 Vdc I_C = 25 mAdc	h_{fe} f = 70 MHz V_{CC} = 20 Vdc I_C = 15 mAdc	h_{FE} V_{CE} = 20 Vdc I_E = 10 mAdc	C_{ob} f = 0.1 to 1.0 MHz V_{CB} = 20 Vdc I_E = 0	$r_b' C_c$ V_{CC} = 20 Vdc I_C = 10 mAdc
	dB	–	–	pF	psec
Min.	10	2.5	50	–	–
Max.	–	–	200	5.0	100

For characteristic curves and test conditions, refer to data on basic type in File No. 10.

JAN2N2857, JANTX2N2857

Silicon N-P-N Epitaxial Planar UHF Transistor

JAN Electrical Specifications: MIL-S-19500/343A
Service: For UHF
Package: JEDEC TO-72

Maximum Ratings

P_T[1] $T_A = 25°C$	P_T[2] $T_C = 25°C$	V_{CBO}	V_{CEO}	V_{EBO}	T_A	I_C
mW	mW	Vdc	Vdc	Vdc	°C	mAdc
200	300	30	15	3	-65 to +200	40

[1] Derate linearly 1.14 mW/°C for $T_A > 25°C$.
[2] Derate linearly 1.71 mW/°C for $T_C > 25°C$.

Primary Electrical Characteristics

Limits	h_{FE} $V_{CE} = 1$ Vdc $I_C = 3$ mAdc	$\|h_{fe}\|$ $V_{CE} = 6$ Vdc $I_C = 5$ mAdc $f = 100$ MHz	C_{cb} $V_{CB} = 10$ Vdc $I_E = 0$ 100 kHz $\leq f \leq$ 1 MHz	NF $V_{CE} = 6$ Vdc $I_C = 1.5$ mAdc $f = 450$ MHz $R_g = 50$ ohms	G_{PE} $V_{CE} = 6$ Vdc $I_C = 1.5$ mAdc $f = 450$ MHz	$r_b' C_c$ $V_{CB} = 6$ Vdc $I_E = 2$ mAdc $f = 31.9$ MHz
			pF	dB	dB	psec
Min	30	10	–	–	12.5	4
Max	150	19	1.0	4.5	21	15

For characteristic curves and test conditions, refer to data on basic type in File No. 61.

JAN2N3375, JANTX2N3375, JANTXV2N3375
JAN2N3553, JANTX2N3553, JANTXV2N3553
JAN2N4440, JANTX2N4440, JANTXV2N4440

Silicon N-P-N Overlay VHF-UHF Transistors

JAN Electrical Specifications: MIL-S-19500/341
Package: JEDEC TO-39-2N3553
JEDEC TO-60-2N3375, 2N4440

Maximum Ratings

Type	P_T T_A= 25°C	P_T T_C = 25°C	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_{stg}	T_J
	W	W	Vdc	Vdc	Vdc	Adc	°C	°C
2N3375, 2N4440	2.6[1]	11.6[3]	65	40	4	1.5	-65 to +200	+200
2N3553	1.0[2]	7.0[4]	65	40	4	1.0	-65 to +200	+200

[1] Derating linearly at 14.86 mW/°C for $T_A > 25°C$.
[2] Derate linearly at 5.71 mW/°C for $T_A > 25°C$.
[3] Derate linearly at 0.066 W/°C for $T_C > 25°C$.
[4] Derate linearly at 0.04 W/°C for $T_C > 25°C$.

Primary Electrical Characteristics

Limits	$V_{CE}(sat)$[1] I_C = 500 mAdc, I_B = 100 mAdc; 2N3375, 2N4440	$V_{CE}(sat)$[1] I_C = 250 mAdc, I_B = 50 mAdc; 2N3553	C_{obo} I_E = 0, V_{CB} = 30 Vdc, 100 kHz ≤ f ≤ 1 MHz	$\|h_{fe}\|$ V_{CE} = 28 Vdc, I_C = 125 mAdc, f = 100 MHz	h_{FE} V_{CE} = 5 Vdc[1], I_C = 150 mAdc
	Vdc	Vdc	pF		
Min	–	–	–	3.5	15
Max	0.7	0.6	10	–	150

Limits	P_{OE} P_{IE} = 1.0 W, f = 100 MHz; 2N3375	P_{OE} P_{IE} = 1.0 W, f = 400 MHz; 2N3375	P_{OE} P_{IE} = 0.25 W, f = 175 MHz; 2N3553	P_{OE} P_{IE} = 1.0 W, f = 100 MHz; 2N4400	P_{OE} P_{IE} = 1.0 W, f = 400 MHz; 2N4400
	W	W	W	W	W
Min	7.5	3.0	2.5	10	4.0
Max	14	6.0	5.0	16	8.0

[1] Pulsed test

For characteristic curves and test conditions, refer to data on basic type in File No. 386.

JAN2N3866, JANTX2N3866

Silicon N-P-N Overlay VHF-UHF Transistors

JAN Electrical Specification: MIL-S-19500/398
Package: JEDEC TO-39

Maximum Ratings

P_T[1] / T_A = 25°C	V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_{stg}	T_J
W	Vdc	Vdc	Vdc	Adc	°C	°C
1.0	60	3.5	30	0.4	-65 to +200	+200

[1] Derate linearly at 5.71 mW/°C for $T_A > 25°C$.

Primary Electrical Characteristics

Limits	h_{FE} V_{CE} = 5.0 Vdc I_C = 50 mAdc	$\|h_{fe}\|$ V_{CE} = 15 Vdc I_C = 50 mAdc f = 200 MHz	C_{obo} V_{CB} = 28 Vdc I_E = 0 100 kHz ≤ f ≤ 1 MHz	$V_{CE(sat)}$ I_C = 100 mAdc I_B = 10 mAdc	P_{OE} V_{CC} = 28 Vdc P_{IE} = 0.15 W f = 400 MHz	P_{OE} V_{CC} = 28 Vdc P_{IE} = 0.075 W f = 400 MHz
			pF	Vdc	W	W
Min	15	2.5	–	–	1.0	0.5
Max	200	8.0	3.0	1.0	2.0	–

For characteristic curves and test conditions, refer to data on basic type in File No. 80.

JAN2N5071, JANTX2N5071

Silicon N-P-N Emitter-Ballasted Overlay VHF Transistor

JAN Electrical Specification: MIL-S-19500/442
Package: JEDEC TO-60

Maximum Ratings

P_T[1] / T_A = 25°C	P_T[2] / T_C = 25°C	V_{CEO}	V_{EBO}	V_{CEX}	I_C	$T_{Oper.}$ & $T_{stg.}$
W	W	Vdc	Vdc	Vdc	Adc	°C
2.6	70	35	4	65	10	-65 to +200

[1] Derate linearly at 15 mW/°C for $T_A > 25°C$ [2] Derate linearly at 400 mW/°C for $T_C > 25°C$

Primary Electrical Characteristics

Limits	h_{FE} V_{CE} = 5 Vdc I_C = 3 Adc	C_{obo} V_{CB} = 30 Vdc I_E = 0 100kHz ≤ f ≤ 1MHz	P_{OE} P_{IE} = 3 W f = 76 MHz	VSWR f = 30 MHz P_{OE} = 30 W	$R_{\theta JC}$
		pF	W		°C/W
Min.	15		24		
Max.	100	85	34	3:1 All Phases	2.5

For characteristic curves and test conditions, refer to data on basic type in File No. 269.

JAN2N5109, JANTX2N5109

Silicon N-P-N Overlay VHF-UHF Transistors

JAN Electrical Specification: MIL-S-19500/453
Package: JEDEC TO-39

Maximum Ratings

P_T[1] $T_A = 25°C$	V_{CBO}	V_{EBO}	V_{CEO}	V_{CER}	I_C	T_{stg}	T_J
W	Vdc	Vdc	Vdc	Vdc	Adc	°C	°C
1.0	40	3.0	20	40	0.4	-65 to +200	+200

[1] Derate linearly 5.71 mW/°C for $T_A > 25°C$.

Primary Electrical Characteristics

Limits	h_{FE} $V_{CE} = 15$ Vdc $I_C = 50$ mAdc	$\|h_{fe}\|$ $V_{CE} = 15$ Vdc $I_C = 50$ mAdc f = 200 MHz	C_{obo} $V_{CB} = 28$ Vdc $I_E = 0$ 100 kHz ≤ f ≤ 1 MHz	$V_{CE(sat)}$ $I_C = 100$ mAdc $I_B = 10$ mAdc	G_{Pe} $V_{CE} = 15$ Vdc $P_{IE} = 10$ dBM $I_C = 10$ mAdc f = 200 MHz
			pF	Vdc	dB
Min	40	6.0	–	–	11.0
Max	120	9.0	3.5	0.5	–

For characteristic curves and test conditions, refer to data on basic type in File No. 281.

JAN2N5918-

Silicon N-P-N Emitter-Ballasted VHF-UHF Transistor

JAN Electrical Specification: MIL-S-19500/473
Package: JEDEC TO-216AA

Maximum Ratings

P_T[1] $T_A = 25°C$	P_T[2] $T_C = 75°C$	V_{CEO}	V_{EBO}	V_{CEX}	I_C	T_J
W	W	Vdc	Vdc	Vdc	Adc	°C
2.4	10	30	4	60	0.75	-65 to +200

[1] Derate linearly 13.7 mW/°C for $T_A > 25°C$
[2] Derate linearly 80 mW/°C for $T_C > 75°C$

Primary Electrical Characteristics

Limits	$V_{CE(sat)}$ $I_C = 2$ Adc $I_B = 400$ mAdc	h_{FE} $V_{CE} = 4$ Vdc $I_C = 0.5$ Adc	C_{obo} $V_{CB} = 30$ Vdc $I_E = 0$ 100 kHz ≤ f ≤ 1 MHz	P_{OE} $P_{IE} = 1.59$ W f = 400 MHz
	Vdc		pF	W
Min	–	15	–	10
Max	–	200	13	13

For characteristic curves and test conditions, refer to data on basic type in File No. 448.

JEDEC TO-72 H-1299

Silicon N-P-N Epitaxial Planar Transistor

For UHF Applications in Industrial and Military Equipment

Features:

- **High gain-bandwidth product — f_T = 1000 MHz min.**
- **High converter (450-to-30-MHz) gain — G_c = 15 dB typ. for circuit bandwidth of approximately 2 MHz**
- **High power gain as neutralized amplifier — G_{pe} = 12.5 dB min. at 450 MHz for circuit bandwidth of 20 MHz**
- **High power output as uhf oscillator — P_o = 30 mW min., 40 mW typ. at 500 MHz; 20 mW typ., at 1 GHz**
- **Low device noise figure — NF = 4.5 dB max. as 450 MHz amplifier; 7.5 dB typ. as 450-to-30-MHz converter**
- **Low collector-to-base time constant — $r_b' C_c$ = 7 ps typ.**
- **Low collector-to-base feedback capacitance — C_{cb} = 0.6 pF typ.**

The RCA-HR2N2857 is a high-reliability version of the RCA-2N2857. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N2857 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N2857 transistor in RCA data bulletin file No. 61.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	30	V
COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	15	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	2.5	V
COLLECTOR CURRENT	I_C	40	mA
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 25° C		300	mW
At case temperatures above 25° C		Derate at 1.72	mW/°C
At ambient temperatures up to 25° C		200	mW
At ambient temperatures above 25° C		Derate at 1.14	mW/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. from seating surface for 10 s max.		265	°C

II. GROUP A TESTS, *at Ambient Temperature (T_A) = 25° C*

	CHARACTERISTIC	Symbol	TEST CONDITIONS							LIMITS		Units
			Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Emitter-to-Base Voltage V_{EB}	DC Emitter Current I_E	DC Base Current I_B	DC Collector Current I_C			
			MHz	V	V	V	mA	mA	mA	Min.	Max.	
*	Collector Cutoff Current	I_{CBO}		15			0			–	10	nA
	Collector-to-Base Breakdown Voltage	BV_{CBO}					0		0.001	30	–	V
	Collector-to-Emitter Breakdown Voltage	BV_{CEO}						0	3	15	–	V
	Emitter-to-Base Breakdown Voltage	BV_{EBO}					–0.01		0	2.5	–	V
*	Static Forward Current Transfer Ratio	h_{FE}			1				3	30	150	
	Small-Signal Forward Current Transfer Ratio	h_{fe}	0.001[c] 100[c]		6 6				2 5	50 10	220 19	
	Collector-to-Base Feedback Capacitance	C_{cb}	0.1 to 1[b]	10			0			–	1.0	pF
	Collector-to-Base Time Constant	$r_b' C_c$	31.9[c]	6			–2			4	15	ps
	Small-Signal Common-Emitter Power Gain in Neutralized Amplifier Circuit	G_{pe}	450[c]		6				1.5	12.5	19	dB
	Power Output as Oscillator	P_o	⩾500[a]	10			–12			30	–	mW
	UHF Device Noise Figure	NF	450[c, d, f]		6				1.5	–	4.5	dB
	UHF Measured Noise Figure	NF	450[c, d]		6				1.5	–	5.0	dB

[a] Fourth lead (case) not connected.

[b] Three-terminal measurement: Lead No. 1 (Emitter) and lead No. 4 (Case) connected to guard terminal.

[c] Fourth lead (case) grounded.

[d] Generator resistance R_g = 50 ohms.

[e] Generator resistance R_g = 400 ohms.

[f] Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test circuit (0.25 dB) and the contribution of the following stages in the test setup (0.25 dB).

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

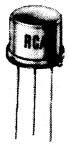
V_{CB} = 15 V

P_T = 0.2 W

RCA
Solid State
Division

RF Power Transistors

HR2N3866



JEDEC TO-39 H-1381

Silicon N-P-N Overlay Transistor

High-Gain Driver for VHF/UHF Applications
in Military and Industrial Communications Equipment

Features:

- **High power gain, unneutralized Class C amplifier**
  - **1-W output at 400 MHz (10-dB gain)**
  - **1-W output at 250 MHz (15-dB gain)**
  - **1-W output at 175 MHz (17-dB gain)**
  - **1-W output at 100 MHz (20-dB gain)**
- **Low output capacitance**
  C_{obo} = 3 pF max.

The RCA-HR2N3866 is a high-reliability version of the RCA-2N3866. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N3866 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N3866 transistor in RCA data bulletin file No. 80.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	55	V
With base open	V_{CEO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.4	A
CONTINUOUS BASE CURRENT	I_B	0.4	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 25° C		5	W
At case temperatures above 25° C		Derate at 0.0286	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE:			
At distances ≥ 1/16 in. (1.58 mm) from seating plane for 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC VOLTAGE (V)		DC CURRENT (mA)					
			V_{CE}	V_{EB}	I_E	I_B	I_C	MIN.	MAX.	
	Collector Cutoff Current: Base-emitter junction reverse biased	I_{CEX}	55	1.5				–	0.1	mA
*	Base open	I_{CEO}	28			0		–	20	μA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	55	–	V
	Collector-to-Emitter Breakdown Voltage: With base open	$V_{(BR)CEO}$				0	5	30	–	V
	With base connected to emitter through 10-ohm resistor	$V_{(BR)CER}$		0			5	55	–	
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Emitter-Cutoff Current	I_{EBO}		3.5				–	0.1	mA
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				20	100	–	1.0	V
*	DC Forward-Current Transfer Ratio	h_{FE}	5				50	10	200	
	Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						–	35	°C/W

DYNAMIC

TEST AND CONDITIONS	SYMBOL	FREQUENCY MHz	LIMITS		UNITS
			MIN.	MAX.	
Power Output (V_{CC} = 28 V): P_{IE} = 0.1 W	P_{OE}	400	1.0	–	W
Large-Signal Common-Emitter Power Gain (V_{CC} = 28 V): P_{IE} = 0.1 W	G_{PE}	400	10	–	dB
Collector Efficiency (V_{CC} = 28 V): P_{IE} = 0.1 W, P_{OE} = 1 W, Source Impedance = 50 Ω	η_C	400	45	–	%
Magnitude of Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio: I_C = 50 mA, V_{CE} = 15 V	$\lvert h_{fe} \rvert$	200	2.5	–	
Available Amplifier Signal Input Power, P_{OE} = 1 W, Source Impedance = 50 Ω	P_i	400	–	0.1	W
Common-Base Output Capacitance (V_{CB} = 28 V)	C_{obo}	1	–	3	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C
V_{CB} = 28 V
P_T = 1 W

JEDEC TO-60 H-1307

High-Power Silicon N-P-N Overlay Transistor

High-Gain Type for Class A, B, or C Operation in VHF/UHF Circuits

Features:

- **Maximum safe-area-of-operation curve**
- **1.2-W (min.) output at 400 MHz (7.8-dB gain)**
- **1.6-W (typ.) output at 175 MHz (12-dB gain)**
- **Hermetic stud-type package**
- **All electrodes isolated from stud**

The RCA-HR2N5090 is a high-reliability version of the RCA-2N5090. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5090 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5090 transistor in RCA data bulletin file No. 270.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	55	V
With base open	V_{CEO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.4	A
CONTINUOUS BASE CURRENT	I_B	0.4	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 100° C		4	W
At case temperatures above 100° C		Derate linearly at 0.04	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During Soldering):			
At distances ≥ 1/16 in. (1.58 mm) from insulating wafer for 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC COLLECTOR VOLTAGE V	DC BASE VOLTAGE V	DC CURRENT mA					
			V_{CE}	V_{BE}	I_E	I_B	I_C	MIN.	MAX.	
*	Collector Cutoff Current: With base open	I_{CEO}	28			0		–	0.02	mA
	With base-emitter junction reverse-biased	I_{CEV}	55	–1.5				–	0.1	
	Emitter Cutoff Current	I_{EBO}		3.5			0	–	0.1	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	55	–	V
	Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO(sus)}$				0	5	30	–	V
	With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER(sus)}$					5	55[a]	–	
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				20	100	–	1.0	V
*	DC Forward-Current Transfer Ratio	h_{FE}	5				50	10	200	
	Thermal Resistance (Junction-to-Case)	$R\theta_{JC}$						–	25	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		DC COLLECTOR VOLTAGE V	OUTPUT POWER (P_{OE}) W	INPUT POWER (P_{IE}) W	COLLECTOR CURRENT (I_C) mA	FREQUENCY (f) MHz	MIN.	MAX.	
Power Output (Class C amplifier, unneutralized)	P_{OE}	V_{CC} = 28		0.2		400	1.2	–	W
Gain-Bandwidth Product	f_T	V_{CE} = 15			50		500	–	MHz
Magnitude of Common Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio	$\|h_{fe}\|$	V_{CE} = 15			50		2.5	–	
Available Amplifier Signal Input Power	P_i		1.2			400	–	0.2	W
Collector Efficiency	η_C		1.2				45	–	%
Collector-to-Base Capacitance	C_{obo}	V_{CB} = 30				1	–	3.5	pF

[a] Pulse through a 25-mH inductor; duty factor = 0.05.

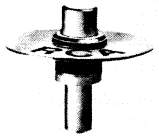
* Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

V_{CB} = 28 V

P_T = 1.75 W



JEDEC TO-215AA Package H-1598

Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers,
Microwave Fundamental-Frequency Oscillators,
and Frequency Multipliers

Features:

- **1-W output with 5-dB gain (min.) at 2 GHz**
- **2-W output with 10-dB gain (typ) at 1 GHz**
- **Ceramic-metal hermetic package with low inductance and low parasitic capacitances**

The RCA-HR2N5470 is a high-reliability version of the RCA-2N5470. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5470 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5470 transistor in RCA data bulletin file No. 350.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	55	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
PEAK COLLECTOR CURRENT		0.4	A
CONTINUOUS COLLECTOR CURRENT	I_C	0.2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25° C		3.5	W
At case temperatures above 25° C		Derate at 0.02	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector Voltage (V)		DC Current (mA)					
			V_{CB}	V_{CE}	I_E	I_B	I_C	Min.	Max.	
*	Collector Cutoff Current	I_{CES}		50				–	1	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	55	–	V
	Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER(sus)}$					5	55	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				10	100	–	1.0	V
	Collector-to-Base Capacitance (Measured at 1 MHz)	C_{cb}	30		0			–	3.0	pF
	RF Power Output (Common-Base Amplifier): At 2 GHz[a]	P_{OB}	28					1.0	–	W
*	Forward Current Transfer Ratio	h_{FE}		5			50	30	150	

[a] For P_{IB} = 0.316 W; minimum efficiency = 30%.

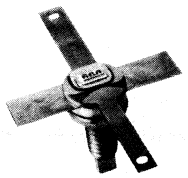
*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

V_{CB} = 15 V

P_T = 1 W



JEDEC TO-216AA Package H-1675

High-Gain Silicon N-P-N Overlay Transistor

For VHF/UHF Communications Equipment

Features:

- **Radial leads for microstripline circuits**
- **2-W (min.) output at 400 MHz (10-dB gain)**
- **2-W (typ.) output at 1 GHz (5-dB gain)**
- **Low-inductance, ceramic-metal hermetic package**
- **All electrodes isolated from stud**

The RCA-HR2N5916 is a high-reliability version of the RCA-2N5916. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5916 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5916 transistor in RCA data bulletin file No. 425.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	24	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 100° C		4	W
At case temperatures above 100° C		Derate linearly at 0.04	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector Voltage	DC Base Voltage	DC Current mA					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector-to-Emitter Cutoff Current: Base-emitter junction shorted	I_{CES}	30	0				–	1	mA
	Collector-to-Emitter Breakdown Voltage:	$V_{(BR)CES}$		0			5[a]	55	–	V
	With base open	$V_{(BR)CEO}$					5[a]	24	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				10	100	–	0.5	V
*	Forward Current Transfer Ratio	h_{FE}	5				50	30	150	
	Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$						–	25	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
		DC Collector Supply (V_{CC}) – V	Output Power (P_{OE}) – W	Input Power (P_{IE}) – W	Frequency (f) – MHz	Min.	Max.	
Power Output	P_{OE}	28		0.2	400	2.0	–	W
Power Gain	G_{PE}	28	2		400	10	–	dB
Collector Efficiency	η_C	28		0.2	400	50	–	%
Collector-Base Capacitance	C_{cb}	30 (V_{CB})			1	–	4.5	pF

[a] Pulsed through a 25-mH inductor; duty factor = 50%

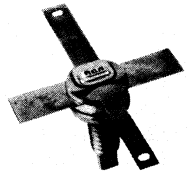
*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

V_{CB} = 16 V

P_T = 1.3 W



JEDEC TO-216AA Package H1675

10-W, 400-MHz High-Gain Silicon N-P-N Emitter-Ballasted Overlay Transistor

For VHF/UHF Communications Equipment

Features:

- **10-W output at 400 MHz (8-dB min. gain)**
- **Emitter-ballasting resistors**
- **Broadband performance (225–400 MHz)**
- **Low-inductance ceramic-metal hermetic package**
- **All electrodes isolated from stud**
- **Radial leads for stripline circuits**

The RCA-HR2N5918 is a high-reliability version of the RCA-2N5918. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5918 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5918 transistor in RCA data bulletin file No. 448.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	30	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.75	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 75° C		10	W
At case temperatures above 75° C		Derate linearly at 0.08	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector Voltage	DC Base Voltage	DC Current mA					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector-to-Emitter Cutoff Current: Base-emitter junction shorted	I_{CES}	30	0				–	5	mA
	Collector-to-Emitter Breakdown Voltage:	$V_{(BR)CES}$		0			100[a]	60	–	V
	With base open	$V_{(BR)CEO}$					100[a]	30	–	
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			1		0	4	–	V
*	Forward Current Transfer Ratio	h_{FE}	4				500	10	200	
	Thermal Resistance, (Junction to Case)	$R_{\theta JC}$						–	12.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
		DC Collector Supply (V_{CC}) – V	Output Power (P_{OE}) – W	Input Power (P_{IE}) – W	Frequency (f) – MHz	Min.	Max.	
Power Output	P_{OE}	28		1.59	400	10	–	W
Power Gain	G_{PE}	28	10		400	8	–	dB
Collector Efficiency	η_C	28	10		400	60	–	%
Collector-to-Base Output Capacitance	C_{obo}	30 (V_{CB})			1	–	13	pF

[a]Pulsed through a 25-mH inductor; duty factor = 50%.

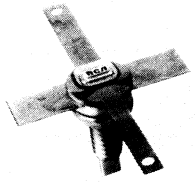
*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

V_{CB} = 28 V

P_T = 2.4 W



JEDEC TO-216AA H-1693

16-W, 400-MHz, Silicon N-P-N Emitter-Ballasted Overlay Transistor

Overdrive Capability of 20 W Output

Features:

- **6-dB gain (min.) at 400 MHz with 16-W (min.) output**
- **Integral emitter-ballasting resistors**
- **Broadband performance (225–400 MHz)**
- **Low-inductance ceramic-metal hermetic package**
- **Radial leads for microstripline circuits**
- **All electrodes isolated from the stud**

The RCA-HR2N5919A is a high-reliability version of the RCA-2N5919A. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5919A are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5919A transistor in RCA data bulletin file No. 505.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	30	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	4.5	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 75° C		25	W
At case temperatures above 75° C		Derate at 0.2	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector Voltage-V	DC Base Voltage-V	DC Current mA					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector-to-Emitter Cutoff Current: With base connected to emitter	I_{CES}	30	0				–	10	mA
	Collector-to-Emitter Breakdown Voltage: With base connected to emitter	$V_{(BR)CES}$		0			200[a]	65	–	V
	With base open	$V_{(BR)CEO}$				0	200[a]	30	–	
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			5		0	4	–	V
*	Forward Current Transfer Ratio	h_{FE}	4				500	10	200	
	Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						–	5.0	°C/W

[a]Pulsed through a 25-mH inductor; duty factor = 50%

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
		DC Collector Supply (V_{CC})-V	Input Power (P_{IE})-W	Output Power (P_{OE})-W	Frequency (f) MHz	Min.	Max.	
Output Power	P_{OE}	28	4.0		400	16	–	W
Overdrive Objective Test		28	7.0		400	20	–	
Power Gain	G_{PE}	28		16	400	6	–	dB
Collector Efficiency	η_C	28	4.0		400	65	–	%
Collector-to-Base Output Capacitance	C_{obo}	30 (V_{CB})			1	–	22	pF

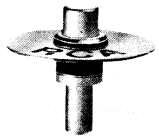
*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

V_{CB} = 28 V

P_T = 2.6 W



JEDEC TO-215AA H-1598

2-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **2-W output with 10-dB gain (min.) at 2 GHz**
- **3-W output with 12-dB gain (typ.) at 1 GHz**
- **Ceramic-metal hermetic package with low inductance and low parasitic capacitances**
- **Stable common-base operation**
- **For coaxial, microstripline, and lumped-constant circuit applications**
- **Integral emitter-ballasting resistors**

The RCA-HR2N5920 is a high-reliability version of the RCA-2N5920. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5920 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5920 transistor in RCA data bulletin file No. 440.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω, sustaining	$V_{CER}(sus)$	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
DC COLLECTOR CURRENT (Continuous)	I_C	0.25	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75° C		3.5	W
At case temperatures above 75° C, derate linearly		0.028	W/° C
For point of measurement of temperature (on collector terminal), see dimensional outline.			
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector or Base Voltage (V)		DC Current (mA)					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector Cutoff Current	I_{CES}	45	0				–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		1	50	–	V
	Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					5	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				10	100	–	1	V
*	Forward Current Transfer Ratio	h_{FE}	5				100	20	200	
	Thermal Resistance (Junction-to-collector terminal)	$R\theta_{JCT}$						–	30	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	POWER INPUT P_{IB}(W)	POWER OUTPUT P_{OB}(W)	SUPPLY VOLTAGE V_{CC}(V)	FREQUENCY (f) GHz	LIMITS		UNITS
						Min.	Max.	
Power Output	P_{OB}	0.2		28	2	2	–	W
Power Gain	G_{PB}	0.2	2.0	28	2	10	–	dB
Collector Efficiency	η_C	0.2	2.0	28	2	40	–	%
Collector-to-Base Capacitance	C_{obo}			30 (V_{CB})	1 MHz		3	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

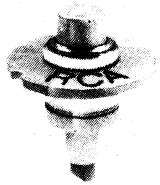
V_{CB} = 15 V

P_T = 2 W

RCA
Solid State
Division

RF Power Transistors

HR2N5921



JEDEC TO-201AA

H-1629

5-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **5-W output with 5.5-dB gain (typ.) at 2.3 GHz**
- **5-W output with 7-dB gain (min.) at 2 GHz**
- **10-W output with 11-dB gain (typ.) at 1.2 GHz**
- **Integral emitter-ballasting resistors**
- **Ceramic-metal hermetic package with low inductance and low parasitic capacitances**

The RCA-HR2N5921 is a high-reliability version of the RCA-2N5921. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N5921 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N5921 transistor in RCA data bulletin file No. 427.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
DC COLLECTOR CURRENT (Continuous)	I_C	0.7	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25° C		14.5	W
At case temperatures above 25° C, derate linearly		0.083	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector or Base Voltage (V)		DC Current (mA)					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector Cutoff Current	I_{CES}	45	0				–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	50	–	V
	Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					10	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				20	100	–	1	V
*	Forward Current Transfer Ratio	h_{FE}	5				500	20	200	
	Thermal Resistance (Junction-to-Flange)	$R_{\theta JF}$						–	12	°C/W

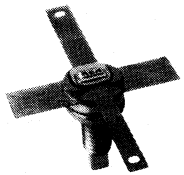
DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
		Frequency (f) – GHz	DC Collector Supply Voltage (V_{CC}) – V	Min.	Max.	
Output Power P_{IB} = 1 W	P_{OB}	2	28	5	–	W
Power Gain P_{OB} = 5 W	G_{PB}	2	28	7	–	dB
Collector Efficiency P_{OB} = 5 W	η_C	2	28	40	–	%
Collector-to-Base Capacitance V_{CB} = 30 V	C_{obo}	1 MHz	–	–	8.5	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_C = 125° C
V_{CB} = 8 V
P_T = 3.2 W



JEDEC TO-216AA H-1675

30-W, 400-MHz Broadband Emitter-Ballasted Silicon N-P-N Overlay Transistor

Features:

- **5-dB gain (min.) at 400 MHz with 30 watts (min.) output**
- **Emitter-ballasting resistors**
- **Broadband performance (225—400 MHz)**
- **Low-inductance ceramic-metal hermetic package**
- **Radial leads for microstripline circuits**
- **All electrodes isolated from the stud**

The RCA-HR2N6105 is a high-reliability version of the RCA-2N6105. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6105 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N6105 transistor in RCA data bulletin file No. 504.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	30	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	4.5	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 75° C		36	W
At case temperatures above 75° C		Derate linearly at 0.288	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
			DC Voltage V		DC Current mA				
			V_{CE}	V_{BE}	I_E	I_C	Min.	Max.	
*	Collector-to-Emitter Cutoff Current: Base connected to emitter	I_{CES}	30	0			–	10	mA
	Collector-to-Emitter Breakdown Voltage: With base connected to emitter	$V_{(BR)CES}$		0		200[a]	65	–	V
	With base open	$V_{(BR)CEO}$				200[a]	30	–	
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			5	0	4	—	V
*	Forward Current Transfer Ratio	h_{FE}	4			500	10	200	
	Thermal Resistance (Junction-to-Case)	$R\theta JC$						3.5	°C/W

[a]Pulsed through a 25-mH inductor; duty factor = 50%.

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS		UNITS
		DC Collector Supply (V_{CC}) – V	Input Power (P_{IE}) – W	Output Power (P_{OE}) – W	Frequency (F) – MHz	Min.	Max.	
Output Power	P_{OE}	28	9.5		400	30	–	W
Overdrive Test	P_{OEO}	28	12.0		400	34	–	
Power Gain	G_{PE}	28		30	400	5	–	dB
Collector Efficiency	η_C	28	9.5		400	65	–	%
Collector-to-Base Output Capacitance	C_{obo}	30 (V_{CB})			1	–	35	pF

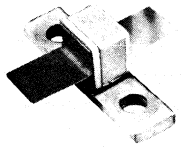
*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

V_{CB} = 28 V

P_T = 2.6 W



RCA HF-28 PACKAGE H-1712

2-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **VSWR capability of ∞: 1 at 2 GHz**
- **2-W output with 8.2-dB gain (min.) at 2 GHz**
- **3-W output with 12-dB gain (min.) at 1 GHz**
- **Ceramic-metal hermetic stripline package with low inductance and low parasitic capacitances**
- **For microstripline and lumped-constant circuit applications**

The RCA-HR2N6265 is a high-reliability version of the RCA-2N6265. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6265 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N6265 transistor in RCA data bulletin file No. 543.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.275	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75° C		6.25	W
At case temperature above 75° C		Derate linearly at 0.05	W/°C
TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector or Base Voltage (V)		DC Current (mA)					
			V_{CE}	B_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector Cutoff Current	I_{CES}	45	0				–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Breakdown Voltage: External base-to-emitter resistance R_{BE} = 10 Ω	$V_{(BR)CER}$					10	50	–	V
*	Forward Current Transfer Ratio	h_{FE}	5				100	10	200	
	Thermal Resistance (Junction-to-Flange)	$R\theta_{JF}$						–	20	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	POWER INPUT P_{IB}(W)	POWER OUTPUT P_{OB}(W)	SUPPLY VOLTAGE V_C(V)	FREQUENCY (f) GHz	LIMITS		UNITS
						Min.	Max.	
Power Output	P_{OB}	0.3		28	2	2	–	W
Power Gain	G_{PB}	0.3	2.0	28	2	8.2	–	dB
Collector Efficiency	η_C	0.3	2.0	28	2	33	–	%
Collector-to-Base Capacitance	C_{obo}			30 (V_{CB})	1 MHz	–	5	pF

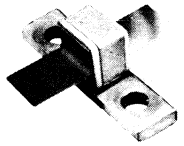
*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C

V_{CB} = 15 V

P_T = 2 W



RCA HF-28 Package

H-1712

5-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators,and Frequency Multipliers

Features:

- **Emitter-ballasting resistors**
- **VSWR capability of ∞: 1 at 2 GHz**
- **5-W output with 7-dB gain (min.) at 2 GHz**
- **13.5-W output with 11-dB gain (typ.) at 1 GHz**
- **Ceramic-metal hermetic stripline package with low inductance and low parasitic capacitances**
- **Stable common-base operation**
- **For microstripline, stripline, and lumped-constant circuit applications**

The RCA-HR2N6266 is a high-reliability version of the RCA-2N6266. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6266 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N6266 transistor in RCA data bulletin file No. 544.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	1	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75° C		14.8	W
At case temperature above 75° C		Derate linearly at 0.118	W/°C
TEMPERATURE RANGE:			
Storage and operaging (Junction)		−65 to +200	°C
CASE TEMPERATURE (During Soldering):			
For 10 s max.		230	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector or Base Voltage (V)		DC Current (mA)					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector Cutoff Current	I_{CES}	45	0				–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	50	–	V
	Emitter-to-Base Breakdown Voltage	$B_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Breakdown Voltage With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					10	50	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				20	100	–	1	V
*	Forward Current Transfer Ratio	h_{FE}	5				100	15	200	
	Thermal Resistance (Junction-to-Flange)	$R_{\theta JF}$						–	8.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
		Frequency (f) – GHz	DC Collector Supply Voltage (V_{CC}) – V	Min.	Max.	
Output Power, P_{IB} = 1 W	P_{OB}	2	28	5	–	W
Power Gain, P_{OB} = 5 W	G_{PB}	2	28	7	–	dB
Collector Efficiency, P_{OB} = 5 W	η_C	2	28	33	–	%
Collector-to-Base Capacitance V_{CB} = 30 V	C_{obo}	1 MHz		–	10	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_C = 135° C

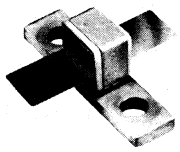
V_{CB} = 8 V

P_T = 3.2 W

RCA
Solid State
Division

RF Power Transistors

HR2N6267



RCA HF-28 PACKAGE H-1712

10-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistor

For UHF/Microwave Power Amplifiers, Microwave Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **Emitter-ballasting resistors**
- **10-W output with 7-dB gain (min.) at 2 GHz (28 V)**
- **8-W output with 6-dB gain (typ.) at 2.3 GHz (28 V)**
- **VSWR capability of 10:1 at 2 GHz**
- **Ceramic metal hermetic stripline package with low inductance and low parasitic capacitances**
- **Stable common-base operation**
- **For microstripline, stripline, and lumped-constant circuit applications**

The RCA-HR2N6267 is a high-reliability version of the RCA-2N6267. It is specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6267 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for this device are the same as those given for the basic 2N6267 transistor in RCA bulletin file No. 545.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	1.5	A
TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75° C		21	W
At case temperature above 75° C		Derate linearly at 0.168	W/°C
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C

II. GROUP A TESTS, at Case Temperature (T_C) = 25° C

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
			DC Collector or Base Voltage (V)		DC Current (mA)					
			V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
*	Collector Cutoff Current	I_{CES}	45	0				–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
	Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					10	50	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				20	100	–	1	V
*	Forward Current Transfer Ratio	h_{FE}	5				100	15	200	
	Thermal Resistance (Junction-to-Flange)	$R_{\theta JF}$						–	6	°C/W

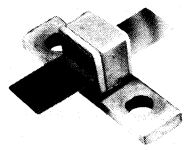
DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS		UNITS
		Frequency (f) – GHz	DC Collector Supply Voltage (V_{CC}) – V	Min.	Max.	
Output Power, P_{IB} = 2 W	P_{OB}	2	28	10	–	W
Power Gain, P_{OB} = 10 W	G_{PB}	2	28	7	–	dB
Collector Efficiency, P_{OB} = 10 W	η_C	2	28	35	–	%
Collector-to-Base Capacitance, V_{CB} = 30 V	C_{obo}	1 MHz		–	13	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_C = 145° C
V_{CB} = 8 V
P_T = 3.2 W



RCA HF-28 Package H-1712

6.5- and 2-W, 2.3-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistors

For Use in Microwave Power Amplifiers, Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **Designed for 20 to 24-V equipment**
- **Emitter-ballasting resistors**
- **VSWR capability of 10:1 at 2.3 GHz**
- **2-W output with 7-dB gain (min.) at 2.3 GHz (HR2N6268)**
- **6.5-W output with 5-dB gain (min.) at 2.3 GHz (HR2N6269)**
- **Stable common-base operation**

The RCA-HR2N6268 and RCA-HR2N6269 are high-reliability versions of the RCA-2N6268 and RCA-2N6269. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2N6268 and HR2N6269 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic 2N6268 and 2N6269 transistors in RCA data bulletin file No. 546.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

		HR2N6268	HR2N6269	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	45	45	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	45	45	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	0.350	1.5	A
TRANSISTOR DISSIPATION:	P_T			
At case temperature up to 75° C		6.25	21	W
At case temperature above 75° C ... Derate linearly at		0.05	0.168	W/°C
TEMPERATURE RANGE:				
Storage and operating (Junction)		−65 to +200		°C
CASE TEMPERATURE (During Soldering):				
For 10 s max.		230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS				UNITS
			DC COLLECTOR OR BASE VOLTAGE (V)		DC CURRENT (mA)			HR2N6268		HR2N6269		
			V_{CE}	V_{BE}	I_E	I_B	I_C	MIN.	MAX.	MIN.	MAX.	
*	Collector Cutoff Current	I_{CES}	40	0				–	2	–	2	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		5	45	–	45	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	3.5	–	V
	Collector-to-Emitter Breakdown Voltage With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$					10	45	–	45	–	V
	Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				10 20	100 100	– –	1 –	– –	– 1	V
	Thermal Resistance (Junction-to-Flange)	$R_{\theta JF}$						–	20	–	6	°C/W
*	Forward Current Transfer Ratio	h_{FE}	5				100	10	200	15	200	

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS				UNITS
		FREQUENCY (f) – GHz	DC COLLECTOR SUPPLY VOLTAGE (V_{CC}) – V	HR2N6268		HR2N6269		
				MIN.	MAX.	MIN.	MAX.	
Output Power, P_{IB} = 0.4 W = 2 W	P_{OB}	2.3 2.3	22 22	2 –	– –	– 6.5	– –	W
Power Gain, P_{OB} = 2 W = 6.5 W	G_{PB}	2.3 2.3	22 22	7 –	– –	– 5	– –	dB
Collector Efficiency, P_{OB} = 2 W = 6.5 W	η_C	2.3 2.3	22 22	33 –	– –	– 32	– –	%
Collector-to-Base Capacitance V_{CB} = 30 V	C_{obo}	1 MHz		–	5.5	–	13	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

	HR2N6268	HR2N6269	
T_A	25	–	°C
T_C	–	145	°C
V_{CB}	15	8	V
P_T	2	3.2	W

RCA
Solid State
Division

RF Power Transistors

HR2003 HR2N6390

RCA HF-46
(RCA HF-46 can also be supplied without flange upon request.)
H-1796

2.5- and 3-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistors

For Use in Microwave Power Amplifiers, Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **2.5-W output with 7-dB gain (min.) at 2 GHz, 28 V (HR2003)**
- **3-W output with 8-dB gain (min.) at 2 GHz, 28 V (HR2N6390)**
- **Load-VSWR capability of ∞: 1 at 2 GHz**
- **Emitter-ballasting resistors**
- **Stable common-base operation**

The RCA-HR2003 and RCA-HR2N6390 are high-reliability versions of the RCA 2003 and RCA 2N6390. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2003 and HR2N6390 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic RCA 2003 and 2N6390 transistors in RCA data bulletin file No. 626.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*		**HR2003**	**HR2N6390**	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	50	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	1	1	A
TRANSISTOR DISSIPATION:	P_T			
At case temperature up to 75° C		8.34	8.34	W
At case temperature above 75° C ... Derate linearly at		0.067	0.067	W/°C
TEMPERATURE RANGE:				
Storage and operating (Junction)		−65 to +200		°C
LEAD TEMPERATURE (During Soldering):				
At distances ≥ 0.02 in. (0.5 mm) from seating plane for 10 s max.		230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS				UNITS
			Voltage V dc		Current mA dc		HR2003		HR2N6390		
			V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	MIN.	MAX.	
*	Collector Cutoff Current: With emitter open	I_{CBO}		28	0		–	0.5	–	–	mA
	With emitter connected to base	I_{CES}	45				–	–	–	2	
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0 0	1 2	50 –	– –	– 50	– –	V
	Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$				5	50	–	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			1	0	3.5	–	3.5	–	V
*	Forward Current Transfer Ratio	h_{FE}	10			50	20	120	20	120	
	Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	15	–	15	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS				UNITS
		VOLTAGE V dc	FREQUENCY GHz	POWER W		HR2003		HR2N6390		
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	MIN.	MAX.	
Output Power	P_{OB}	28 28	2 2	0.5 0.475		2.5 –	– –	– 3	– –	W
Large-Signal Common-Base Power Gain	G_{PB}	28 28	2 2		2.5 3	7 –	– –	– 8	– –	dB
Collector Efficiency	η_C	28 28	2 2		2.5 3	30 –	– –	– 30	– –	%
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	5	–	5	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_A = 25° C
V_{CB} = 15 V
P_T = 2 W

RCA
Solid State
Division

RF Power Transistors

HR2005 HR2N6391

RCA HF-46
(RCA HF-46 can also be supplied without flange upon request.)
H-1796

5-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistors

For Use in Microwave Power Amplifiers, Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **5-W output with 7-dB gain (min.) at 2 GHz, 28 V for both types**
- **Load-VSWR capability of ∞: 1 at 2 GHz**
- **Emitter-ballasting resistors**
- **Stable common-base operation**

The RCA-HR2005 and RCA-HR2N6391 are high-reliability versions of the RCA2005 and RCA-2N6391. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2005 and HR2N6391 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic RCA2005 and 2N6391 transistors in RCA data bulletin file No. 627.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*

		HR2005	HR2N6391	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	50	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	2.5	2.5	A
TRANSISTOR DISSIPATION:	P_T			
At case temperature up to 75° C		16.7	16.7	W
At case temperature above 75° C ..... Derate linearly at		0.133	0.133	W/°C
TEMPERATURE RANGE:				
Storage and operating (Junction)		−65 to +200		°C
LEAD TEMPERATURE (During Soldering):				
At distances ≥ 0.02 in. (0.5 mm) from seating plane for 10 s max.			230	°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS				UNITS
		Voltage V dc		Current mA dc		HR2005		HR2N6391		
		V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	MIN.	MAX.	
* Collector Cutoff Current: With emitter open	I_{CBO}		28	0		–	0.5	–	–	mA
With emitter connected to base	I_{CES}	45				–	–	–	3	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0 0	1 5	50 –	– –	– 50	– –	V
Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$				5	50	–	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			1	0	3.5	–	3.5	–	V
* Forward Current Transfer Ratio	h_{FE}	10			200	20	120	20	120	
Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	7.5	–	7.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS				UNITS
		VOLTAGE V dc	FREQUENCY GHz	POWER W		HR2005		HR2N6391		
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	MIN.	MAX.	
Output Power	P_{OB}	28	2	1		5	–	5	–	W
Large-Signal Common-Base Power Gain	G_{PB}	28	2		5	7	–	7	–	dB
Collector Efficiency	η_C	28	2		5	30	–	30	–	%
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	9	–	9	pF

*Recorded before and after burn-in for each device (serialized).

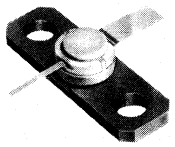
III. BURN-IN CONDITIONS

T_C = 135° C
V_{CB} = 8 V
P_T = 3.2 W

RCA
Solid State
Division

RF Power Transistors

HR2010 HR2N6392 HR2N6393



RCA HF-46
(RCA HF-46 can also be supplied without flange upon request.)
H-1796

10-W, 2-GHz, Emitter-Ballasted Silicon N-P-N Overlay Transistors

For Use in Microwave Power Amplifiers, Fundamental-Frequency Oscillators, and Frequency Multipliers

Features:

- **10-W output with 7-dB gain (min.) at 2 GHz, 28 V (HR2N6393)**
- **10-W output with 5-dB gain (min.) at 2 GHz, 28 V (HR2010, HR2N6392)**
- **Load-VSWR capability of 10:1 at 2 GHz**
- **Emitter-ballasting resistors**
- **Stable common-base operation**

The RCA-HR2010, RCA-HR2N6392, and RCA-HR2N6393 are high-reliability versions of the RCA 2010, RCA-2N6392, and RCA-2N6393. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR2010, HR2N6392, and HR2N6393 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic RCA2010, 2N6392, and 2N6393 transistors in RCA data bulletin file No. 628.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*		**HR2010**	**HR2N6392**	**HR2N6393**	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	50	45	V
COLLECTOR-TO-EMITTER VOLTAGE:					
With external base-to-emitter resistance, R_{BE} = 10 Ω	V_{CER}	50	50	45	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	3.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	3.5	3.5	3.5	A
TRANSISTOR DISSIPATION:	P_T				
At case temperature up to 75° C		21	21	21	W
At case temperature above 75° C ..... Derate linearly at		0.167	0.167	0.167	W/°C
TEMPERATURE RANGE:					
Storage and operating (Junction)			−65 to +200		°C
LEAD TEMPERATURE (During Soldering):					
At distances ≥ 0.02 in. (0.5 mm) from seating plane for 10 s max.			230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS Voltage V dc		TEST CONDITIONS Current mA dc		LIMITS HR2010		LIMITS HR2N6392		LIMITS HR2N6393		UNITS
			V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
*	Collector Cutoff Current: With emitter open	I_{CBO}		28			–	0.5	–	–	–	–	mA
	With emitter connected to base	I_{CES}	45 40				– –	– –	– –	3 –	– –	– 3	
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0	5	50	–	50	–	45	–	V
	Collector-to-Emitter Breakdown Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{(BR)CER}$				5	50	–	50	–	45	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			1	0	3.5	–	3.5	–	3.5	–	V
*	Forward Current Transfer Ratio	h_{FE}	10			500[a]	20	120	20	120	20	120	
	Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	6	–	6	–	6	°C/W

[a] Pulse test: pulse duration = 80 μs

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS VOLTAGE V dc	TEST CONDITIONS FREQUENCY GHz	TEST CONDITIONS POWER W		LIMITS HR2010		LIMITS HR2N6392		LIMITS HR2N6393		UNITS
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output Power	P_{OB}	28 28	2 2	2 3		– 10	– –	– 10	– –	10 –	– –	W
Large-Signal Common-Base Power Gain	G_{PB}	28	2		10	5	–	5	–	7	–	dB
Collector Efficiency	η_C	28	2		10	33	–	33	–	35	–	%
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	10	–	11	–	11	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

T_C = 145° C

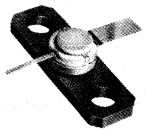
V_{CB} = 8 V

P_T = 3.2 W

RCA
Solid State
Division

RF Power Transistors

HR3001 HR3003 HR3005



RCA HF-46
(RCA HF-46 can also be supplied without flange upon request.)
H-1796

1-W, 2.5-W, and 4.5-W, 3-GHZ, Emitter-Ballasted N-P-N Transistors

Features:

- **1-W output with 7-dB gain (min.) at 3 GHz (HR3001)**
- **2.5-W output with 5-dB gain (min.) at 3 GHz (HR3003)**
- **4.5-W output with 5-dB gain (min.) at 3 GHz (HR3005)**
- **Emitter-ballasting resistors**
- **Stable common-base operation**
- **Hermetic stripline package with low inductances and low parasitic capacitances**
- **Load-VSWR capability of 10:1 at 3 GHz**

The RCA-HR3001, RCA-HR3003, and RCA-HR3005 are high-reliability versions of the RCA3001, RCA3003, and RCA3005. They are specially processed and screened for high reliability in accordance with the basic schedules outlined earlier in the discussion of Processing and Screening of HR-Series High-Reliability Transistors. The maximum ratings, specific electrical (Group A) tests and test limits, and the burn-in conditions for the HR3001, HR3003, and HR3005 are shown below. The basic electrical-characteristics curves and test conditions and the mechanical details for these devices are the same as those given for the basic RCA3001, RCA3003, and RCA3005 transistor in RCA data bulletin file No. 657.

I. MAXIMUM RATINGS, *Absolute-Maximum Values:*		**HR3001**	**HR3003**	**HR3005**	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	50	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	3.5	3.5	V
TRANSISTOR DISSIPATION:	P_T				
At case temperature up to 75° C		5	8.34	14.7	W
At case temperature above 75° C ..... Derate linearly at		0.04	0.067	0.118	W/°C
TEMPERATURE RANGE:					
Storage and operating (Junction)			−65 to +200		°C
LEAD TEMPERATURE (During Soldering):					
At distances ≥ 0.02 in. (0.5 mm) from seating plane for 10 s max.			230		°C

II. GROUP A TESTS, *at Case Temperature (T_C) = 25° C*

STATIC

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS						UNITS
			Voltage V dc		Current mA dc		HR3001		HR3003		HR3005		
			V_{CE}	V_{CB}	I_E	I_C	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
*	Collector Cutoff Current: With emitter open	I_{CBO}		28	0		–	0.5	–	0.5	–	0.5	mA
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0	5	50	–	50	–	50	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1	0	3.5	–	3.5	–	3.5	–	V
*	Forward Current Transfer Ratio	h_{FE}	5			100	15	120	15	120	15	120	
	Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$					–	25	–	15	–	8.5	°C/W

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS						UNITS
		VOLTAGE V dc	FREQUENCY GHz	POWER W		HR3001		HR3003		HR3005		
		V_{CC}	f	P_{IB}	P_{OB}	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output Power	P_{OB}	28	3	0.2		1.0	–	–	–	–	–	W
		28	3	0.8		–	–	2.5	–	–	–	
		28	3	1.4		–	–	–	–	4.5	–	
Large-Signal Common-Base Power Gain	G_{PB}	28	3		1.0	7	–	–	–	–	–	dB
		28	3		2.5	–	–	5	–	–	–	
		28	3		4.5	–	–	–	–	5	–	
Collector Efficiency	η_C	28	3		1.0	30	–	–	–	–	–	%
		28	3		2.5	–	–	30	–	–	–	
		28	3		4.5	–	–	–	–	30	–	
Collector-to-Base Output Capacitance	C_{obo}	V_{CB} = 28	1 MHz			–	3	–	5	–	7	pF

*Recorded before and after burn-in for each device (serialized).

III. BURN-IN CONDITIONS

	HR3001	HR3003	HR3005	
T_A	–	25	–	°C
T_C	130	–	145	°C
V_{CB}	15	15	8	V
P_T	1.9	2.0	3.2	W

RCA
Solid State
Division

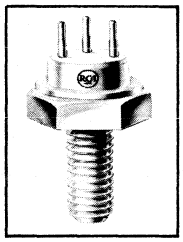
RF Power Transistors

40279

The RCA-40279 is the ultra-high reliability version of the RCA-2N3375 epitaxial silicon N-P-N planar transistor intended for class-A, -B, or -C amplifier, frequency multiplier, or oscillator operation. This device is subjected to special preconditioning tests for selection in ultra-high-reliability, large-signal, high-power, VHF-UHF applications in Space, Military, and Industrial communications equipment.

- **Ultra-High Reliability**
- **Complete Qualification Testing**

High-Power
VHF-UHF
Amplifier



JEDEC TO-60

RF SERVICE, Maximum Ratings (Absolute-Maximum Values)

Collector-To-Base Voltage, V_{CBO}	65	volts
Collector-To-Emitter Voltage:		
With base open, V_{CEO}	40	volts
With V_{BE} =-1.5 volts, V_{CEV}	65	volts
Emitter-To-Base Voltage, V_{EBO}	4	volts
Collector Current, I_C	1.5	amps.

Transistor Dissipation, P_T:		
At T_C up to 25°C	11.6	watts
At T_C above 25°C	Derate linearly to 0 watts at 200°C	
Temperature Range:		
Storage	-65 to 200	°C
Operating (Junction)	-65 to 200	°C
Lead Temperature (During soldering):		
At distances 1/32" from insulating wafer for 10 sec. max.	230	°C

ELECTRICAL CHARACTERISTICS – Case Temp. = 25°C (Unless Otherwise Specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		DC COLLECTOR VOLTS		DC BASE VOLTS	DC CURRENT (MILLIAMPERES)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-Cutoff Current	I_{CEO}	–	30	–	–	0	–	–	0.1	μa
Collector To-Base Breakdown Voltage	BV_{CBO}	–	–	–	0	–	0.1	65	–	Volts
Collector-To-Emitter Breakdown Voltage	BV_{CEO}	–	–	–	–	0	0 to 200*	40**	–	Volts
Collector-To-Emitter Breakdown Voltage	BV_{CEV}	–	–	-1.5	–	–	0 to 200*	65**	–	Volts
Emitter-To-Base Breakdown Voltage	BV_{EBO}	–	–	–	0.1	–	0	4	–	Volts
Collector-To-Emitter Saturation Voltage	V_{CE}(sat)	–	–	–	–	100	0.5 amp	–	1	Volt
Output Capacitance	C_{ob}	30	–	–	0	–	–	–	10	pf
RF Power Output Amplifier, Unneutralized										
At 100 Mc (See Fig. 1)	P_{OUT}	–	28	–	–	–	–	7.5●	–	Watts
At 400 Mc (See Fig. 2)		–	28	–	–	–	–	3▲	–	Watts
Forward Current Transfer Ratio	h_{FE}	–	5	–	–	–	150	10	–	–

* Pulsed through an inductor (25 mh); duty factor = 50%

** Measured at a current where the breakdown voltage is a minimum.

● For P_{IN} = 1.0 w; minimum efficiency = 65%

▲ For P_{IN} = 1.0 w; minimum efficiency = 40%

TO-60 DIMENSIONAL OUTLINE

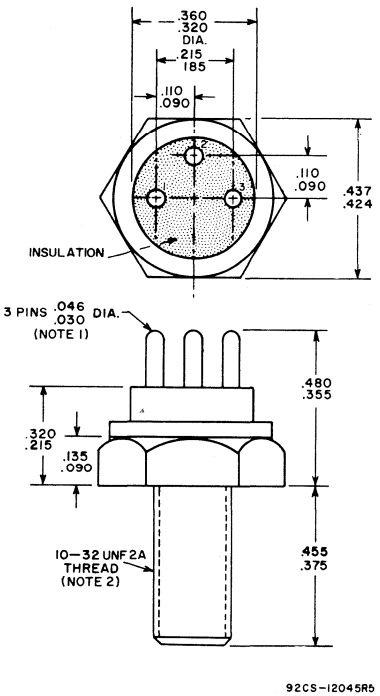
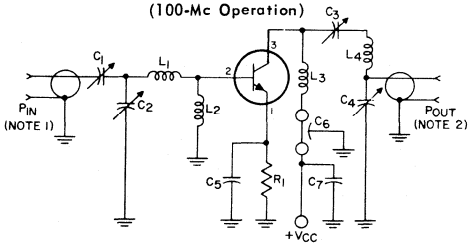


FIGURE 1

RF AMPLIFIER CIRCUIT FOR 40279
POWER-OUTPUT TEST
(100-Mc Operation)



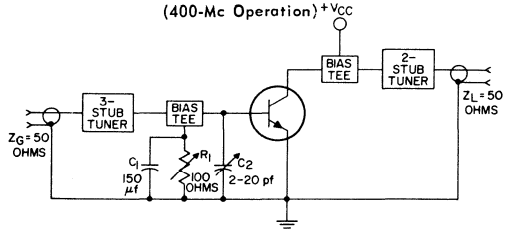
NOTE 1: GENERATOR IMPEDANCE = 50 OHMS.
NOTE 2: LOAD IMPEDANCE = 50 OHMS.

FOR 100-MC OPERATION

C_1, C_2: 7-100 PF
C_3, C_4: 4-40 PF
C_5: 330 PF, DISC CERAMIC
C_6: 1500 PF
C_7: 0.005 μF, DISC CERAMIC
L_1: 3 TURNS NO. 16 WIRE, 1/4" ID, 5/16" LONG
L_2: FERRITE CHOKE, Z = 750 (±20%) OHMS
L_3: 2.4-μH CHOKE
L_4: 5 TURNS NO. 16 WIRE, 5/16" ID, 7/16" LONG
R_1: 1.35 OHMS, NON-INDUCTIVE

FIGURE 2

RF AMPLIFIER CIRCUIT FOR 40279
POWER-OUTPUT TEST
(400-Mc Operation)



RELIABILITY TESTING

Electrically, the RCA-40279 is similar to the RCA-2N3375; the exception being the 40279 I_{CEO} is 100 nanoamperes maximum. In addition to Preconditioning and Group A tests, a Qualification Approval test series (Group B Tests) is performed on a semi-annual basis. All units are tested to assure freedom from second breakdown in Class-A applications.

Preconditioning (100 Per Cent Testing of Each Transistor)

1. Serialization
2. Record I_{CEO}, h_{FE}, V_{CE}(sat)
3. Temperature Cycling-Method 102A of MIL-STD-202, 5 cycles, -65°C +200°C
4. Bake, 72 hours minimum, +200°C
5. Constant Acceleration-Method 2006 of MIL-STD-750, 10, 000G, Y_1 and Y_2 axes
6. Record I_{CEO}, h_{FE}, V_{CE}(sat)
7. Reverse Bias Age, T_A = 150°C, V_{CB} = 28 V, t = 168 hours

*8. Record I_{CEO}, h_{FE}, V_{CE}(sat)

9. Power Age, T_A = 25°C, V_{CB} = 28 V, t = 500 hours, P_D = 2.6 W, free air

*10. Record I_{CEO}, h_{FE}, V_{CE}(sat) at 168 hours and 500 hours

11. Helium Leak, 1 x 10^{-8} cc/sec. max.
12. Methanol Bomb, 70 psig, 18 to 24 hours
13. X-Ray, RCA spec. 1750326
14. Record Subgroups 2 and 3 of Group A Tests

*
Delta criteria after 168 hours Reverse Bias Age and after 168 hours and 500 hour Power Age

ΔI_{CEO}	+100% or +10 nanoamperes whichever is greater
Δh_{FE}	±30%
ΔV_{CE}(sat)	±0.1 V

Group A Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
	Subgroup 1		10				
2071	Visual and Mechanical Examination	–	–	–	–	–	–
	Subgroup 2		5				
3036D	Collector-To-Emitter Cutoff Current	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	100	namps
3001D	Collector-To-Base Breakdown Voltage	I_C = 100 μa, I_E = 0	–	BV_{CBO}	65	–	Volts
3026D	Emitter-To-Base Breakdown Voltage	I_E = 100 μa, I_C = 0	–	BV_{EBO}	4	–	Volts
3011D	Collector-To-Emitter Breakdown Voltage	I_C = 0 to 200 ma (Inductive) I_B = 0	–	BV_{CEO}	40	–	Volts
3011A	Collector-To-Emitter Breakdown Voltage	I_C = 0 to 200 ma (inductive) V_{BE} = -1.5 V	–	BV_{CEV}	65	–	Volts
3071	Collector-To-Emitter Saturation Voltage	I_C = 500 ma, I_B = 100 ma	–	V_{CE}(sat)	–	1	Volt
3076	Forward Current Transfer Ratio	I_C = 150 ma V_{CE} = 5 V	–	h_{FE}	10	–	
	Subgroup 3		5				
3236	Output Capacitance	f = 140 Kc, V_{CB} = 30 V, I_E = 0	–	C_{ob}	–	10	pf
See Fig. 1	R.F. Power Output (Min. Eff. = 65%)	V_{CE} = 28 V P_i = 1 W, f = 100 mc	–	P_{OUT}	7.5	–	Watts
See Fig. 2	R.F. Power Output (Min. Eff. = 40%)	V_{CE} = 28 V, P_i = 1 W, f = 400 mc	–	P_{OUT}	3	–	Watts
	Subgroup 4		15				
3036D	Collector Cutoff Current	T_A = 150°C ± 3°C, V_{CB} = 30 V, I_E = 0	–	I_{CBO}	–	100	μamp
3076	Forward Current Transfer Ratio	T_A = 150°C ± 3°C, I_C = 150 ma, V_{CE} = 5 V	–	h_{FE}	–	200	–

Group B Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD*	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
	Subgroup 1 (10 samples)	–	7	–	–	–	–
2066	Physical Dimensions	TO-60	–	–	–	–	–
202/102A	Temperature Cycle	5∿, -65°C, 200°C	–	–	–	–	–
1056B	Thermal Shock	0°C, 100°C	–	–	–	–	–
1021	Moisture Resistance	Omit lead fatigue	–	–	–	–	–
2036D	Torque-To-Stud	1 minute, 12 inch pounds	–	–	–	–	–
	Subgroup 2 (10 samples)		7				
2016	Impact Shock	500G, 5 blows X_1, Y_1, Z_1, 1 msec.	–	–	–	–	–
2046	Vibration Fatigue	–	–	–	–	–	–
2056	Vibration Var. Freq.	–	–	–	–	–	–
	Subgroup 3 (10 samples)		7				
2026	Solderability	–	–	–	–	–	–
1066	Dew Point	25°C, -65°C read I_{CEO}	–	–	–	–	–
1001	Barometric Pressure	100,000 ft. read I_{CEO}	–	–	–	–	–
	Subgroup 4 (25 samples)		7				
1031	Storage Life	200°C, 1000 hr	–	–	–	–	–
2006	Constant Acceleration	20,000G, Y_1, Y_2	–	–	–	–	–
	Subgroup 5 (25 samples)		7				
1026	Operating Life	1000 hrs T_C = 140°C, V_{CB} = 28 V, P_D = 4 W	–	–	–	–	–
	End Points Subgroups 1, 2, 3, 4, 5						
3036D	Collector-Cutoff Current	V_{CE} = 30, I_B = 0	–	I_{CEO}	–	1	μamp
3011A	Collector-To-Emitter Breakdown Voltage	I_C = 0 to 200 ma (inductive) V_{BE} = -1.5 V	–	BV_{CEV}	60	–	Volts
	R.F. Power Output (See Fig. 1)	f = 100 mc, V_{CE} = 28 V, P_i = 1 W	–	P_{OUT}	6.5	–	Watts
3076	Forward Current Transfer Ratio	I_C = 150 ma, V_{CE} = 5 V	–	h_{FE}	9	–	–
3026D	Emitter-To-Base Breakdown Voltage	I_E = 100 μa, I_C = 0	–	BV_{EBO}	3.5	–	Volts

* Acceptance/Rejection Criteria of Group B tests: For an LTPD plan of 7% the total sample size is 80 for which the maximum number of rejects allowed is 2. Acceptance is also subject to a maximum of one (1) reject per Subgroup.

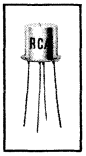
Group B tests are performed once every six months as part of Qualification Approval.

RCA
Solid State
Division

RF Power Transistors

40294

ULTRA-HIGH-RELIABILITY SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR



JEDEC
TO-72

For UHF Applications in Critical Aerospace and Military Equipment

RCA-40294 is an ultra-high-reliability double-diffused, epitaxial planar transistor of the silicon NPN type for low-noise amplifier, mixer, and oscillator applications at frequencies up to 500 MHz (common-emitter configuration), and up to 1200 MHz (common-base configuration).

This transistor is electrically and mechanically like RCA-2N2857, but is specially processed, preconditioned, and tested for critical aerospace and military applications.

The 40294 utilizes a hermetically sealed JEDEC TO-72 package. All active transistor elements are insulated from the case, which may be grounded by a fourth lead in applications requiring shielding of the device.

The curves of Typical Characteristics shown in the technical bulletin for RCA-2N2857 also apply for RCA-40294.

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	30 max.	V
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15 max.	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	2.5 max.	V
COLLECTOR CURRENT, I_C	40 max.	mA
TRANSISTOR DISSIPATION, P_T:		
For operation with heat sink:		
At case temperatures* up to 25°C	300 max.	mW
At case temperatures* above 25°C	Derate at 1.72	mW/°C
For operation in free air:		
At ambient temperatures up to 25°C	200 max.	mW
At ambient temperatures above 25°C	Derate at 1.14	mW/°C
TEMPERATURE RANGE:		
Storage and Operating (Junction)	-65 to +200	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds maximum.	265 max.	°C

* Measured at center of seating surface.

Features

- Meets performance requirements of TX2N2857 MIL-S-19500/343 USAF, 7 March 1966
- Extra-rigorous control and inspection of all parts, materials, and internal assemblies before sealing
- 100% thermal and mechanical preconditioning after sealing
- complete electrical and mechanical QUALITY CONFORMANCE test program
- 100% RELIABILITY ASSURANCE testing
- 100% PERFORMANCE-REQUIREMENTS testing
- 100% Noise Figure and Power Gain Tests at 450 MHz
- high gain-bandwidth product — f_T = 1000 MHz min.
- very low Device Noise Figure — NF = 4.5 dB max. at 450 MHz
- high power gain as neutralized amplifier — G_{pe} = 12.5 dB min. at 450 MHz for circuit bandwidth of 20 MHz
- high power output as uhf oscillator — P_o = 30 mW min. at 500 MHz
- low collector-to-base time constant — $r_b'C_c$ = 15 ps max.

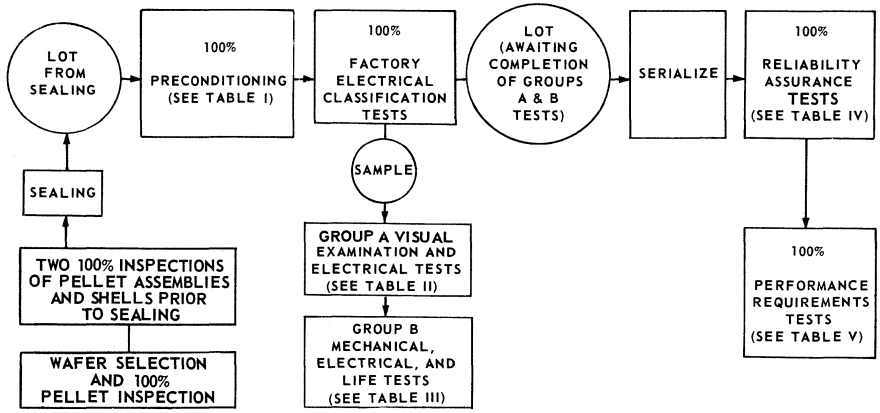


Fig. 1 - High-Reliability Testing Process Flow Diagram

TABLE I 100% PRECONDITIONING BEFORE FACTORY, QUALITY, RELIABILITY-ASSURANCE AND PERFORMANCE REQUIREMENTS TESTS

STABILIZATION BAKE	48 hours minimum at 200° C
TEMPERATURE CYCLING (PER MIL-STD-750 METHOD 1051, COND. C)	5 complete cycles from -65° C to +200° C, each including 15 minutes at -65° C, 15 minutes at +200° C, and 5 minutes at 25° C
HELIUM-LEAK TEST (PER MIL-STD-202, METHOD 112 COND. C, PROC.IIIA)	Leakage may not exceed 10^{-8} atm cc/s
BUBBLE TEST (PER MIL-STD-202, METHOD 112 COND. A)	150° C minimum, 1 minute, ethylene glycol
CONSTANT-ACCELERATION (CENTRIFUGE) TEST (PER MIL-STD-750, METHOD 2006)	20,000 G's; Y_1 plane, 1 minute

TABLE II

GROUP A TESTS

Subgroup	Lot Tolerance Per Cent Defective	Characteristic Test	Symbol	MIL-STD 750 Reference Test Method	TEST CONDITIONS							LIMITS		Units
					Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B	RCA 40294		
					°C	MHz	V	V	mA	mA	mA	Min.	Max.	
1	5	Visual and Mechanical Examination	--	2071	--	--	--	--	--	--	--	--	--	
2	3	Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0		--	10	nA
		Collector-Cutoff Current	I_{CES}	3041 Bias Condition C	25±3	--		16				--	100	nA
		Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0		30	--	V
		Collector-to-Emitter Breakdown Voltage	$BV_{CEO(sus)}$	3011 Test Condition D	25±3	--			3*		0	15	--	V
		Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	-0.001		2.5	--	V
		Base-to-Emitter Voltage	V_{BE}	3066 Test Condition A	25±3	--			10		1	--	1	V
		Collector-to-Emitter Voltage	V_{CE}	3071	25±3	--			10		1	--	0.4	V
		Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3			30	150	
3	10	Small-Signal Power Gain▲ (See Fig. 2 for Test Circuit)	G_{pe}		25±3	450		6	1.5			12.5	19	dB
		Device Noise Figure◈; Generator Resistance (R_G) = 50 Ω (See Fig. 3 for Test Circuit)	NF		25±3	450		6	1.5			--	4.5	dB
		Measured Noise Figure Generator Resistance R_G = 50Ω (See Fig. 3 for test circuit)▲	NF		25±3	450		6	1.5			--	5.0	dB
		Collector-to-Base Time Constant▲ (See Fig. 4 for Test Circuit)	$r_b'C_c$		25±3	31.9		6		-2		4	15	ps
		Oscillator Power Output (See Fig. 5 for Test Circuit)	P_o		25±3	≥500	10			-12		30	--	mW
		Collector-to-Base● Feedback Capacitance	C_{cb}		25±3	≥0.1 ≤1	10			0		--	1	pF
4	10	Static Forward Current Transfer Ratio (Low Temperature)	h_{FE}	3076	-55±3	--		1	3			10	--	
		Collector-Cutoff Current (High Temperature)	I_{CBO}	3036 Bias Condition D	150^{+0}_{-5}	--	15			0		--	1	μA
		Small-Signal, Short Circuit Forward Current-Transfer Ratio▲	h_{fe}	3206	25±3	0.001		6	2			50	220	
		Magnitude of Small-Signal, Short-Circuit Forward Current Transfer Ratio▲	$\lvert h_{fe} \rvert$	3206	25±3	100		6	5			10	19	

* Pulse Test

▲ Lead No. 4 (Case) Grounded

◈ Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test amplifier and the contribution of the following stages in the test setup.

● Three-terminal measurement with emitter and case leads guarded.

TABLE III
GROUP B TESTS

Subgroup	Test	MIL-STD 750 Reference	Lot Tolerance Per Cent Defective %	INITIAL AND ENDPOINT CHARACTERISTICS TESTS							Units
				Characteristic Test	MIL-STD 750 Reference	Test Conditions	RCA-40294 Initial Values Min.	Initial Values Max.	End Point Values Min.	End Point Values Max.	
1	PHYSICAL DIMENSIONS (See Dimensional Outline Drawing on page 7)	2066	20	--	--	--	--	--	--	--	
2	SOLDERABILITY Solder Temp. = 260±5°C	2026	10	I_{CBO}	3036D	T_A =25±3 °C, V_{CB}=15 V	--	10	--	10	nA
	TEMPERATURE-CYCLING TEST (Condition C)	1051									
	THERMAL-SHOCK TEST: T_{min} = 0^{+5}_{-0} °C, T_{max} = 100^{+0}_{-5} °C	1056 Test Condition A		h_{FE}	3076	T_A =25±3 °C, V_{CE}=1 V, I_C=3 mA	30	150	30	150	
	MOISTURE-RESISTANCE TEST	1021									
3	SHOCK TEST: NON-OPERATING 1500 G's, 0.5 ms 5 blows each in X_1, Y_1, Y_2, and Z_1 planes	2016	10	I_{CBO}	3036D	T_A =25±3 °C, V_{CB}=15 V	--	10	--	10	nA
	VIBRATION FATIGUE TEST: NON-OPERATING 60 ±20 Hz, 20 G's	2046		h_{FE}	3076	T_A =25±3°C, V_{CE}=1 V, I_C=3 mA	30	150	30	150	
	VIBRATION VARIABLE-FREQUENCY TEST	2056									
	CONSTANT-ACCELERATION TEST: 20,000 G's	2006									
4	TERMINAL STRENGTH TEST	2036 Test Condition E	20	Helium Leak Test	MIL-STD 202 Method112 Condition C Procedure III A		--	--	--	10^{-8}	atm cm^3/s
				Bubble Test	MIL-STD 202 Condition A	T_A=150°C (min.) 1 minute					
5	SALT-ATMOSPHERE TEST	1041	20	I_{CBO}	3036D	T_A =25±3 °C, V_{CB}=15 V	--	10	--	10	nA
				h_{FE}	3076	T_A =25±3°C, V_{CE}=1 V, I_C=3 mA	30	150	30	150	
6	HIGH-TEMPERATURE LIFE TEST (NON-OPERATING): T_A =200±10°C Duration=1000 hrs.	1031	λ= 7%	I_{CBO}	3036D	T_A =25±3° C, V_{CB}=15 V	--	10	--	20	nA
				h_{FE}	3076	T_A =25±3°C, V_{CE}=1 V, I_C=3 mA	30	150	24	180	
7	STEADY-STATE OPERATION LIFE TEST: Common-Base Circuit T_A =25±3° C V_{CB}=12.5±0.5 V PT=200 mW Duration=1000 hrs.	1026	λ= 7%	I_{CBO}	3036D	T_A =25±3 °C, V_{CB}=15 V	--	10	--	20	nA
				h_{FE}	3076	T_A =25±3 °C, V_{CE}=1 V, I_C=3 mA	30	150	24	180	

TABLE IV

100% RELIABILITY ASSURANCE TEST

THE CUMULATIVE REJECTS OF TABLES IV AND V SHALL NOT EXCEED 10% OF THE LOT

Test	MIL-STD 750 Reference	INITIAL AND ENDPOINT CHARACTERISTICS TESTS				
		Characteristic Test	RCA-40294 Initial Value	RCA-40294 Endpoint Value	MIL-STD 750 Reference	Test Conditions
POWER BURN-IN: Common-Base Circuit T_A =25±3°C V_{CB}=12.5±0.5 V P_T=200 mW Duration=340 hours	1026	ΔI_{CBO}	10 max. nA	Δ=±5 nA	3036 Bias Condition D	T_A =25±3°C V_{CB}=15 V
		Δh_{FE}	30 min. 150 max.	Δ=±15%	3076	T_A =25±3°C V_{CE}=1 V I_C=3 mA

TABLE V

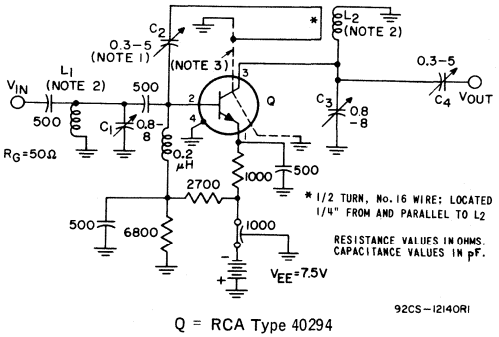
100% PERFORMANCE REQUIREMENTS TESTS

THE CUMULATIVE REJECTS OF TABLES IV AND V SHALL NOT EXCEED 10% OF THE LOT

Test	Symbol	MIL-STD 750 Reference	TEST CONDITIONS							LIMITS		Units
			Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B	RCA 40294		
			°C	MHz	V	V	mA	mA	mA	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0		--	10	nA
Collector-Cutoff Current	I_{CES}	3041 Bias Condition C	25±3	--		16				--	100	nA
Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0		30	--	V
Collector-to-Emitter Breakdown Voltage	BV_{CEO} (sus)	3011 Test Condition D	25±3	--			3*		0	15	--	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	−0.001		2.5	--	V
Base-to-Emitter Voltage	V_{BE}	3066 Test Condition A	25±3	--			10		1	--	1	V
Collector-to-Emitter Voltage	V_{CE}	3071	25±3	--			10		1	--	0.4	V
Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3			30	150	
Device Noise Figure▲: Generator Resistance (R_G)=50 Ohms (See Fig. 3 for Test Circuit)	NF	--	25±3	450		6	1.5			--	4.5	dB
Measured Noise Figure Generator Resistance R_G = 50Ω (See Fig.3 for test circuit)▲	NF		25±3	450		6	1.5			--	5.0	dB
Visual Examination (External) Under 20-Power Magnification		Examine leads, header, and shell for visual defects.										

* Pulse Test

▲ Lead No. 4 (Case) Grounded



Q = RCA Type 40294

NOTE 1: (NEUTRALIZATION PROCEDURE): (A) CONNECT A 450-MHz SIGNAL GENERATOR (WITH R_g = 50 OHMS) TC THE INPUT TERMINALS OF THE AMPLIFIER. (B) CONNECT A 50-OHM RF VOLTMETER ACROSS THE OUTPUT TERMINALS OF THE AMPLIFIER. (C) APPLY V_{EE}, AND WITH THE SIGNAL GENERATOR ADJUSTED FOR 5 mV OUTPUT FROM THE AMPLIFIER, TUNE C_1, C_3, AND C_4 FOR MAXIMUM OUTPUT. (D) INTERCHANGE THE CONNECTIONS TO THE SIGNAL GENERATOR AND THE RF VOLTMETER. (E) WITH SUFFICIENT SIGNAL APPLIED TO THE OUTPUT TERMINALS OF THE AMPLIFIER, ADJUST C_2 FOR A MINIMUM INDICATION AT THE INPUT (F) REPEAT STEPS (A), (B), AND (C) TO DETERMINE IF RETUNING IS NECESSARY.

NOTE 2: L_1 & L_2–SILVER-PLATED BRASS ROD, 1-1/2" LONG x 1/4" DIA. INSTALL AT LEAST 1/2" FROM NEAREST VERTICAL CHASSIS SURFACE.

NOTE 3: EXTERNAL INTERLEAD SHIELD TO ISOLATE THE COLLECTOR LEAD FROM THE EMITTER AND BASE LEADS.

Fig. 2 – Neutralized Amplifier Circuit Used to Measure 450-MHz Power Gain and Noise Figure for RCA-40294

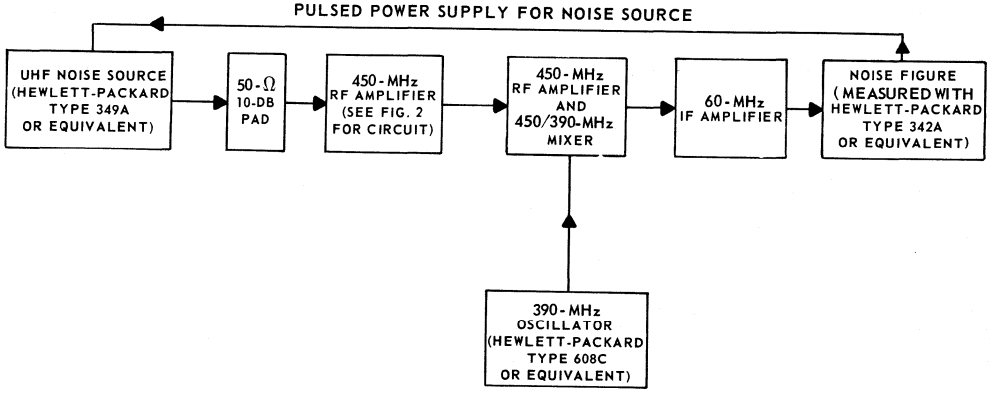
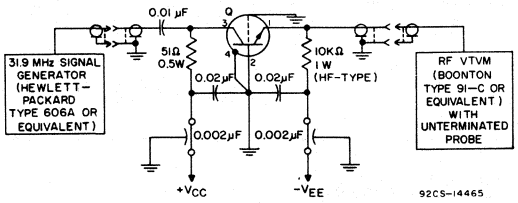


Fig. 3 - Block Diagram of 450-MHz Noise-Figure Test Circuit for RCA-40294



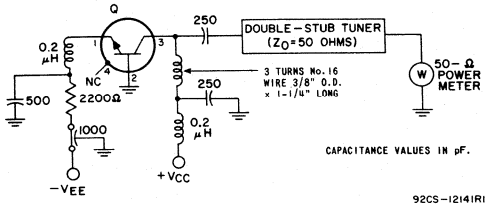
Q = RCA Type 40294

NOTE: Careful shielding must be used between input and output to keep signal feed-through to an absolute minimum.

PROCEDURE:

1. Before inserting the transistor in the test fixture, connect a short circuit between the collector and emitter terminals of the fixture and adjust the 31.9-MHz input for 0.5 V RMS at the emitter terminal.
2. Remove the short circuit between the collector and emitter terminals of the fixture, insert the transistor to be tested, and adjust V_{CC} and V_{EE} for V_{CB} = 6 V, I_C = 2 mA.
3. Read $r_b'C_c$ on rf-voltmeter scale ($r_b'C_c$ in picoseconds = 10 times meter indication in millivolts) (1 millivolt = 10 picoseconds).

Fig.4 - Collector-to-Base Time Constant Measurement Circuit

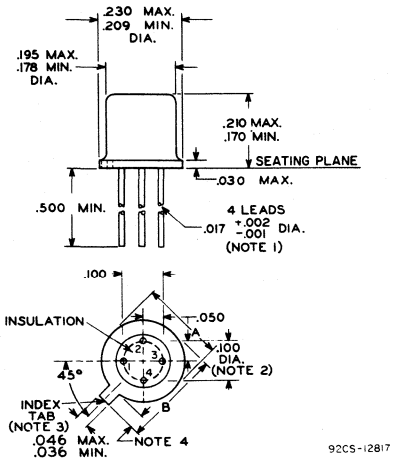


Q = RCA Type 40294

Fig.5 - Oscillator Circuit Used to Measure 500-MHz Power Output for RCA-40294

DIMENSIONAL OUTLINE

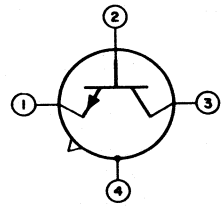
JEDEC TO-72



TERMINAL DIAGRAM

Bottom View

LEAD 1 – EMITTER
LEAD 2 – BASE
LEAD 3 – COLLECTOR
LEAD 4 – CONNECTED TO CASE



NOTE 1: THE SPECIFIED LEAD DIAMETER APPLIES IN THE ZONE BETWEEN 0.050" AND 0.250" FROM THE SEATING PLANE. FROM 0.250" TO THE END OF THE LEAD A MAXIMUM DIAMETER OF 0.021" IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIAMETER IS NOT CONTROLLED.

NOTE 2: MAXIMUM DIAMETER LEADS AT A GAUGING PLANE 0.054" + 0.001" – 0.000" BELOW SEATING PLANE TO BE WITHIN 0.007" OF THEIR TRUE LOCATION RELATIVE TO MAX. WIDTH TAB AND TO THE MAXIMUM 0.230" DIAMETER MEASURED WITH A SUITABLE GAUGE. WHEN GAUGE IS NOT USED, MEASUREMENT WILL BE MADE AT SEATING PLANE.

NOTE 3: FOR VISUAL ORIENTATION ONLY.

NOTE 4: TAB LENGTH TO BE 0.028" MINIMUM – 0.048" MAXIMUM, AND WILL BE DETERMINED BY SUBTRACTING DIAMETER A FROM DIMENSION B.

RCA
Solid State
Division

RF Power Transistors

40296

JEDEC TO-72 H-1299

Ultra-High-Reliability Silicon N-P-N Epitaxial Planar Transistor

For UHF Applications in Critical Aerospace and Military Equipment

Features:

- **Meets performance requirements of TX2N2857 MIL-S-19500/343 USAF, 7 March 1966**
- **Extra-rigorous control and inspection of all parts, materials, and internal assemblies before sealing**
- **100% thermal and mechanical preconditioning after sealing**
- **Complete electrical and mechanical QUALITY CONFORMANCE test program**
- **100% RELIABILITY ASSURANCE testing**
- **100% PERFORMANCE-REQUIREMENTS testing**
- **100% noise figure and power gain tests at 450 MHz**

RCA-40296 is an ultra-high-reliability double-diffused, epitaxial planar transistor of the silicon n-p-n type for low-noise amplifier, mixer, and oscillator applications at frequencies up to 500 MHz (common-emitter configuration), and up to 1200 MHz (common-base configuration).

This transistor is electrically and mechanically like RCA-2N2857, but is specially processed, preconditioned, and tested for critical aerospace and military applications.

The 40296 utilizes a hermetically sealed JEDEC TO-72 package. All active transistor elements are insulated from the case, which may be grounded by a fourth lead in applications requiring shielding of the device.

The curves of Typical Characteristics shown in the technical bulletin for RCA-2N2857 also apply for RCA-40296.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	2.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	40	mA
TRANSISTOR DISSIPATION	P_T		
With heat sink, at case* temperatures up to 25°C		300	mW
With heat sink, at case* temperatures above 25°C		Derate linearly 1.72	mW/°C
At ambient temperatures up to 25°C		200	mW
At ambient temperatures above 25°C		Derate linearly 1.14	mW/°C
TEMPERATURE RANGE:			
Storage & Operating (Junction)		-65 to +200	°C
CASE TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. (0.8 mm) from seating surface for 10 seconds max.		265	°C

* Measured at center of seating surface.

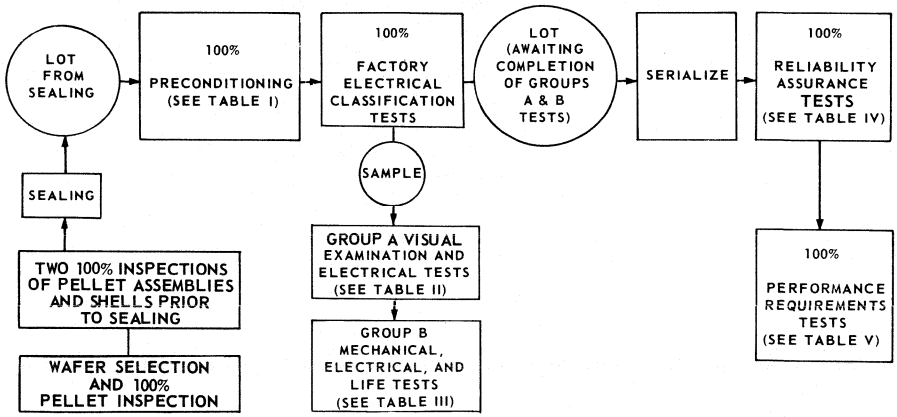
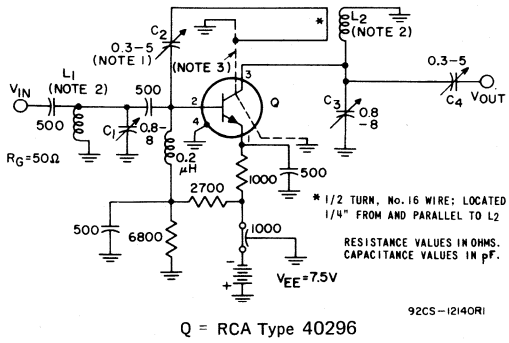


Fig. 1 - High-Reliability Testing Process Flow Diagram



Q = RCA Type 40296

NOTE 1: (NEUTRALIZATION PROCEDURE): (A) CONNECT A 450-MHz SIGNAL GENERATOR (WITH R_g = 50 OHMS) TO THE INPUT TERMINALS OF THE AMPLIFIER. (B) CONNECT A 50-OHM RF VOLTMETER ACROSS THE OUTPUT TERMINALS OF THE AMPLIFIER. (C) APPLY V_{EE}, AND WITH THE SIGNAL GENERATOR ADJUSTED FOR 5 mV OUTPUT FROM THE AMPLIFIER, TUNE C_1, C_3, AND C_4 FOR MAXIMUM OUTPUT. (D) INTERCHANGE THE CONNECTIONS TO THE SIGNAL GENERATOR AND THE RF VOLTMETER. (E) WITH SUFFICIENT SIGNAL APPLIED TO THE OUTPUT TERMINALS OF THE AMPLIFIER, ADJUST C_2 FOR A MINIMUM INDICATION AT THE INPUT. (F) REPEAT STEPS (A), (B), AND (C) TO DETERMINE IF RETUNING IS NECESSARY.

NOTE 2: L_1 & L_2—SILVER-PLATED BRASS ROD, 1-1/2" LONG x 1/4" DIA. INSTALL AT LEAST 1/2" FROM NEAREST VERTICAL CHASSIS SURFACE.

NOTE 3: EXTERNAL INTERLEAD SHIELD TO ISOLATE THE COLLECTOR LEAD FROM THE EMITTER AND BASE LEADS.

Fig. 2 - Neutralized Amplifier Circuit Used to Measure 450-MHz Power Gain and Noise Figure.

TABLE I 100% PRECONDITIONING BEFORE FACTORY, QUALITY, RELIABILITY-ASSURANCE AND PERFORMANCE REQUIREMENTS TESTS

STABILIZATION BAKE	48 hours minimum at 200° C
TEMPERATURE CYCLING (PER MIL-STD-750 METHOD 1051, COND. C)	5 complete cycles from -65° C to +200° C, each including 15 minutes at -65° C, 15 minutes at +200° C, and 5 minutes at 25° C
HELIUM-LEAK TEST (PER MIL-STD-202, METHOD 112 COND. C, PROC.IIIA)	Leakage may not exceed 10^{-8} atm cc/s
BUBBLE TEST (PER MIL-STD-202, METHOD 112 COND. A)	150° C minimum, 1 minute, ethylene glycol
CONSTANT-ACCELERATION (CENTRIFUGE) TEST (PER MIL-STD-750, METHOD 2006)	20,000 G's; Y_1 plane, 1 minute

TABLE II
GROUP A TESTS

Subgroup	Lot Tolerance Per Cent Defective	Characteristic Test	Symbol	MIL-STD 750 Reference Test Method	TEST CONDITIONS							LIMITS		Units
					Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B	RCA 40296		
					°C	MHz	V	V	mA	mA	mA	Min.	Max.	
1	5	Visual and Mechanical Examination	--	2071	--	--	--	--	--	--	--	--	--	
2	3	Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0		--	10	nA
		Collector-Cutoff Current	I_{CES}	3041 Bias Condition C	25±3	--		16				--	100	nA
		Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0		30	--	V
		Collector-to-Emitter Breakdown Voltage	$BV_{CEO(sus)}$	3011 Test Condition D	25±3	--			3*		0	15	--	V
		Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	0.001		2.5	--	V
		Base-to-Emitter Voltage	V_{BE}	3066 Test Condition A	25±3	--			10		1	--	1	V
		Collector-to-Emitter Voltage	V_{CE}	3071	25±3	--			10		1	--	0.4	V
		Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3			30	150	
3	10	Small-Signal Power Gain▲ (See Fig. 2 for Test Circuit)	G_{pe}		25±3	450		6	1.5			11.5	16.5	dB
		Device Noise Figure⊛: Generator Resistance (R_G) = 50 Ω (See Fig. 3 for Test Circuit)	NF		25±3	450		6	1.5			--	3.4	dB
		Measured Noise Figure Generator Resistance R_G = 50Ω (See Fig.3 for test circuit)▲	NF		25±3	450		6	1.5				4.2	dB
		Collector-to-Base Time Constant▲ (See Fig. 4 for Test Circuit)	$r_b'C_c$		25±3	31.9		6		-2		4	15	ps
		Oscillator Power Output (See Fig. 5 for Test Circuit)	P_o		25±3	≥500	10			-12		30	--	mW
		Collector-to-Base ● Feedback Capacitance	C_{cb}		25±3	≥0.1 ≤1	10			0		--	1	pF
4	10	Static Forward Current Transfer Ratio (Low Temperature)	h_{FE}	3076	-55±3	--		1	3			10	--	
		Collector-Cutoff Current (High Temperature)	I_{CBO}	3036 Bias Condition D	150^{+0}_{-5}	--	15			0		--	1	μA
		Small-Signal, Short Circuit Forward Current-Transfer Ratio▲	h_{fe}	3206	25±3	0.001		6	2			50	220	
		Magnitude of Small-Signal, Short-Circuit Forward Current Transfer Ratio▲	$\lvert h_{fe} \rvert$	3206	25±3	100		6	5			10	20	

* Pulse Test

▲ Lead No. 4 (Case) Grounded

⊛ Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test amplifier and the contribution of the following stages in the test setup.

● Three-terminal measurement with emitter and case leads guarded.

TABLE III
GROUP B TESTS

Subgroup	Test	MIL-STD 750 Reference	Lot Tolerance Per Cent Defective %	INITIAL AND ENDPOINT CHARACTERISTICS TESTS							Units
				Characteristic Test	MIL-STD 750 Reference	Test Conditions	RCA-40296 Initial Values Min.	Initial Values Max.	End Point Values Min.	End Point Values Max.	
1	PHYSICAL DIMENSIONS (See Dimensional Outline Drawing on page 7)	2066	20	--	--	--	--	--	--	--	
2	SOLDERABILITY Solder Temp. = 260±5°C	2026	10	I_{CBO}	3036D	T_A =25±3 °C, V_{CB}=15 V	--	10	--	10	nA
	TEMPERATURE-CYCLING TEST (Condition C)	1051									
	THERMAL-SHOCK TEST: T_{min} = 0^{+5}_{-0} °C, T_{max} = 100^{+0}_{-5} °C	1056 Test Condition A		h_{FE}	3076	T_A =25±3 °C, V_{CE}=1 V, I_C=3 mA	30	150	30	150	
	MOISTURE-RESISTANCE TEST	1021									
3	SHOCK TEST: NON-OPERATING 1500 G's, 0.5 ms 5 blows each in X_1, Y_1, Y_2, and Z_1 planes	2016	10	I_{CBO}	3036D	T_A =25±3 °C, V_{CB}=15 V	--	10	--	10	nA
	VIBRATION FATIGUE TEST: NON-OPERATING 60 ±20 Hz, 20 G's	2046		h_{FE}	3076	T_A =25±3°C, V_{CE}=1 V, I_C=3 mA	30	150	30	150	
	VIBRATION VARIABLE-FREQUENCY TEST	2056									
	CONSTANT-ACCELERATION TEST: 20,000 G's	2006									
4	TERMINAL STRENGTH TEST	2036 Test Condition E	20	Helium Leak Test	MIL-STD 202 Method 112 Condition C Procedure III A		--	--	--	10^{-8}	atm cm^3/s
				Bubble Test	MIL-STD 202 Condition A	T_A=150°C (min.) 1 minute					
5	SALT-ATMOSPHERE TEST	1041	20	I_{CBO}	3036D	T_A =25±3 °C, V_{CB}=15 V	--	10	--	10	nA
				h_{FE}	3076	T_A =25±3°C, V_{CE}=1 V, I_C=3 mA	30	150	30	150	
6	HIGH-TEMPERATURE LIFE TEST (NON-OPERATING): T_A =200±10° C Duration=1000 hrs.	1031	λ= 7%	I_{CBO}	3036D	T_A =25±3° C, V_{CB}=15 V	--	10	--	20	nA
				h_{FE}	3076	T_A =25±3°C, V_{CE}=1 V, I_C=3 mA	30	150	24	180	
7	STEADY-STATE OPERATION LIFE TEST: Common-Base Circuit T_A =25±3° C, V_{CB}=12.5±0.5 V, P_T=200 mW Duration=1000 hrs.	1026	λ= 7%	I_{CBO}	3036D	T_A =25±3 °C, V_{CB}=15 V	--	10	--	20	nA
				h_{FE}	3076	T_A =25±3°C, V_{CE}=1 V, I_C=3 mA	30	150	24	180	

TABLE IV

100% RELIABILITY ASSURANCE TEST

THE CUMULATIVE REJECTS OF TABLES IV AND V SHALL NOT EXCEED 10% OF THE LOT

Test	MIL-STD 750 Reference	INITIAL AND ENDPOINT CHARACTERISTICS TESTS				
		Characteristic Test	RCA-40296 Initial Value	RCA-40296 Endpoint Value	MIL-STD 750 Reference	Test Conditions
POWER BURN-IN: Common-Base Circuit T_A =25±3°C V_{CB}=12.5±0.5 V P_T=200 mW Duration=340 hours	1026	ΔI_{CBO}	10 max. nA	Δ= ±5 nA	3036 Bias Condition D	T_A =25±3 °C V_{CB}=15 V
		Δh_{FE}	30 min. 150 max.	Δ=±15%	3076	T_A =25±3°C V_{CE}=1 V I_C=3 mA

TABLE V

100% PERFORMANCE REQUIREMENTS TESTS

THE CUMULATIVE REJECTS OF TABLES IV AND V SHALL NOT EXCEED 10% OF THE LOT

Test	Symbol	MIL-STD 750 Reference	TEST CONDITIONS							LIMITS RCA 40296		Units
			Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B			
			°C	MHz	V	V	mA	mA	mA	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0		--	10	nA
Collector-Cutoff Current	I_{CES}	3041 Bias Condition C	25±3	--		16				--	100	nA
Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0		30	--	V
Collector-to-Emitter Breakdown Voltage	BV_{CEO} (sus)	3011 Test Condition D	25±3	--			3*		0	15	--	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	0.001		2.5	--	V
Base-to-Emitter Voltage	V_{BE}	3066 Test Condition A	25±3	--			10		1	--	1	V
Collector-to-Emitter Voltage	V_{CE}	3071	25±3	--			10		1	--	0.4	V
Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3			30	150	
Device Noise Figure▲: Generator Resistance (R_G)=50 Ohms (See Fig. 3 for Test Circuit)	NF	--	25±3	450		6	1.5			--	3.9	dB
Visual Examination (External) Under 20-Power Magnification		Examine leads, header, and shell for visual defects.										

* Pulse Test

▲ Lead No. 4 (Case) Grounded

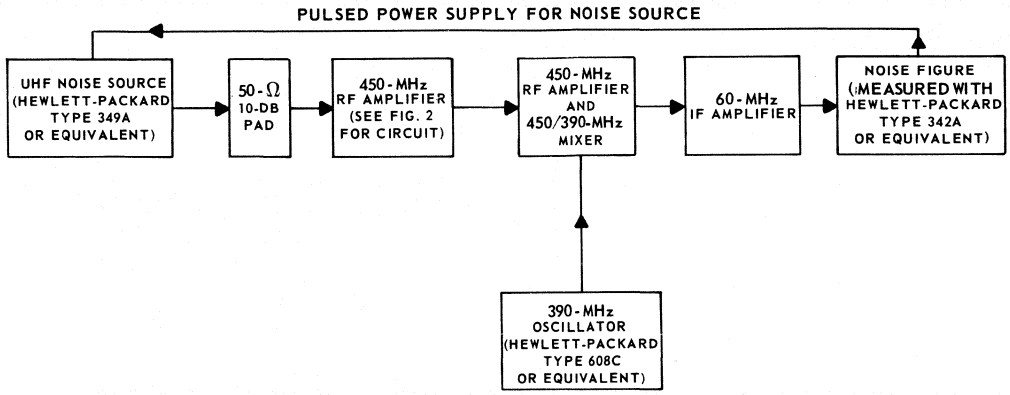
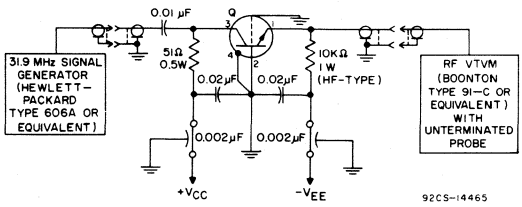


Fig. 3 - Block Diagram of 450-MHz Noise-Figure Test Circuit



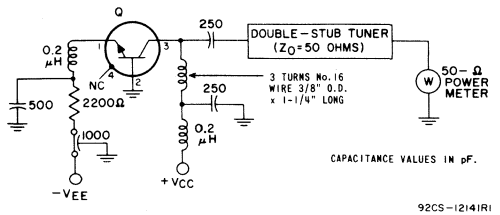
Q = RCA Type 40296

NOTE: Careful shielding must be used between input and output to keep signal feed-through to an absolute minimum.

PROCEDURE:

1. Before inserting the transistor in the test fixture, connect a short circuit between the collector and emitter terminals of the fixture and adjust the 31.9-MHz input for 0.5 V RMS at the emitter terminal.
2. Remove the short circuit between the collector and emitter terminals of the fixture, insert the transistor to be tested, and adjust V_{CC} and V_{EE} for V_{CB} = 6 V, I_C = 2 mA.
3. Read $r_b'C_c$ on rf-voltmeter scale ($r_b'C_c$ in picoseconds = 10 times meter indication in millivolts) (1 millivolt = 10 picoseconds).

Fig. 4 - Collector-to-Base Time Constant Measurement Circuit

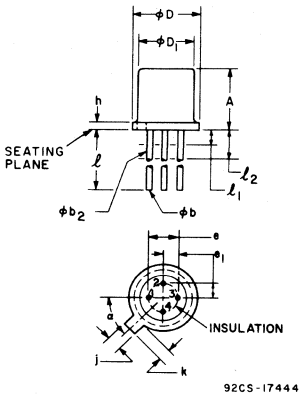


Q = RCA Type 40296

Fig. 5 - Oscillator Circuit Used to Measure 500-MHz Power Output

DIMENSIONAL OUTLINE

JEDEC TO–72



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
φb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
φD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) ϕb_2 applies between l_1 and l_2. φb applies between l_2 and 0.50 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.50 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter 0.019 in. (0.484 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.025 mm) – 0.000 (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

Note 6: Tab centerline.

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector
Lead 4 – Connected to case

RCA
Solid State
Division

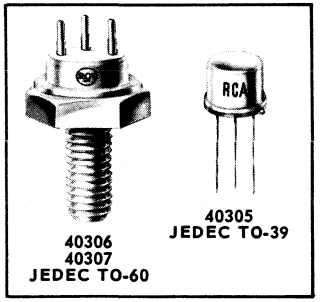
RF Power Transistors
40305
40306
40307

RCA-40305, 40306, and 40307 are high-reliability variants of RCA-2N3553, 2N3375, and 2N3632 epitaxial silicon n-p-n overlay transistors. They are intended for Class-A▲, -B, or -C amplifier, frequency multiplier, or oscillator operation.

These devices are subjected to special preconditioning tests for selection in high-reliability, large-signal, high-power, VHF-UHF applications in Space, Military, and Industrial communications equipment.

High Reliability

High-Power VHF-UHF Amplifier



40306
40307
JEDEC TO-60

40305
JEDEC TO-39

FEATURES

- High-Reliability Assured By Seven (7) Preconditioning Steps
- Data Recorded Before and After "Power-Age Test" and Held to Critical Delta Criteria
- High Voltage Ratings —
  V_{CBO} = 65 volts max.
  V_{CEV} = 65 volts max.
  V_{CEO} = 40 volts max.
- 100 Per-Cent Tested to Assure Freedom from Second Breakdown for Operation in Class-A Applications
- High Power Output, P_{OUT}, Unneutralized Class-C Amplifier —
  At 400 Mc, 3 w min. (40306)
  175 Mc { 13.5 w min. (40307) / 2.5 w min. (40305)
  100 Mc, 7.5 w min. (40306)

RF SERVICE▲

Maximum Ratings, *Absolute-Maximum Values*

	40305	40306	40307	
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	65	65	65	volts
COLLECTOR-TO-EMITTER VOLTAGE:				
With base open, V_{CEO}	40	40	40	volts
With V_{BE} = -1.5 volts, V_{CEV}	65	65	65	volts
EMITTER-TO-BASE VOLTAGE, V_{EBO}	4	4	4	volts
COLLECTOR CURRENT, I_C	1.0	1.5	3.0	amperes
TRANSISTOR DISSIPATION, P_T▲:				
At case temperatures up to 25° C	7.0	11.6	23	watts

	40305	40306	40307	
At case temperatures above 25° C	Derate linearly to 0 watts at 200° C			
TEMPERATURE RANGE:				
Storage	-65 to 200			°C
Operating (Junction)	-65 to 200			°C
PIN OR LEAD TEMPERATURE (During soldering):				
At distances ≧ 1/32" from insulating wafer (TO-60 package) or from seating plane (TO-39 package) for 10 sec. max.	230			°C

▲Secondary breakdown considerations limit maximum DC operating conditions — contact your RCA representative for specific data.

ELECTRICAL CHARACTERISTICS

Case Temperature = 25° C

Characteristic	Symbol	TEST CONDITIONS						LIMITS						Units
		DC Collector Volts		DC Base Volts	DC Current (Milliamperes)			40305		40306		40307		
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current	I_{CEO}		30			0		-	0.1	-	0.1	-	0.25	μamp
Collector-to-Base Breakdown Voltage	BV_{CBO}				0 0 0		0.1 0.3 0.5	- 65 -	- - -	65 - -	- - -	- - 65	- - -	volts
Emitter-to-Base Breakdown Voltage	BV_{EBO}				0.1 0.25		0 0	4 -	- -	4 -	- -	- 4	- -	volts
Collector-to-Emitter Breakdown Voltage	BV_{CEO}					0	0 to 200[a]	40[b]	-	40[b]	-	40[b]	-	volts
	BV_{CEX}			-1.5			0 to 200[a]	65[b]	-	65[b]	-	65[b]	-	volts
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$					100 50	500 250	- -	- 1	- -	1 -	- -	1 -	volt
DC Forward-Current Transfer Ratio	h_{FE}		5 5				150 300	10 -	- -	10 -	- -	- 10	- -	
Collector-to-Base Capacitance Measured at 1 Mc	C_{ob}	30			0			-	10	-	10	-	20	pf
RF Power Output Amplifier, Unneutralized At 100 Mc (See *Fig.2*) 175 Mc (See *Fig.1*) 175 Mc (See *Fig.3*) 400 Mc (See *Fig.4*)	P_{OUT}		28 28 28 28					- 2.5[d] - -	- - - -	7.5[c] - - 3[f]	- - - -	- - 13.5[e] -	- - - -	watts

[a] Pulsed through an inductor (25 mh); duty factor = 50%.

[b] Measured at a current where the breakdown voltage is a minimum.

[c] For P_{IN} = 1.0 w; minimum efficiency = 65%.

[d] For P_{IN} = 1/4 w; minimum efficiency = 50%.

[e] For P_{IN} = 3.5 w; minimum efficiency = 70%.

[f] For P_{IN} = 1.0 w; minimum efficiency = 40%.

RELIABILITY TESTING

RCA types 40305, 40306, and 40307 are electrically similar to RCA-2N3553, 2N3375, and 2N3632 respectively; but they differ in that they have substantially lower collector-cutoff current. I_{CEO} for the 40305 and 40306 is 100 nanoamperes maximum and I_{CEO} for the 40307 is 250 nanoamperes maximum.

Preconditioning (100 Per-Cent Testing of Each Transistor)

1. Helium Leak, 1 x 10^{-8} cc/sec. max.
2. Temperature Cycling-Method 102A of MIL-STD-202, 3 cycles, -65° C to +200° C
3. Methanol Bomb, 70 psig, 16 hours minimum
4. Bake, 72 hours minimum, +200° C
5. Constant Acceleration-Method 2006 of MIL-STD-750, 10,000 G, Y_1 axis
6. Serialization
7. Record I_{CEO}, h_{FE}, V_{CE}(sat)
8. Power Age, T_A = 25° C, V_{CB} = 28 V, t = 168 hours, free air
   P_D(40305) = 1 watt
   P_D(40306, 40307) = 2.6 watts
* 9. Record I_{CEO}, h_{FE}, V_{CE}(sat)
10. X-Ray Inspection, RCA Spec. 1750326
11. Record Subgroups 2 and 3 of Group A Tests.

* Delta criteria after 168 hours Power Age

I_{CEO}	40305 40306	+100% or +10 nanoamperes whichever is greater
I_{CEO}	40307	+100% or +25 nanoamperes whichever is greater
h_{FE}		±30%
V_{CE}(sat)		±0.1 V

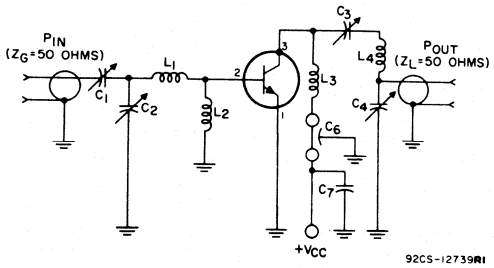
Group A Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	SYMBOL	CONDITIONS	LTPD	LIMITS						UNITS
					40305		40306		40307		
					Min.	Max.	Min.	Max.	Min.	Max.	
2071	**Subgroup 1** Visual and Mechanical Examination	-	-	10 -	-	-	-	-	-	-	-
3041D	**Subgroup 2** Collector-To-Emitter Cutoff Current	I_{CEO}	V_{CE} = 30 V, I_B = 0	5 -	-	0.1	-	0.1	-	0.25	μamp
3001D	Collector-To-Base Breakdown Voltage	BV_{CBO}	I_C = 300 μa, I_E = 0	-	65	-	-	-	-	-	volts
			I_C = 100 μa, I_E = 0	-	-	-	65	-	-	-	volts
			I_C = 500 μa, I_E = 0	-	-	-	-	-	65	-	volts
3026D	Emitter-To-Base Breakdown Voltage	BV_{EBO}	I_E = 100 μa, I_C = 0	-	4	-	4	-	-	-	volts
			I_E = 250 μa, I_C = 0	-	-	-	-	-	4	-	volts
3011D	Collector-To-Emitter Breakdown Voltage	BV_{CEO}	I_C = 0 to 200 ma[a], I_B = 0	-	40[b]	-	40[b]	-	40[b]	-	volts
3011A	Collector-To-Emitter Breakdown Voltage	BV_{CEX}	I_C = 0 to 200 ma[a], V_{BE} = -1.5 V	-	65[b]	-	65[b]	-	65[b]	-	volts
3071	Collector-To-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 250 ma, I_B = 50 ma	-	-	1	-	-	-	-	volts
			I_C = 500 ma, I_B = 100 ma	-	-	-	-	1	-	1	volts
3076	Forward Current Transfer Ratio	h_{FE}	I_C = 150 ma, V_{CE} = 5 V	-	10	-	10	-	-	-	
			I_C = 300 ma, V_{CE} = 5 V	-	-	-	-	-	10	-	
3236	**Subgroup 3** Open Circuit Output Capacitance	C_{ob}	f = 1 Mc, V_{CB} = 30 V, I_E = 0	5 -	-	10	-	10	-	20	pf
See Fig.1	R. F. Power Output	P_{OUT}	V_{CE} = 28 V, P_{IN} = 0.25 watt, f = 175 Mc, Min. Effic. = 50%	-	2.5	-	-	-	-	-	watts
See Fig.2			V_{CE} = 28 V, P_{IN} = 1 watt, f = 100 Mc, Min. Effic. = 65%	-	-	-	7.5	-	-	-	watts
See Fig.3			V_{CE} = 28 V, P_{IN} = 3.5 watts, f = 175 Mc, Min. Effic. = 70%	-	-	-	-	-	13.5	-	watts
See Fig.4			V_{CE} = 28 V, P_{IN} = 1 watt, f = 400 Mc, Min. Effic. = 40%	-	-	-	3	-	-	-	watts
3036D	**Subgroup 4** Collector Cutoff Current	I_{CBO}	T_A = 150° C ± 3° C, V_{CB} = 30 V, I_E = 0	15 -	-	100	-	100	-	250	μamp
3076	Forward Current Transfer Ratio	h_{FE}	T_A = 150° C ± 3° C, I_C = 150 ma, V_{CE} = 5 V	-	-	200	-	200	-	-	
			T_A = 150° C ± 3° C, I_C = 300 ma, V_{CE} = 5 V	-	-	-	-	-	-	200	

[a] Pulsed through an inductor (25 mh); duty factor = 50%.

[b] Measured at a current where the breakdown voltage is a minimum.

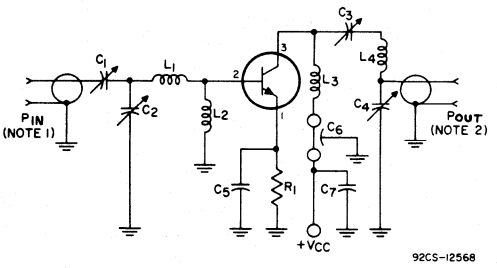
RF AMPLIFIER CIRCUIT FOR 40305
POWER-OUTPUT TEST
(175-Mc Operation)



C1,C2,C3,C4: 3-35 pf
C6: 1,000 pf
C7: 0.005 μf, disc ceramic
L1: 2 turns No.16 wire, 3/16" ID, 1/4" long
L2: Ferrite choke, Z = 450 ohms
L3: 2 turns No.16 wire, 1/4" ID, 1/4" long
L4: 4 turns No.16 wire, 3/8" ID, 3/8" long

Fig.1

RF AMPLIFIER CIRCUIT FOR 40306
POWER-OUTPUT TEST
(100-Mc Operation)



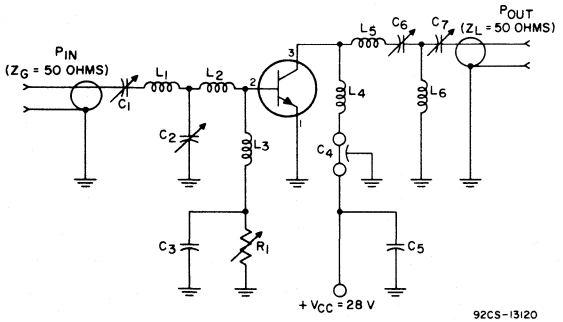
NOTE 1: GENERATOR IMPEDANCE = 50 OHMS.
NOTE 2: LOAD IMPEDANCE = 50 OHMS.

For 100-Mc Operation:

C1,C2: 7-100 pf
C3,C4: 4-40 pf
C5: 330 pf, disc ceramic
C6: 1500 pf
C7: 0.005 μf, disc ceramic
L1: 3 turns No.16 wire, 1/4" ID, 5/16" long
L2: Ferrite choke, Z = 750(±20%) ohms
L3: 2.4-μh choke
L4: 5 turns No.16 wire, 5/16" ID, 7/16" long
R1: 1.35 ohms, non-inductive

Fig.2

RF AMPLIFIER CIRCUIT FOR 40307
POWER-OUTPUT TEST
(175-Mc Operation)



For 175-Mc Operation:

C1,C6: 3-35 pf
C2,C7: 8-60 pf
C4: 1,000 pf
C3,C5: 0.005 μf, disc ceramic
L1,L5: 4 turns No.18 wire, 1/4" ID, 3/16" long
L2: 1 turn No.16 wire, 1/4" ID, 3/16" long
L3: Ferrite choke, Z = 450 ohms
L4: RF choke, 1.0 μh
L6: 2-1/2 turns No.16 wire, 1/4" ID, 1/4" long
R1: 50 ohms

Fig.3

RF AMPLIFIER CIRCUIT FOR 40306
POWER-OUTPUT TEST
(400-Mc Operation)

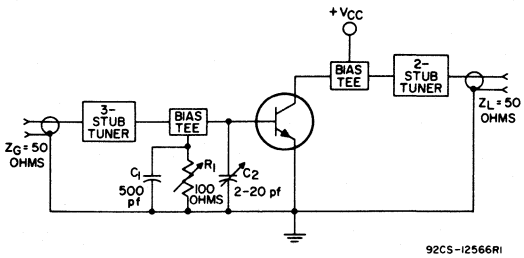
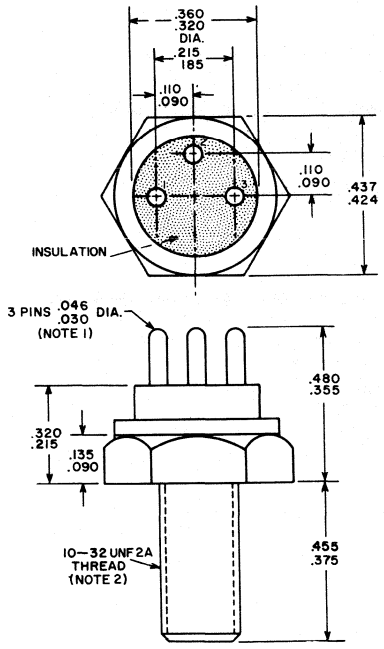


Fig.4

DIMENSIONAL OUTLINES

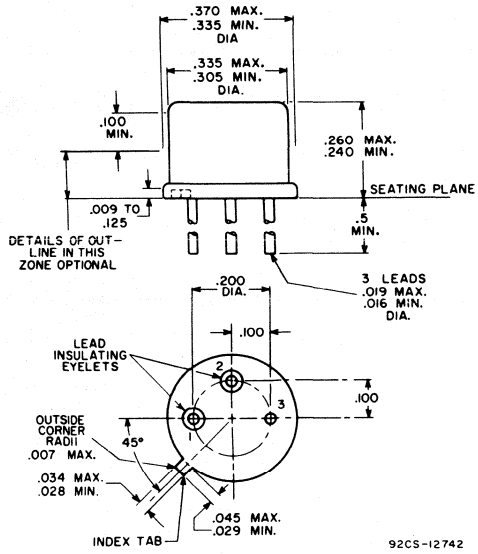
FOR TYPES 40306, 40307
JEDEC TO-60



92CS-12045R5

Dimensions in Inches

FOR TYPE 40305
JEDEC TO-39



92CS-12742

Dimensions in Inches

NOTE 1: THE PIN SPACING PERMITS INSERTION IN ANY SOCKET HAVING A PIN-CIRCLE DIAMETER OF 0.200" AND CONTACTS WHICH WILL ACCOMMODATE PINS HAVING A DIAMETER OF 0.035" MIN., 0.045" MAX.

NOTE 2: THE TORQUE APPLIED TO A 10-32 HEX NUT ASSEMBLED ON THE THREAD DURING INSTALLATION SHOULD NOT EXCEED 12 INCH-POUNDS.

NOTE 3: THIS DEVICE MAY BE OPERATED IN ANY POSITION.

TERMINAL CONNECTIONS

Pin or Lead No.1 - Emitter

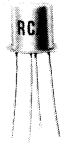
Pin or Lead No.2 - Base

Pin or Lead No.3 - Collector (For 40306, 40307)
Collector, Case (For 40305)

RCA
Solid State
Division

RF Power Transistors

40414



JEDEC TO-72 H-1299

High-Reliability Silicon N-P-N Epitaxial Planar Transistor

For UHF Applications in Industrial and Military Equipment

Features:

- **High gain-bandwidth product: f_T = 1000 MHz min.**
- **High converter (450-to-30 MHz) gain: G_c = 15 dB typ. for circuit bandwidth of approximately 2 MHz**
- **High power gain as neutralized amplifier: G_{PE} = 12.5 dB min. at 450 MHz for circuit bandwidth of 20 MHz**
- **High power output as uhf oscillator: P_{OE} = {30 mW min., 40 mW typ. at 500 MHz; 20 mW typ., at 1 GHz}**
- **Low device noise figure: NF = {4.5 dB max. as 450 MHz amplifier; 7.5 dB typ., as 450-to-30 MHz converter}**
- **Low collector-to-base time constant: $r_b'C_c$ = 7 ps typ.**
- **Low collector-to- base feedback capacitance: C_{cb} = 0.6 pF typ.**

RCA-40414 is a double-diffused epitaxial planar transistor of the silicon n-p-n type. It is extremely useful in low-noise-amplifier, oscillator, and converter applications at frequencies up to 500 MHz in the common-emitter configuration, and up to 1200 MHz in the common-base configuration.

The 40414 is electrically and mechanically like the RCA-2N2857, but each shipment of the RCA-40414 is accompanied by a certified summary of the results of the Group A Electrical Tests and the Group B Environmental Tests shown in Tables I and II, respectively. The Test Data Summary and Certification shown in the Specimen Copy on page 5 are the results of the acceptance tests for the production lot from which the shipment is made.

RCA-40414 utilizes a hermetically sealed 4-lead JEDEC TO-72 package. All active elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead in applications requiring shielding of the device.

The curves of Typical Characteristics shown in the Technical Bulletin for RCA-2N2857 also apply for RCA-40414.

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	2.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	40	mA
TRANSISTOR DISSIPATION	P_T		
At case temperatures* up to 25°C		300	mW
At case temperatures* above 25°C		Derate linearly 1.71	mW/°C
At ambient temperatures up to 25°C		200	mW
At ambient temperatures above 25°C		Derate linearly 1.14	mW/°C
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to +200	°C
CASE TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. (0.8 mm) from seating surface for 10 seconds max.		265	°C

* Measured at center of seating surface.

TABLE I – GROUP A TESTS

Subgroup	Lot Tolerance Per Cent Defective	Characteristic Test	Symbol	MIL-STD 750 Reference Test Method	TEST CONDITIONS						LIMITS		Units
					Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Collector Current I_C	DC Emitter Current I_E	RCA 40414		
					°C	MHz	V	V	mA	mA	Min.	Max.	
1	10	Visual and Mechanical Examination	--	2071	--	--	--	--	--	--	--	--	
2	5	Collector-Cutoff Current	I_{CBO}	3036 Bias Condition D	25±3	--	15			0	--	10	nA
		Collector-to-Base Breakdown Voltage	BV_{CBO}	3001 Test Condition D	25±3	--			0.001	0	30	--	V
		Collector-to-Emitter Breakdown Voltage	BV_{CEO} (sus)	3011 Test Condition D	25±3	--			3*	$I_B = 0$	15	--	V
		Emitter-to-Base Breakdown Voltage	BV_{EBO}	3026 Test Condition D	25±3	--			0	-0.01	2.5	--	V
		Static Forward Current-Transfer Ratio	h_{FE}	3076	25±3	--		1	3		30	150	
3	15	Small-Signal Power Gain▲(See Fig.1 for Test Circuit)	G_{pe}		25±3	450		6	1.5		12.5	19	dB
		Device Noise Figure※ Generator Resistance (R_G) = 50Ω (See Fig.2 for Test Circuit)	NF		25±3	450		6	1.5		--	4.5	dB
		Measured Noise Figure: Generator Resistance (R_G)= 50Ω (See Fig.2 for test circuit)▲	NF		25±3	450		6	1.5		--	5.0	dB
		Collector-to-Base Time Constant▲(See Fig.3 for Test Circuit)	$r_b'C_c$		25±3	31.9	6		2		4	15	ps
		Oscillator Power Output (See Fig.4 for Test Circuit)	P_o		25±3	≥500	10			-12	30	--	mW
		Collector-to-Base Feedback Capacitance●	C_{cb}		25±3	≥0.1 ≤1	10			0	--	1	pF
4	15	Static Forward Current Transfer Ratio (Low Temperature)	h_{FE}	3076	-55±3	--		1	3		10	--	
		Collector-Cutoff Current (High Temperature)	I_{CBO}	3036 Bias Condition D	+0 150 -5	--	15			0	--	1	μA
		Small-Signal, Short Circuit Forward Current-Transfer Ratio▲	h_{fe}	3206	25±3	0.001		6	2		50	220	
		Magnitude of Small-Signal, Short-Circuit Forward Current-Transfer Ratio▲	$\lvert h_{fe} \rvert$	3206	25±3	100		6	5		10	19	

* Pulse Test

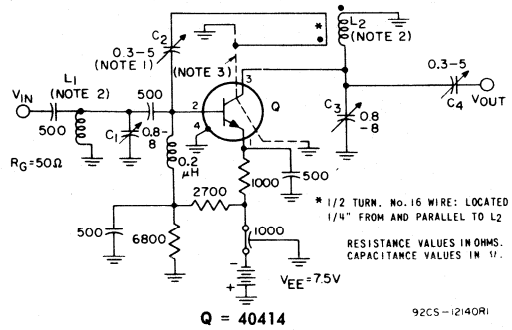
▲Lead No.4 (Case) Grounded

●Three-terminal measurement with emitter and case leads guarded.

※Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test amplifier and the contribution of the following stages in the test setup.

TABLE II – GROUP B TESTS

Subgroup	Test	MIL-STD 750 Reference	Lot Tolerance Per Cent Defective	INITIAL AND ENDPOINT CHARACTERISTICS TESTS							Units
				Characteristic Test	MIL-STD 750 Reference	Test Conditions	RCA-40414 Initial Values		RCA-40414 End Point Values		
			%				Min.	Max.	Min.	Max.	
1	PHYSICAL DIMENSIONS (See Dimensional Outline Drawing on page 6)	2066	20	--	--	--	--	--	--	--	
2	SOLDERABILITY Without Aging	2026	20	I_{CBO}	3036D	$T_A = 25 \pm 3^oC$, $V_{CB} = 15$ V	--	10	--	30	nA
	TEMPERATURE-CYCLING TEST (Condition C)	1051									
	THERMAL-SHOCK TEST: $T_{min} = 0^{+5}_{-0}\ ^oC$, $T_{max} = 100^{+0}_{-5}\ ^oC$	1056 Test Condition A		h_{FE}	3076	$T_A = 25 \pm 3^oC$, $V_{CE} = 1$ V, $I_C = 3$ mA	30	150	18	--	
	MOISTURE-RESISTANCE TEST	1021									
3	SHOCK TEST: NON-OPERATING 1500 G's, 0.5 ms 5 blows each in X_1, Y_1, Y_2 and Z_1 planes	2016	20	I_{CBO}	3036D	$T_A = 25 \pm 3^oC$, $V_{CB} = 15$ V	--	10	--	30	nA
	VIBRATION FATIGUE TEST: NON-OPERATING 60 ± 20 Hz, 20 G's	2046									
	VIBRATION VARIABLE-FREQUENCY TEST	2056		h_{FE}	3076	$T_A = 25 \pm 3^oC$, $V_{CE} = 1$ V, $I_C = 3$ mA	30	150	18	--	
	CONSTANT-ACCELERATION TEST: 20,000 G's	2006									
4	TERMINAL STRENGTH TEST	2036 Test Condition E	20	--	--	--	--	--	--	--	
				--	--	--	--	--	--	--	
5	SALT-ATMOSPHERE TEST	1041	20	I_{CBO}	3036D	$T_A = 25 \pm 3^oC$, $V_{CB} = 15$ V	--	10	--	30	nA
				h_{FE}	3076	$T_A = 25 \pm 3^oC$, $V_{CE} = 1$ V, $I_C = 3$ mA	30	150	18	--	
6	HIGH-TEMPERATURE LIFE TEST (NON-OPERATING): $T_A = 200 \pm 10^oC$ Duration = 1000 hrs.	1031	$\lambda = 10\%$	I_{CBO}	3036D	$T_A = 25 \pm 3^oC$, $V_{CB} = 15$ V	--	10	--	30	nA
				h_{FE}	3076	$T_A = 25 \pm 3^oC$, $V_{CE} = 1$ V, $I_C = 3$ mA	30	150	18	--	
7	STEADY-STATE OPERATION LIFE TEST: Common-Base Circuit $T_A = 25 \pm 3^oC$ $V_{CB} = 12.5 \pm 0.5$ V $P_T = 200$ mW Duration = 1000 hrs.	1026	$\lambda = 10\%$	I_{CBO}	3036D	$T_A = 25 \pm 3^oC$, $V_{CB} = 15$ V	--	10	--	30	nA
				h_{FE}	3076	$T_A = 25 \pm 3^oC$, $V_{CE} = 1$ V, $I_C = 3$ mA	30	150	18	--	



NOTE 1: (NEUTRALIZATION PROCEDURE): (A) CONNECT A 450-MHz SIGNAL GENERATOR (WITH R_g = 50 OHMS) TC THE INPUT TERMINALS OF THE AMPLIFIER. (B) CONNECT A 50-OHM RF VOLTMETER ACROSS THE OUTPUT TERMINALS OF THE AMPLIFIER. (C) APPLY V_{EE}, AND WITH THE SIGNAL GENERATOR ADJUSTED FOR 5 mV OUTPUT FROM THE AMPLIFIER, TUNE C_1, C_3, AND C_4 FOR MAXIMUM OUTPUT. (D) INTERCHANGE THE CONNECTIONS TO THE SIGNAL GENERATOR AND THE RF VOLTMETER. (E) WITH SUFFICIENT SIGNAL APPLIED TO THE OUTPUT TERMINALS OF THE AMPLIFIER, ADJUST C_2 FOR A MINIMUM INDICATION AT THE INPUT (F) REPEAT STEPS (A), (B), AND (C) TO DETERMINE IF RETUNING IS NECESSARY.

NOTE 2: L_1 & L_2–SILVER-PLATED BRASS ROD, 1-1/2" LONG x 1/4" DIA. INSTALL AT LEAST 1/2" FROM NEAREST VERTICAL CHASSIS SURFACE.

NOTE 3: EXTERNAL INTERLEAD SHIELD TO ISOLATE THE COLLECTOR LEAD FROM THE EMITTER AND BASE LEADS.

Fig.1 - Neutralized Amplifier Circuit Used to Measure 450-HMz Power Gain and Noise Figure for RCA-40414.

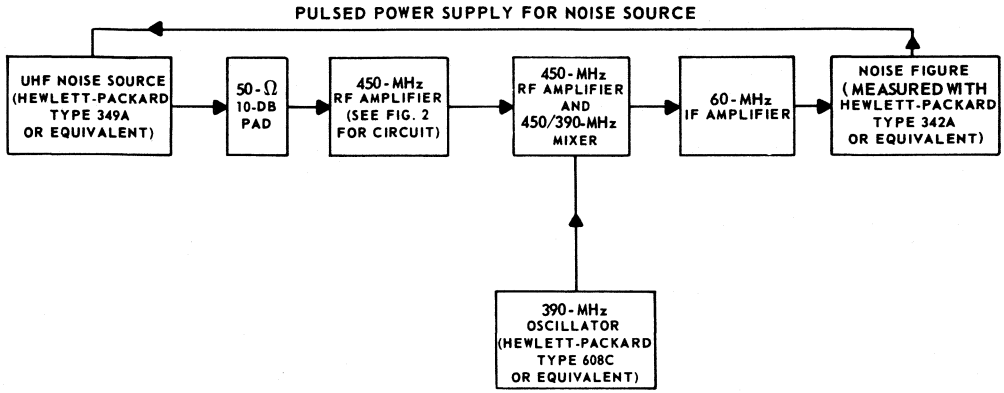
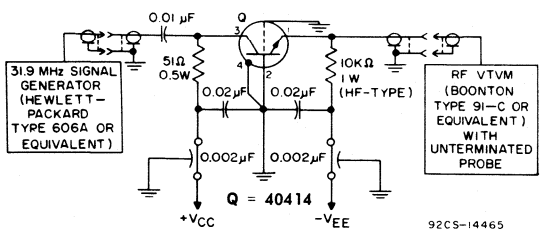


Fig.2 - Block Diagram of 450-MHz Noise-Figure Test Circuit for RCA-40414.



NOTE: Careful shielding must be used between input and output to keep signal feed-through to an absolute minimum.

PROCEDURE:

1. Before inserting the transistor in the test fixture, connect a short circuit between the collector and emitter terminals of the fixture and adjust the 31.9-MHz input for 0.5 V RMS at the emitter terminal.
2. Remove the short circuit between the collector and emitter terminals of the fixture, insert the transistor to be tested, and adjust V_{CC} and V_{EE} for V_{CB} = 6 V, I_C = 2 mA.
3. Read $r_b'C_c$ on rf-voltmeter scale ($r_b'C_c$ in picoseconds = 10 times meter indication in millivolts) (1 millivolt = 10 picoseconds).

Fig.3 - Collector-to-Base Time Constant Measurement Circuit.

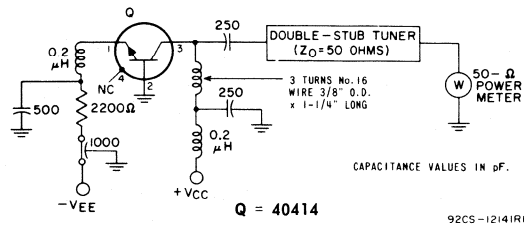


Fig.4 - Oscillator Circuit Used to Measure 500-MHz Power Output for RCA-40414.

RCA SOLID STATE DIVISION
SOMERVILLE, NEW JERSEY

TEST DATA SUMMARY AND CERTIFICATION

RCA TYPE 40414 LOT IDENTITY _____

TEST DATA SUMMARY

ITEM	TEST DESCRIPTION	LTPD	SAMPLE SIZE	DEFECTS ALLOWED	DEFECTS FOUND
	GROUP A TESTS				
Subgroup 1	Visual and Mechanical Examination	10			
Subgroup 2	Electrical	5			
Subgroup 3	Electrical	10			
Subgroup 4	Electrical	20			
	GROUP B TESTS				
Subgroup 1	Physical Dimensions	20			
Subgroup 2	Solderability; Temperature Cycling; Thermal Shock; Moisture Resistance	20			
Subgroup 3	Shock, Vibration Fatigue, Vibration, Variable Frequency, Constant Acceleration	20			
Subgroup 4	Terminal Strength	20			
Subgroup 5	Salt Atmosphere	20			
Subgroup 6	High-Temperature Life, Non-Operating	λ = 10%			
Subgroup 7	Steady-State Operation Life	λ = 10%			

CERTIFICATION

I hereby certify that the data listed above is complete, accurate and representative of the product week indicated. The above data was obtained in accordance with RCA specifications.

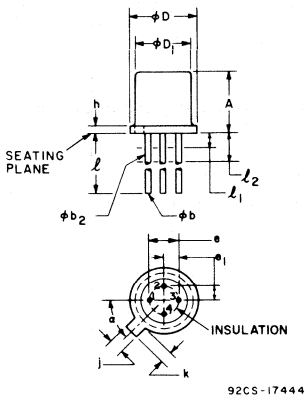
SEAL

SIGNATURE
QUALITY CONTROL MANAGER

DATE _____

DIMENSIONAL OUTLINE

JEDEC TO–72



TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector
Lead 4 – Connected to case

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.50 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.50 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter 0.019 in. (0.484 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.025 mm) – 0.000 (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

Note 6: Tab centerline.

RCA
Solid State
Division

RF Power Transistors

40577

HIGH-RELIABILITY TRANSISTOR

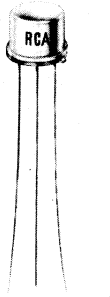
High-Gain Device for Class A or C Operation in VHF Circuits

RCA–40577* is a high-reliability variant of the RCA–2N3118, a triple-diffused transistor. It is especially processed for high reliability. It is intended for Class A and C amplifier, frequency multiplier or oscillator operation in high-reliability, large-signal, high-power VHF applications in Space, Military, and Industrial communications equipment.

High reliability is assured by eight preconditioning steps, including drift temperature measurements after the High Temperature Reverse Bias and Power Age tests. The 40577 also features complete qualification and lot acceptance testing.

*Formerly RCA-Dev. No. TA7079

- 8 Preconditioning Steps
- Complete Qualification and Lot Acceptance Testing
- 1.0 Watt Output Min. at 50 MHz
- 0.4 Watt Output Min. at 150 MHz



JEDEC TO–5

H–1380

RATINGS

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE:			
With V_{BE} = −1.5 volts	V_{CEV}	85	V
With base open	V_{CEO}	60	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
COLLECTOR CURRENT	I_C	0.5	A
TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 25° C		3	W
At free-air temperatures up to 25° C		0.5	W
At case temperatures above 25° C		See *Fig.4*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. from insulating wafer for 10 s max.		230	°C

TYPICAL POWER OUTPUT vs. POWER INPUT

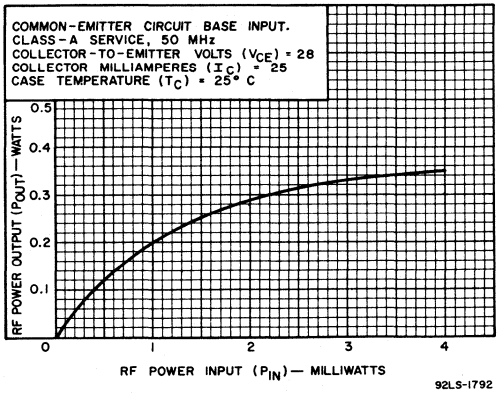


Fig. 1

ELECTRICAL CHARACTERISTICS
Case Temperature = 25° C
Except As Indicated

Characteristics	Symbols	TEST CONDITIONS							LIMITS		Units
		Frequency (MHz)	DC Collector-to-Base Voltage (volts)	DC Collector-to-Emitter Voltage (volts)	DC Base Volts	DC Current (Milliamperes)					
		f	V_{CB}	V_{CE}	V_{BE}	I_C	I_E	I_B	Min.	Max.	
Collector-Cutoff Current 25 °C[a]	I_{CBO}		30				0			10	nA
Collector-Cutoff Current 150 °C[a]	I_{CBO}		30				0			5	μA
Emitter-to-Base Breakdown Voltage	BVEBO					0	0.1		4		volts
Collector-to-Emitter Breakdown Voltage (Sustaining)	$BV_{CEO(sus)}$					10 pulsed[b]		0	60		volts
Reverse Collector-to-Emitter Breakdown Voltage	BV_{CEX}				−1.5	0.1			85		volts
Output Capacitance	C_{ob}	1	28			0				6	pF
$r_{bb}' C_b'_c$ Product	$r_{bb}' C_b'_c$	50		28		25				60	ps
DC Forward-Current Transfer Ratio[b]	h_{FE}			5		100			50	275	
Small-Signal Forward-Current Transfer Ratio	h_{fe}	50		28		25			5		
Real Part of Short-Circuit Input Impedance	$h_{ie(real)}$	50		28		25			25	75	ohms
Real Part of Short-Circuit Output Impedance	$1/Y_{22(real)}$	50		28		25			500	1000	ohms
Output Power Class-C Service Pin = 0.1 watt (with heat sink)	P_{OUT}	50[c]		28					1.0		watt
		150[d]		28					0.4		watt
Power Gain Class-A Service P_{out} = 0.2 watt (with heat sink)	PG	50[e]		28		25			18		dB

[a] T_{FA} = free air temperature.
[b] Pulse duration 300 μs; duty factor, less than 1.8%.
[c] See Figure 9.
[d] See Figure 3.
[e] See Figure 5.

TYPICAL LARGE-SIGNAL OPERATION, CLASS-C SERVICE
150 MHz

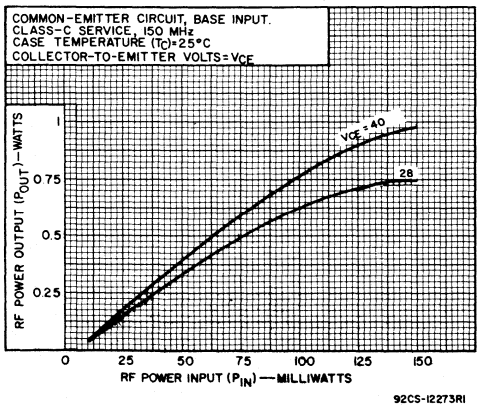
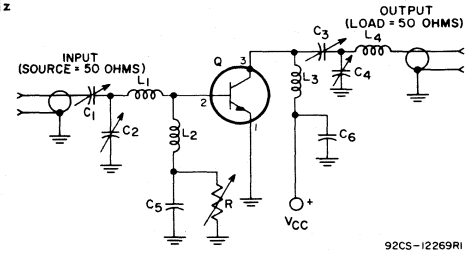


Fig. 2



C_1, C_2: 1.5–20 pF
C_3: 4–40 pF
C_4: 7–100 pF
C_5: 1800 pF
C_6: 0.01 μF
R: 100 ohms, variable

L_1: 0.1 μH, 4 turns, No.18 wire, 1/4" ID, closely wound
L_2: 750-ohm ferrite choke
L_3: 0.075 μH, 4 turns, No.16 wire, 1/4" ID x 3/8" long
L_4: 0.055 μH, 3 turns, No.16 wire, 1/4" ID x 1/4" long
Q: 40577

Fig. 3

RELIABILITY SPECIFICATIONS . . . . . .

In addition to Preconditioning and Group A tests, a Qualification Approval test series (Group B tests) is performed on each lot.

Preconditioning (100 Per Cent Testing of Each Transistor)

1. Serialization
2. Record I_{CBO}, h_{FE}
3. Temperature Cycling-Method 107B, Cond. C of MIL-STD-202, 5 cycles, -65^{o} C to 200^{o} C
4. Bake, 72 hours minimum, 200^{o} C
5. Constant Acceleration-Method 2006 of MIL-STD-750, 10,000g, Y_1 and Y_2 axes
6. X-Ray
7. Record I_{CBO}, h_{FE}
8. Reverse Bias Age, $T_A = 175^{o}$ C, $V_{CB} = 60$ V, t = 96 hours
9. [d] Record I_{CBO}, h_{FE}.
10. Power Age, $T_A = 25^{o}$ C, $V_{CB} = 28$ V, t = 340 hours, $P_T = 1$ W, free air
11. [d] Record I_{CBO}, h_{FE} at 340 hours
12. Helium Leak, 1 x 10^{-7} cc/sec. max.
13. Gross Leak, MIL-STD-202, Method 112
14. Record Subgroups 2 and 3 of Group A Tests

[d] Delta criteria after 96 hours Reverse Bias Age and 340 hours Power Age.

ΔI_{CBO}	+100% or +5 nanoamperes whichever is greater
Δh_{FE}	±20%

Definitions

Delta (Δ): Delta shall be determined by subtracting the parameter value measured before application of stress from the value measured after the application of stress.

Group A Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD	SYMBOL	LIMITS Min.	LIMITS Max.	UNITS
	Subgroup 1		10				
2071	Visual and Mechanical Examination	—	—	—	—	—	—
	Subgroup 2		5				
3036D	Collector-Cutoff Current	V_{CB} = 30V, I_E = 0	—	I_{CBO}	—	10	nA
3001D	Collector-to-Emitter Breakdown Voltage	I_C = 100 μA, V_{BE} = −1.5 V	—	BV_{CEV}	85[g]	—	volts
3026D	Emitter-to-Base Breakdown Voltage	I_E = 100 μA, I_C = 0	—	BV_{EBO}	4	—	volts
3011D	Collector-to-Emitter Breakdown Voltage	I_C = 10 mA[f], I_B = 0	—	V_{CEO}	60[g]	—	volts
3076	DC Forward-Current Transfer Ratio	I_C = 100 mA, V_{CE} = 5V	—	h_{FE}	50	275	
	Subgroup 3		5				
3236	Output Capacitance	f = 0.1 to 1.0 MHz, V_{CB}=28V, I_E = 0	—	C_{ob}	—	6.0	pF
See *Fig.3*	Power Output	f = 50 MHz, V_{CE} = 28V, Pin = 0.1 W	—	P_{OUT}	1.0	—	watts
See *Fig.5*	RF Power Output (Min. Eff. = 45%)	V_{CE} = 28 V, P_{IN} = 0.1 W, f = 150 MHz	—	P_{OUT}	0.4	—	watts
3306	Small-Signal Forward-Current Transfer Ratio	I_C = 25 mA, V_{CE} = 28 V, f = 50 MHz	—	h_{fe}	—	5.0	
	Subgroup 4		15				
3036D	Collector-Cutoff Current	$T_A = 150^{o}$ C, V_{CB} = 30 V	—	I_{CBO}	—	5	μA
3201	Input Impedance	V_{CE} = 28 V, I_C = 25 mA, f = 50 MHz	—	h_{ie}	25	75	ohms
3231	Output Admittance	V_{CE} = 28 V, I_C = 25 mA, f = 50 MHz	—	Y_{22}	1	2	mmho

[f] Pulsed through an inductor (25 μH); duty factor = 50%.

[g] Measured at a current where the breakdown voltage is a minimum.

General Reliability Specifications that are applicable to all rf power transistors are given in booklet RFT-701 and must be used in conjunction with the specific Preconditioning, Group A Tests, and Group B Tests shown below.

Group B Tests[h]

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS
	Subgroup 1	(13 Samples)
2066	Physical Dimensions	JEDEC TO-5 Pkg.
	Subgroup 2	(13 Samples)
2026	Solderability	Omit aging, Dwell time = 10 s ± 1 s
1051	Thermal Shock (Temp. Cycling)	Test Condition C
1056	Thermal Shock (Glass Strain)	Test Condition B
	Seal (Leak Rate)	Method 112 of MIL-STD-202 Test Cond. C, procedure III; Test Cond. A for gross leaks
1021	Moisture Resistance	
	Subgroup 3	(13 Samples)
2016	Shock	1,500 g, 0.5 ms, 5 blows each orientation: X_1, Y_1, Y_2, Z_1
2046	Vibration Fatigue	Nonoperating
2056	Vibration Var. Freq.	—
2006	Constant Acceleration	20,000 G Y_1, Y_2
	Subgroup 4	(13 Samples)
2036	Terminal Strength (Lead Fatique)	Test Cond. E
	Subgroup 5	(13 Samples)
1041	Salt Atmosphere	
	Subgroup 6	(25 Samples)
1031	High Temperature Life (Non-operating)	$T_{storage}$ = 200° C t = 1000 hrs.
	Subgroup 7	(25 Samples)
1026	Steady-State Operation	P_T = 1.5 W, T_C = 100° C t = 1000 hrs. V_{CB} = 40 V

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	SYMBOL	LIMITS		UNITS
				Min.	Max.	
	End Points Subgroups (2, 3, 5, 6)					
3036D	Collector Base Cutoff Current	V_{CB} = 30 V, I_E = 0	I_{CBO}		1.0	μA
3001D	Collector Base Breakdown Voltage	V_{BE} = −1.5 V, I_C = 100 μA	BV_{CEV}	80		
3076	DC Forward-Current Transfer Ratio	I_C = 100 mA, V_{CE} = 5 V	h_{FE}	35	325	—

[h] Acceptance/Rejection Criteria of Group B tests: For an LTPD plan of 7% the total sample size is 115 for which the maximum number of rejects allowed is 4. Acceptance is also subject to a maximum of one (1) reject per Sub-group. Group B tests are performed on each lot for Qualification or Lot Acceptance.

[i] Pulsed through an inductor (25 mH); duty factor = 50%.

[k] Measured at a current where the breakdown voltage is a minimum.

TYPICAL CLASS A-SERVICE OPERATION, 50 MHz NEUTRALIZED

DISSIPATION DERATING CURVE

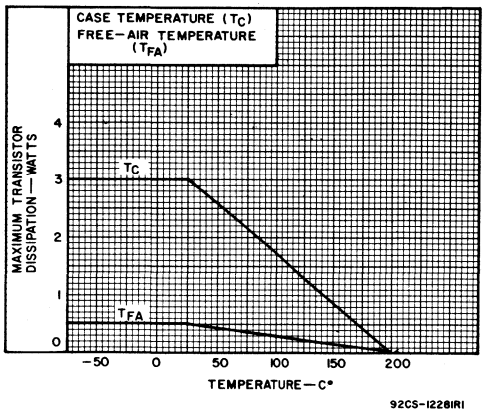
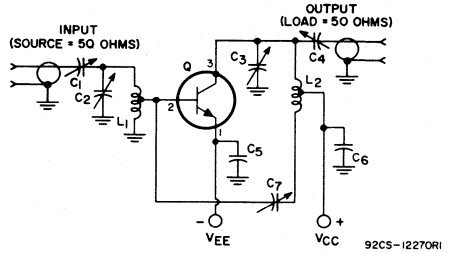


Fig. 4



C_1: 7–100 pF
C_2: 8–60 pF
C_3: 14–150 pF
C_4: 6–80 pF
C_5, C_6: 0.005 μF
C_7: 0.9–7 pF

L_1: 0.12 μH, 3 turns, No.16 wire, 7/16" ID x 1/4" long, tap at 1 turn from ground
L_2: 0.23 μH, 5 turns, No.16 wire, 7/16" ID x 1/2" long, tap at 3 turns from collector terminal
Q: 4057

Fig. 5

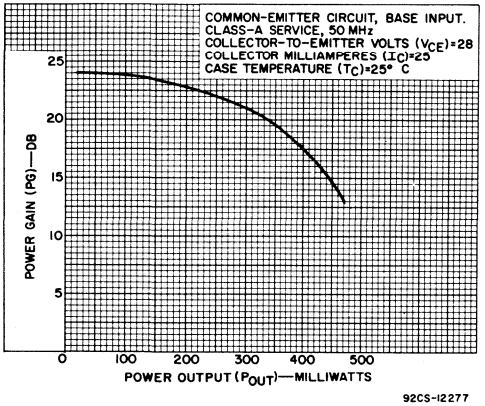


Fig. 6

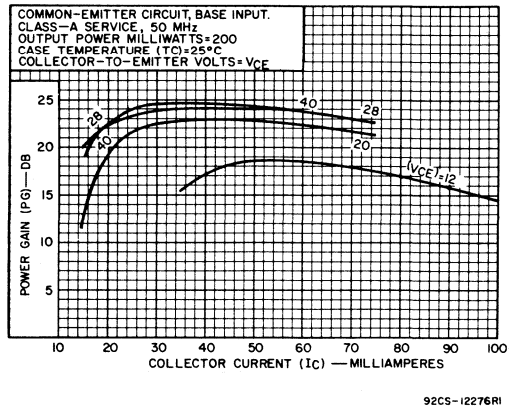


Fig. 7

TYPICAL LARGE-SIGNAL OPERATION, CLASS-C SERVICE, 50 MHz

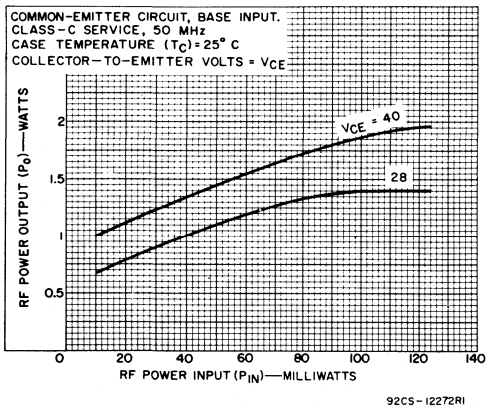
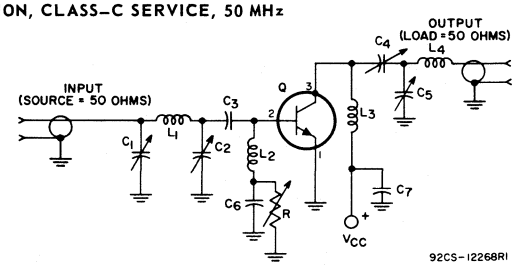


Fig. 8



C_1: 70–350 pF
C_2, C_4, C_5: 7–100 pF
C_3: 0.01 μF
C_6: 0.002 μF
C_7: 0.02 μF
R: 1000 ohms, variable

L_1: 0.13 μH, 4 turns, No.18 wire, 1/4" ID, closely wound
L_2: 2.4 μH, choke, Miller Part No.4606
L_3: 0.6 μH, 10 turns, No.18 wire, 3/8" ID, closely wound
L_4: 0.6 μH, 10 turns, No.18 wire, 3/8" ID, closely wound
Q: 40577

Fig. 9

TYPICAL SMALL-SIGNAL OPERATION CHARACTERISTICS

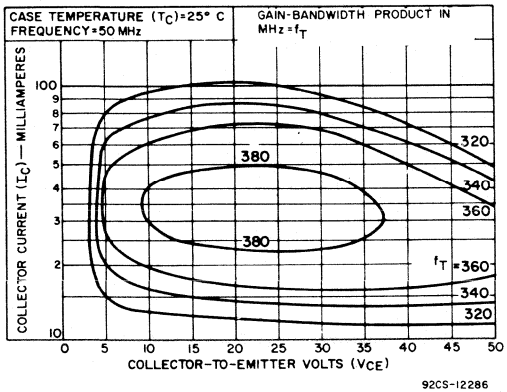


Fig. 10

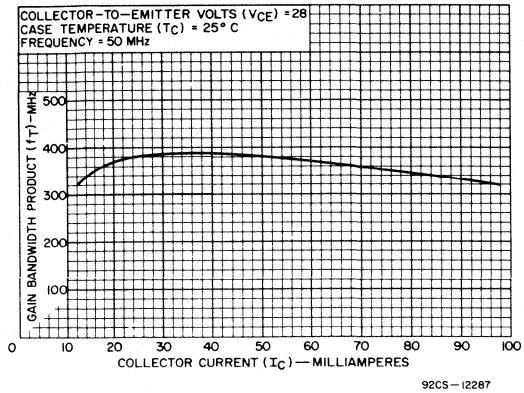


Fig. 11

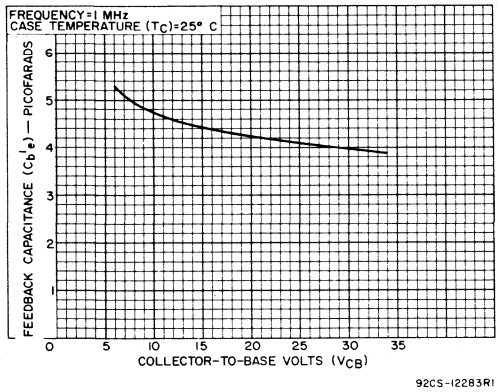


Fig. 12

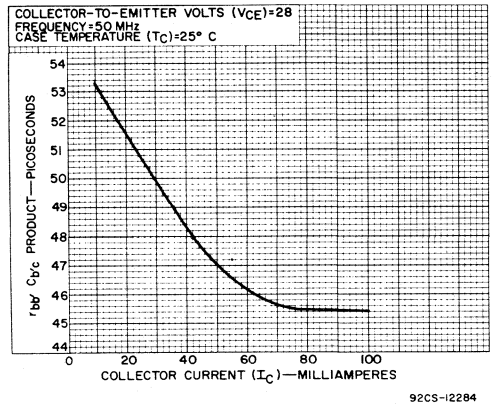


Fig. 13

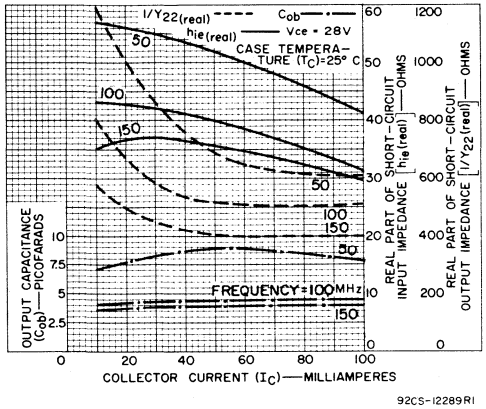


Fig. 14

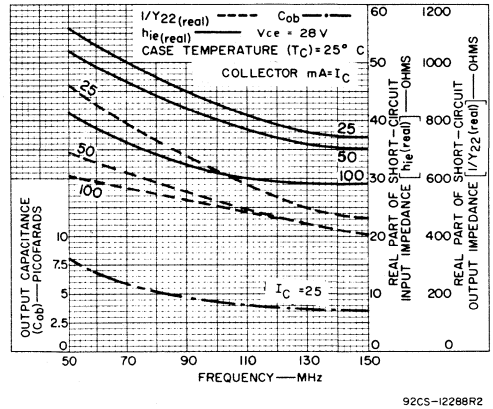
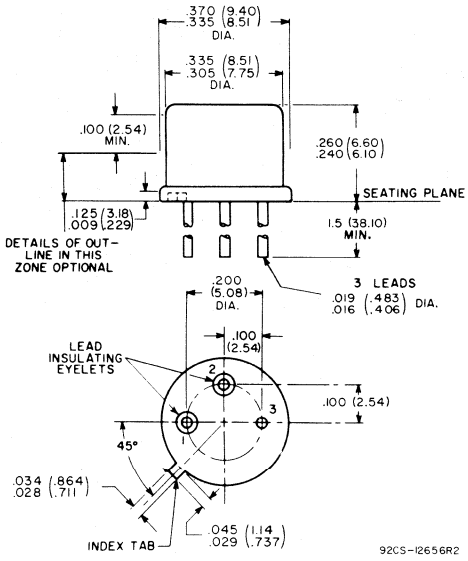


Fig. 15

DIMENSIONAL OUTLINE
JEDEC No.TO-5



Note *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector, Case

RCA
Solid State
Division

RF Power Transistors

40578

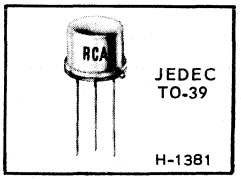
HIGH-RELIABILITY TRANSISTOR

RCA–40578* is a high-reliability variant of the RCA–2N3866, an epitaxial n-p-n planar transistor of "overlay" emitter electrode construction. It is especially processed for high reliability. It is intended for Class A, B, and C amplifier, frequency multiplier, or oscillator operation in high-reliability, driver or predriver stages, VHF-UHF applications in Space, Military, and Industrial communications equipment.

High reliability is assured by eight preconditioning steps, including drift temperature measurements after the High Temperature Reverse Bias and Power Age tests. The 40578 also features complete qualification and lot acceptance testing.

* Formerly RCA–Dev. No. TA7080

High-Gain Device for Class A,B, or C Operation in VHF-UHF Circuits



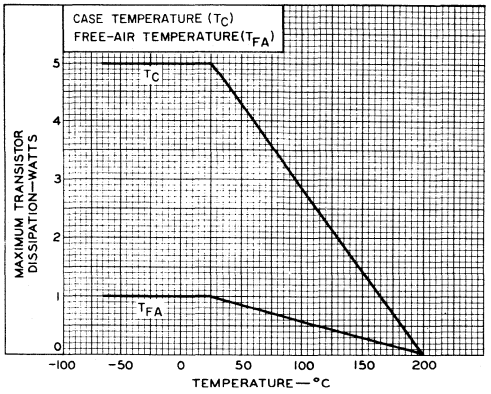
- 8 Preconditioning Steps
- Complete Qualification and Lot Acceptance Testing
- High Power Gain, Unneutralized Class C Amplifier
  - At 400 MHz, 1 W output with 10 dB gain (min.)
  - 250 MHz, 1 W output with 15 dB gain (typ.)
  - 175 MHz, 1 W output with 17 dB gain (typ.)
  - 100 MHz, 1 W output with 20 dB gain (typ.)

RATINGS

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance (R_{BE} = 10 ohms	V_{CER}	55	V
With base open	V_{CEO}	30	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5	V
COLLECTOR CURRENT	I_C	0.4	A
TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 25° C		5	W
At free-air temperatures up to 25° C		1.0	W
At temperatures above 25° C		See *Fig. 1*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≧ 1/32 in. from seating plane for 10 s max.		230	°C

DISSIPATION DERATING CURVE



92CS-10446R3

Fig. 1

ELECTRICAL CHARACTERISTICS

Case Temperature = 25° C

Characteristic	Symbol	TEST CONDITIONS						LIMITS		Units
		DC Collector Volts		DC Base Volts	DC Current (mA)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-Cutoff Current	I_{CEO}		28			0		-	100	nA
Collector-to-Base Breakdown Voltage	BV_{CBO}				0		0.1	55	-	V
Collector-to-Emitter Voltage (Sustaining)	$V_{CER(sus)}$[a]						5	55	-	V
	$V_{CEO(sus)}$					0	5	30	-	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}				0.1		0	3.5	-	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$					20	100	-	1.0	V
Collector-to-Base Capacitance (Measured at 1 MHz)	C_{ob}	30			0			-	3.0	pF
RF Power Output Class-C Amplifier, Unneutralized At 100 MHz At 250 MHz At 400 MHz (See Fig.3)	P_{OUT}		28[b] 28[b] 28[b]					1.8 (typ.)[c] 1.5 (typ.)[d] 1.0[e]		W
Gain-Bandwidth Product	f_T		15				50	800 (typ.)		MHz

[a] With external base-emitter resistance (R_{BE}) = 10 Ω.

[b] V_{CC} value.

[c] For P_{IN} = 0.05 W; minimum efficiency = 60%.

[d] For P_{IN} = 0.1 W; minimum efficiency = 50%.

[e] For P_{IN} = 0.1 W; minimum efficiency = 45%.

POWER OUTPUT vs. FREQUENCY

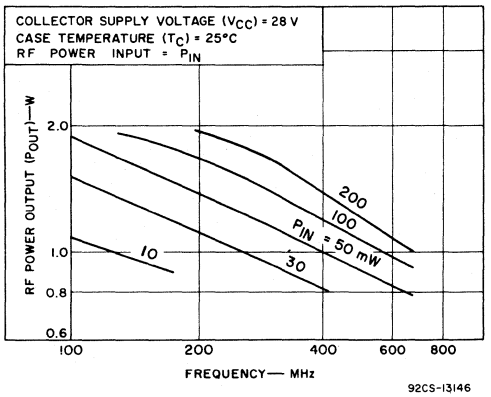
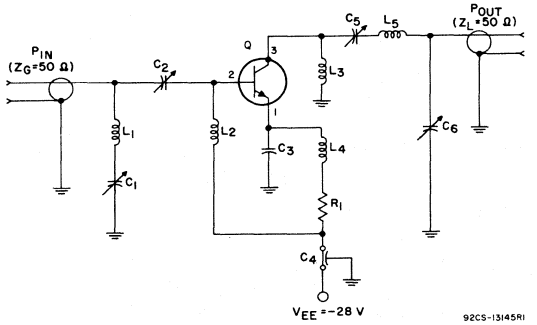


Fig. 2

RF AMPLIFIER CIRCUIT FOR POWER-OUTPUT TEST

(400-MHz Operation)



C1: 3-35 pF
C2, C5: 8-60 pF
C3: 12 pF
C4: 1,000 pF
C6: 0.9-7 pF
L1: 2 turns No.18 wire, 1/4" ID, 1/8" long

L2: Ferrite rf choke, 1 turn, Z = 450 Ω
L3, L4: RF choke, 0.1 μH
L5: 2-1/2 turns, No.18 wire, 1/4" ID, 3/16" long
R1: 5.6 Ω, 1 W
Q: 40578

Fig. 3

RELIABILITY SPECIFICATIONS . . . . . .

In addition to Preconditioning and Group A tests, a Qualification Approval test series (Group B tests) is performed on each lot.

Preconditioning (100 Per Cent Testing of Each Transistor)

1. Serialization
2. Record I_{CEO}, h_{FE}
3. Temperature Cycling-Method 107B Cond. C of MIL-STD-202, 5 cycles, -65^{o} C to 200^{o} C
4. Bake, 72 hours minimum, 200^{o} C
5. Constant Acceleration-Method 2006 of MIL-STD-750, 10,000g, Y_1 and Y_2 axes
6. X-Ray
7. Record I_{CEO}, h_{FE}
8. Reverse Bias Age, $T_A = 200^{o}$ C, $V_{CB} = 50$ V, t = 96 hours
9. [d] Record I_{CEO}, h_{FE}
10. Power Age, $T_A = 25^{o}$ C, $V_{CB} = 28$ V, t = 340 hours, $P_T = 1$ W, free air
11. [d] Record I_{CEO}, h_{FE}, V_{CE} at 340 hours
12. Helium Leak, 1×10^{-7} cc/sec. max.
13. Gross Leak, MIL-STD-202, Method 112
14. Record Subgroups 2 and 3 of Group A Tests

[d] Delta criteria after 96 hours Reverse Bias Age and 340 hours Power Age

ΔI_{CEO}	+100% or +20 nanoamperes whichever is greater
Δh_{FE}	±20%

Definitions

Delta (Δ): Delta shall be determined by subtracting the parameter value measured before application of stress from the value measured after the application of stress.

Group A Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD	SYMBOL	LIMITS Min.	LIMITS Max.	UNITS
	Subgroup 1		10				
2071	Visual and Mechanical Examination	–	–	–	–	–	–
	Subgroup 2		5				
3041D	Collector-Cutoff Current	$V_{CE} = 28$ V	–	I_{CEO}	–	100	nA
3001D	Collector-to-Base Breakdown Voltage	$I_C = 100$ μA	–	BV_{CBO}	55	–	volts
3026D	Emitter-to-Base Breakdown Voltage	$I_E = 100$ μA	–	BV_{EBO}	3.5	–	volts
3011D	Collector-to-Emitter Breakdown Voltage	$I_C = 0$ to 5 mA[f]	–	BV_{CEO}	30[g]	–	volts
3011B	Collector-to-Emitter Breakdown Voltage	$I_C = 0$ to 5 mA[f], $R_{BE} = 10\ \Omega$	–	BV_{CER}	55[g]	–	volts
3071	Collector-to-Emitter Saturation Voltage	$I_C = 100$ mA, $I_B = 20$ mA	–	$V_{CE(sat)}$	–	1	volt
3076	DC Forward-Current Transfer Ratio	$I_C = 100$ mA, $V_{CE} = 5$ V	–	h_{FE}	10	–	–
	Subgroup 3		5				
3236	Output Capacitance	$V_{CB} = 30$ V	–	C_{ob}	–	3.0	pF
3261	Extrapolated Unity Gain Frequency	$I_C = 50$ mA, $V_{CE} = 15$ V, f = 200 MHz	–	f_T	500	–	MHz
See *Fig. 3*	RF Power Output (Min. Eff. = 45%)	$V_{CE} = 28$ V, $P_{IN} = .1$ W, f = 400 MHz	–	P_{OUT}	1.0	–	watts
	Subgroup 4		15				
3036D	Collector-Cutoff Current	$T_A = 150^{o}$ C ± 3° C, $V_{CB} = 30$ V	–	I_{CBO}	–	100	μA
3076	DC Forward-Current Transfer Ratio	$T_A = -55^{o}$ C ± 3° C, $I_C = 100$ mA, $V_{CE} = 5$ V	–	h_{FE}	5	–	–

[f] Pulsed through an inductor (25 μH); duty factor = 50%.
[g] Measured at a current where the breakdown voltage is a minimum.

General Reliability Specifications that are applicable to all rf power transistors are given in booklet RFT-701 and must be used in conjunction with the specific Preconditioning, Group A Tests, and Group B Tests shown below.

Group B Tests

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS
	Subgroup 1	(13 Samples)
2066	Physical Dimensions	
	Subgroup 2	(13 Samples)
2026	Solderability	
1051	Thermal Shock (Temp. Cycling)	Test Condition C
1056	Thermal Shock (Glass Strain)	Test Condition B
2036	Terminal Strength (Tension)	Test Condition A, weight = 5 lbs. time = 15 s each terminal
	Seal (Leak Rate)	Method 112 of MIL-STD-202 Test Cond. C, procedure IIIa, Test Cond. A for gross leaks
1021	Moisture Resistance	10^{-8} cc/s
	Subgroup 3	(13 Samples)
2016	Shock	1,500 g, 0.5 ms, 5 blows each orientation: X_1, Y_1, Z_1, (15 blows total)
2046	Vibration Fatigue	Nonoperating
2056	Vibration Var. Freq.	—
2006	Constant Acceleration	20,000 G Y_1, Y_2
	Subgroup 4	(13 Samples)
2036E	Terminal Strength (Lead Fatigue)	
	Subgroup 5	(13 Samples)
1041	Salt Atmosphere	
	Subgroup 6	(25 Samples)
1031	High Temperature Life (Nonoperating)	$T_{storage}$ = 200° C
	Subgroup 7	(25 Samples)
1026	Steady-State Operation	T_{FA} = 25° C t = 1000 hrs. P_T = 1 W, V_{CB} = 28 V free air, no heat sink

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	SYMBOL	LIMITS Min.	LIMITS Max.	UNITS
	End Points Subgroups (2, 3, 5, 6, 7)					
3041D	Collector-to-Emitter Cutoff Current	V_{CE} = 28 V	I_{CEO}	—	1.0	μA
3011B	Collector-to-Emitter Breakdown Voltage	I_C = 5 mA (Inductive)[i] R_{BE} = 10	BV_{CER}	50[k]	—	volts
See *Fig. 3*	RF Power Output (Min. Eff. = 45%)	V_{CE} = 28 V, P_{IN} = 0.1 W, f = 400 MHz	P_{OUT}	0.95	—	watts
3076	DC Forward-Current Transfer Ratio	I_C = 100 mA V_{CE} = 5 V	h_{FE}	9	—	—
3026D	Emitter-to-Base Breakdown Voltage	I_E = 100 mA	BV_{EBO}	3.0	—	volts

[h] Acceptance/Rejection Criteria of Group B tests: For an LTPD plan of 7% the total sample size is 115 for which the maximum number of rejects allowed is 4. Acceptance is also subject to a maximum of one (1) reject per Sub-group. Group B tests are performed on each lot for Qualification or Lot Acceptance.

[i] Pulsed through an inductor (25 mH); duty factor = 50%.

[k] Measured at a current where the breakdown voltage is a minimum.

GAIN-BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

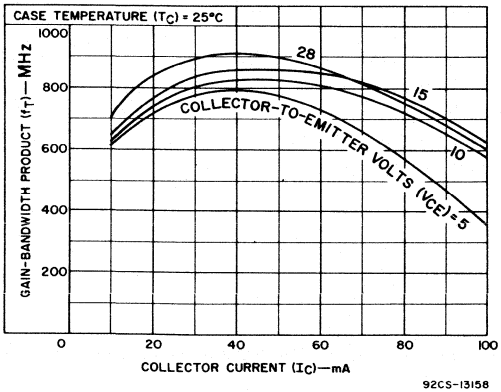


Fig.4

SERIES INPUT RESISTANCE vs. FREQUENCY

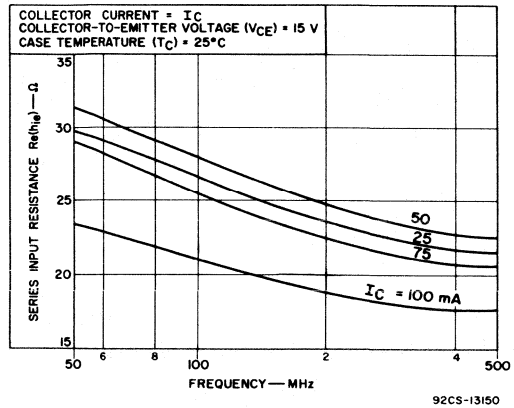


Fig. 5

SERIES INPUT REACTANCE vs. FREQUENCY

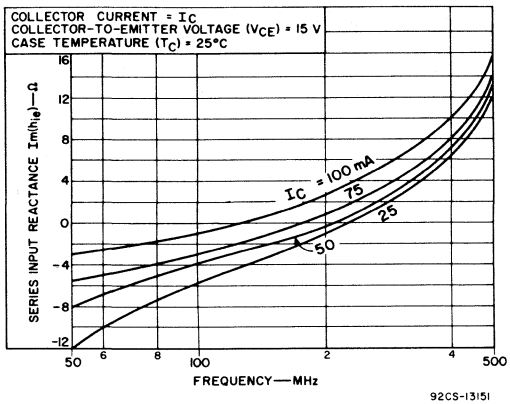


Fig.6

SERIES INPUT RESISTANCE & REACTANCE vs. FREQUENCY

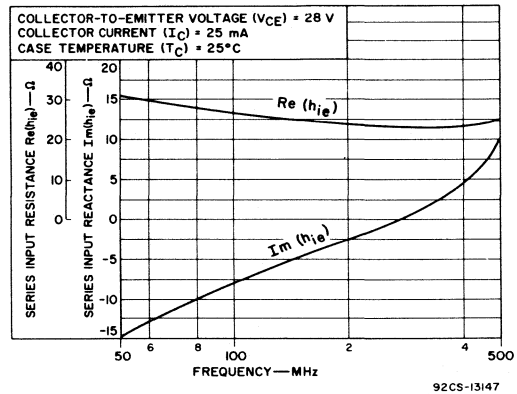


Fig.7

PARALLEL OUTPUT RESISTANCE vs. FREQUENCY

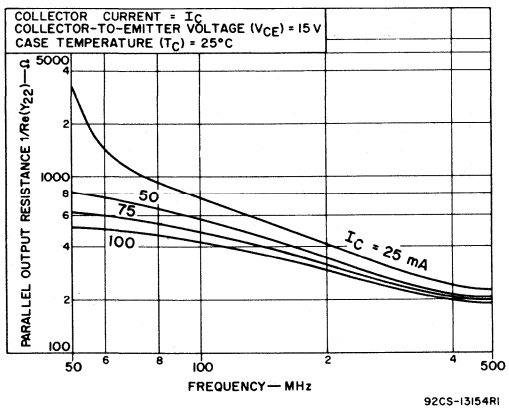


Fig.8

PARALLEL OUTPUT CAPACITANCE vs. FREQUENCY

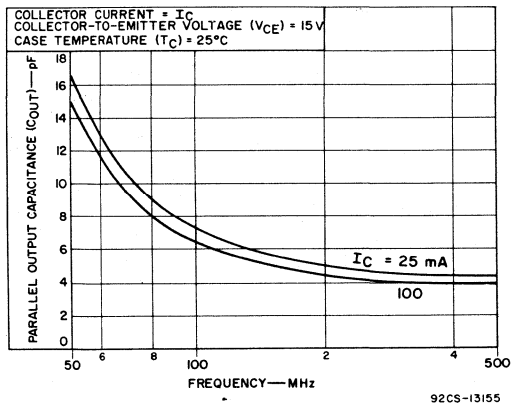


Fig.9

PARALLEL OUTPUT RESISTANCE & CAPACITANCE vs. FREQUENCY

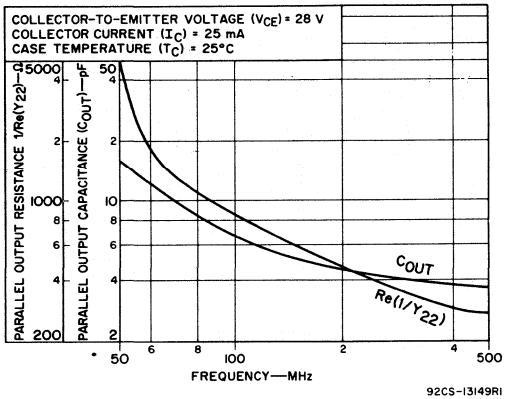


Fig. 10

VARIATION OF COLLECTOR-TO-BASE CAPACITANCE

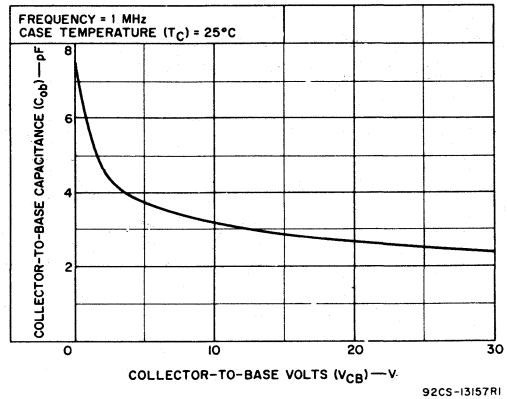
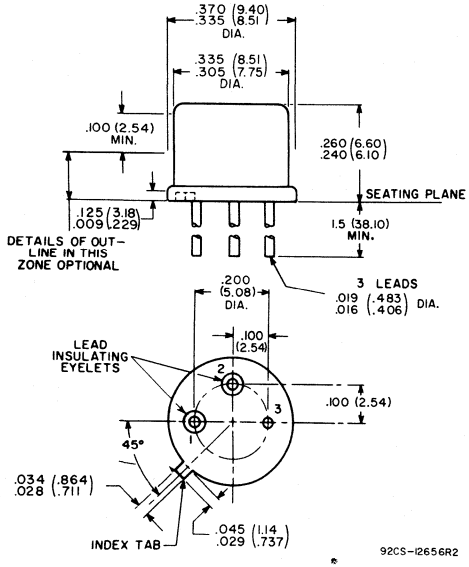


Fig. 11

DIMENSIONAL OUTLINE JEDEC TO-39



DIMENSIONS IN INCHES AND MILLIMETERS

Note: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

TERMINAL CONNECTIONS

Lead No. 1 – Emitter
Lead No. 2 – Base
Case, Lead No. 3 – Collector

RCA
Solid State
Division

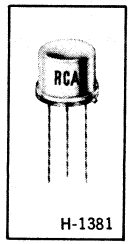
RF Power Transistors

40605

SILICON N-P-N "overlay" TRANSISTOR

"Premium" High-Reliability Type

For Class-A,-B, or -C Service in VHF/UHF Military, Industrial, and Commercial Equipment



JEDEC TO-39

RCA-40605* is an epitaxial silicon n-p-n planar transistor featuring "overlay" emitter electrode construction. It is intended for class-A, -B, or -C amplifier, frequency multiplier, and oscillator service in VHF/UHF equipment.

Premium high-reliability type 40605 is identical to RCA-2N3553 but is preconditioned and tested for use in critical aerospace and industrial equipment.

*Formerly RCA Dev. Type No. TA7361.

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65 V
COLLECTOR-TO-EMITTER VOLTAGE:		
With-1.5 volts (V_{BE}) of reverse bias & external base-to-emitter resistance (R_{BE}) = 33 Ω	V_{CEX}	65 V
With base open	V_{CEO}	40 V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4 V
CONTINUOUS COLLECTOR CURRENT	I_C	0.33 A
PEAK COLLECTOR CURRENT	I_{Cpk}	1 A
TRANSISTOR DISSIPATION:	P_T	
At case temperatures up to 25°C		7 W
At case temperatures above 25°C derate linearly at		0.04 W/°C
At ambient temperatures up to 25°C		1 W
At ambient temperatures above 25°C derate linearly at		5.71 mW/°C
TEMPERATURE RANGE:		
Storage & Operating (Junction)		-65 to +200°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max		230°C

FEATURES:

- **High Power Output**
  - **Class-C Amplifier . . . 2.5-W (min.) at 175 MHz**
  - **Oscillator . . . 1.5-W (typ.) at 500 MHz**

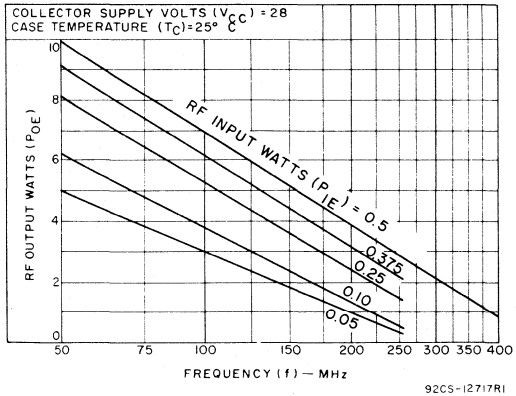


Fig.1 - Typical power output vs. frequency.

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		DC Collector Volts	DC Base Volts	DC Current mA					
		V_{CE}	V_{BE}	I_E	I_B	I_C	MIN.	MAX.	
Collector-Cutoff Current	I_{CEO}	30			0		–	0.1	μA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.3	65	–	V
Collector-to-Emitter Breakdown Voltage: *(See Fig. 2.)* With base open	$V_{(BR)CEO}$				0	200[a]	40[b]	–	V
With base-emitter junction reverse biased & external base-to-emitter resistance (R_{BE}) = 33 Ω	$V_{(BR)CEX}$		−1.5			200[a]	65[b]	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	4	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				50	250	–	1	V

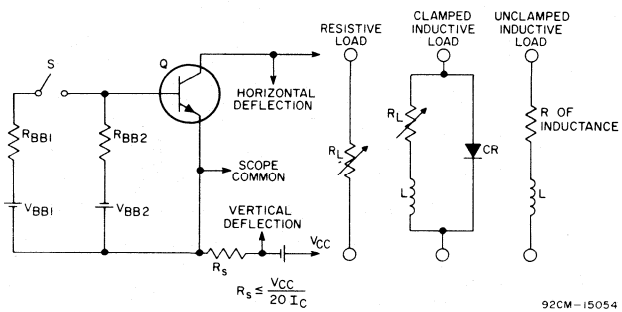
[a] Pulsed through a 25-mH inductor; duty factor = 50%

[b] Measured at a current where the breakdown voltage is a minimum.

DYNAMIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS		UNITS
		DC Collector Supply (V_{CC}) – V	Input Power (P_{IE}) – W	Frequency (f) – MHz	MIN.	TYP.	
Power Output *(See Fig. 3.)*	P_{OE}	28	0.25	175	2.5[c]	–	W
Collector-to-Base Capacitance	C_{obo}	V_{CB} = 30 V, I_C = 0	–	1	–	10	pF
Gain-Bandwidth Product	f_T	V_{CE} = 28 V, I_C = 125 mA	–	–	350	–	MHz

[c] Minimum efficiency = 50%

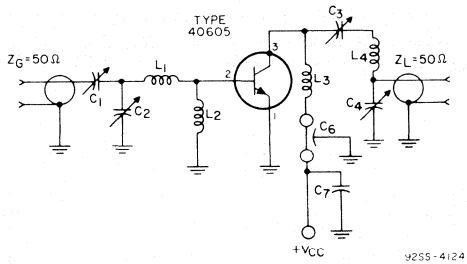


L: 25 mH at 100 mA
R_{BB1}: 150 Ω
R_S: 1 Ω
S: Clare Mercury Relay or equivalent
V_{CC}: 20 V
V_{BB1}: 20 V

$V_{(BR)CEO}$ Measurement	$V_{(BR)CEX}$ Measurement
R_{BB2} = ∞	R_{BB2} = 33 Ω
V_{BB2} = 0	V_{BB2} = - 1.5 V

R of inductance = 83 Ω

Fig.2 - Circuit used to measure voltages $V_{(BR)CEO}$ and $V_{(BR)CEX}$ (unclamped).



C_1, C_2
C_3, C_4: 3-35 pF
C_5: 100 pF, feed-through
C_6: 0.005 μF, disc-ceramic
L_1: 2 turns No. 16 wire, 3/16 in. ID, ¼ in. long
L_2: Ferrite choke, 450 Ω impedance
L_3: 2 turns No. 16 wire, ¼ in. ID, ¼ in. long
L_4: 4 turns No. 16 wire, 3/8 in. ID, 3/8 in. long

Fig.3 - 175 MHz amplifier test circuit for measurement of power output.

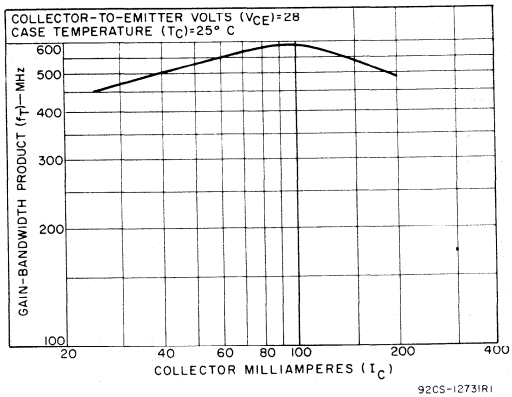


Fig.4 - Typical gain-bandwidth product.

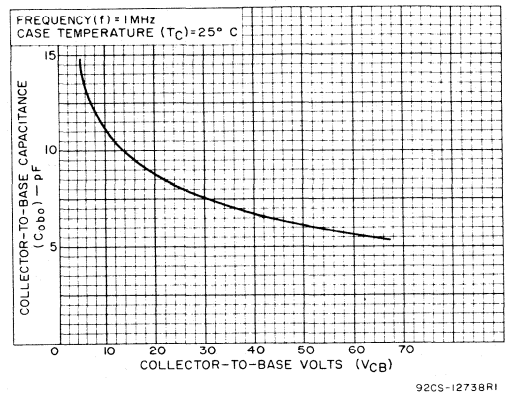


Fig.5 - Typical variation of collector-to-base capacitance.

RELIABILITY SPECIFICATIONS . . .

General Reliability Specifications that are applicable to all rf power transistors are given in booklet RFT-701 and must be used in conjunction with the specific lot screening, Group A Tests, and Group B Tests shown below.

Lot Acceptance Data

Conditioning Screens (100% Testing, see Table I) a) Attributes Data on Burn-In b) Attributes Data on Radiographic Inspection c) Variables Data on Burn-In	
Group A (Lot Sampling, see Table II) a) Variables Data	**Group B** (Lot Sampling, see Table III) a) Attributes Data (From a member of the family)

Table 1. Description of Total Lot Screening – 100% Testing

TEST	CONDITIONS	MIL-STD-750		MIL-STD-202	
		METHOD	CONDITIONS	METHOD	CONDITIONS
1. Lot identification	–	–	–	–	–
2. Pre-seal visual inspection	In accordance with RCA's RFT-701 (See note 1)	–	–	–	–
3. Temp. cycling	5 cycles	1051	C	–	–
4. High Temp. storage	72 hrs. min. at $T_A = 200^0$ C	–	–	–	–
5. Acceleration	20,000 g min.; Y_1 direction only	2006	–	–	–
6. Fine leak	–	–	–	112	C
7. Gross leak	Fluorocarbon bubble test (See note 2)	–	–	–	–
8. Serialize	–	–	–	–	–
9. Pre burn-in electrical	See Table 1 A	–	–	–	–
10. Burn-in	(See note 3)	–	–	–	–
11. Post burn-in electrical	Delta requirements See table 1 A	–	–	–	–
12. Radiographic inspection	–	–	–	–	–

Note 1: Complete title of RFT-701 is: "General Reliability Specifications of RCA RF Power Transistors".

Note 2: Immersed in fluorochemical FC 78 at 65 psig for 4 hrs, unit is than placed in fluorochemical FC 48 at 80^0 C (nominal) and observed for bubbles.

Note 3: Burn-in tests:
Reverse bias age – all transistors shall be operated for 96 hrs at $T_A = 150^0$ C, $V_{CB} = 50$ V
Power age – all transistors shall be operated for 340 hrs at $T_A = 25^0$ C $\pm 3^0$ C, $V_{CB} = 30$ V, $P_T = 1$ W.

Table 1A. Pre Burn-In & Post Burn-In Tests and Delta (Δ) Limits

TEST	SYMBOL	MIL-STD-750		LIMITS		UNITS
		METHOD	CONDITIONS	MIN.	MAX.	
Collector-Cutoff Current	I_{CEO}	3041	V_{CE} = 30 V, bias cond. D	–	0.1	μA
DC Forward-Current Transfer Ratio	h_{FE}	3076	V_{CE} = 5 V, I_C = 150 mA pulsed	15	150	–

Delta (Δ) Limits:

I_{CEO} and h_{FE} of Table 1A shall be retested after each burn-in test and the data recorded for all devices in the lot. The tests measured shall not have changed during each burn-in test from the initial value by more than the specified amount as follows:

$\Delta I_{CEO} = \pm 100\%$ or 10 nA, whichever is greater
$\Delta h_{FE} = \pm 20\%$

All transistors that exceed the delta (Δ) limits or the limits of Table 1A after each burn-in test shall be removed from the lot and the quantity removed shall be recorded in the lot history.

Table II. Group A Electrical Sampling Inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD	SYMBOL	LIMITS		UNITS
	METHOD	CONDITIONS			MIN.	MAX.	
Subgroup 1			10				
Visual and Mechanical Examination	2071	–	–	–	–	–	–
Subgroup 2			5				
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	100	nA
Collector-to-Base Breakdown Voltage	3001D	I_C = 0.3 mA	–	$V_{(BR)CBO}$	65	–	V
Emitter-to-Base Breakdown Voltage	3026D	I_E = 0.1 mA	–	$V_{(BR)EBO}$	4	–	V
Collector-to-Emitter Breakdown Voltage	3011D See Fig. 2.	I_C = 200 mA[a]	–	$V_{(BR)CEO}$	40[b]	–	V
Collector-to-Emitter Breakdown Voltage	3011B See Fig. 2.	I_C = 200 mA[a], V_{BE} = -1.5 V, R_{BE} = 33 Ω	–	$V_{(BR)CEX}$	65[b]	–	V
Collector-to-Emitter Saturation Voltage	3071	I_C = 250 mA, I_B = 50 mA	–	V_{CE} (sat)	–	1	V
DC Forward-Current Transfer Ratio	3076	I_C = 150 mA, V_{CE} = 5 V	–	h_{FE}	15	150	–
Subgroup 3			5				
Output Capacitance	3236	V_{CB} = 30 V, I_C = 0	–	C_{obo}	–	10	pF
Extrapolated Unity Gain Frequency	3261	I_C = 125 mA, V_{CE} = 28 V, f = 100 MHz	–	f_T	350	–	MHz
RF Power Output (Min. Eff. = 50%)	See Fig. 3.	V_{CE} = 28 V, P_{IE} = 0.25 W, f = 175 MHz	–	P_{OE}	2.5	–	W
Subgroup 4			15				
Collector-Cutoff Current	3036D	T_A = 150° C ± 3° C, V_{CB} = 30 V	–	I_{CBO}	–	100	μA
DC Forward-Current Transfer Ratio	3076	T_A = -55° C ± 3° C, I_C = 150 mA, V_{CE} = 5 V	–	h_{FE}	10	–	–

[a] Pulsed through a 25 mH inductor; duty factor = 50%

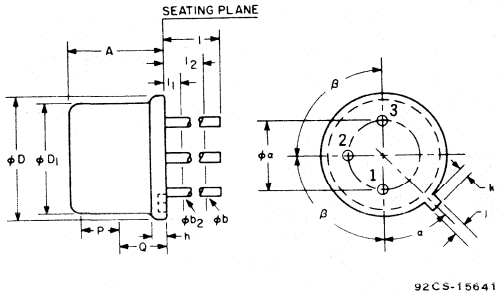
[b] Measured at a current where the breakdown voltage is a minimum

Table III. Group B Environmental Sampling Inspection

EXAMINATION OR TEST	MIL-STD-750 METHOD	MIL-STD-750 CONDITIONS	LTPD	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
Subgroup 1			20				
Physical Dimensions	2066	–		–	–	–	–
Subgroup 2			15				
Solderability	2026	–		–	–	–	–
Thermal Shock (Temp. Cycling)	1051	Test Condition C		–	–	–	–
Thermal Shock (Glass Strain)	1056	Test Condition B		–	–	–	–
Seal (Leak Rate)	–	Method 112 of MIL-STD-202 Test Cond. C, procedure III a For Gross Leaks, Refer to Note 1 in Lot Screening sequence		–	–	1×10^{-7}	atm cc/s
				–	–	–	–
Moisture Resistance	1021	–		–	–	–	–
End Points:							
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0		I_{CEO}	–	100	nA
Collector-to-Emitter Breakdown Voltage	3011D See Fig. 2.	I_C = 200 mA[a]		$V_{(BR)CEO}$	40	–	V
DC Forward-Current Transfer Ratio	3076	I_C = 150 mA, V_{CE} = 5 V		h_{FE}	12	–	–
RF Power Output (Min. Eff = 50%)	See Fig. 3	V_{CE} = 28 V, P_{IE} = 0.25 W, f = 175 MHz		P_{OE}	2.5	–	W
Subgroup 3			15				
Shock	2016	1,500 g, 0.5 ms, 5 blows each orientation: X_1, Y_1, Z_1, Y_2,(15 blows total)		–	–	–	–
Vibration Fatigue	2046	Nonoperating		–	–	–	–
Vibration, Variable Frequency	2056	–		–	–	–	–
Constant Acceleration	2006	20,000 g Y_1, Y_2		–	–	–	–
End Points: (Same as Subgroup 2)							
Subgroup 4			15				
Terminal Strength (Lead Fatigue)	2036E	–		–	–	–	–
Subgroup 5			15				
Salt Atmosphere	1041	–		–	–	–	–
Subgroup 6							
High Temperature Life (Nonoperating)		T_{stg} = + 200° C, t = 1000 hrs.	–	–	–	–	–
End Points:							
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	1	μA
Collector-to-Emitter Breakdown Voltage	3011D See Fig. 2.	I_C = 200 mA[a]	–	$V_{(BR)CEO}$	40	–	V
DC Forward-Current Transfer Ratio	3076	I_C = 150 mA, V_{CE} = 5 V	–	h_{FE}	12	–	–
RF Power Output (Min. Eff. = 50%)	See Fig. 3	V_{CE} = 28 V, P_{IE} = 0.25 W, f = 175 MHz	–	P_{OE}	2.3	–	W

[a] Pulsed through a 25 μH inductor; duty factor = 50%

DIMENSIONAL OUTLINE
JEDEC No.TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	.190	.210	4.83	5.33	
A	.240	.260	6.10	6.60	
ϕb	.016	.021	.406	.533	2
ϕb_2	.016	.019	.406	.483	2
ϕD	.350	.370	8.89	9.40	
ϕD_1	.315	.335	8.00	8.51	
h	.009	.125	.229	3.18	
j	.028	.034	.711	.864	
k	.029	.040	.737	1.02	3
l	.500		12.70		2
l_1		.050		1.27	2
l_2	.250		6.35		2
P	.100		2.54		1
Q					4
α	45^0 NOMINAL				
β	90^0 NOMINAL				

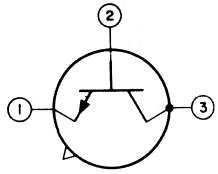
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010 in (.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and .5 in (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond .5 in (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL DIAGRAM



LEAD 1 – EMITTER
LEAD 2 – BASE
CASE, LEAD 3 – COLLECTOR

RCA
Solid State
Division

RF Power Transistors

40606

JEDEC TO-60 H-1307

High-Reliability Silicon N-P-N Overlay Transistor

For Large-Signal, High-Power VHF/UHF Applications in Military and Industrial Communications Equipment

Features:

- **High power output, unneutralized class C amplifier**
- **High voltage ratings**
- **100 per cent tested to assure freedom from second breakdown for operation in class A applications**
- **All three electrodes electrically isolated from case for design flexibility**

RCA-40606 is an epitaxial silicon n-p-n planar transistor. This device is intended for class A, B, C amplifier, frequency multiplier, or oscillator operation. The device was developed for vhf/uhf applications.

The transistor employs the overlay concept in emitter-electrode design — an emitter electrode consisting of many microscopic areas connected together through the use of a diffused-grid structure and an overlay of metal which is applied on the silicon wafer by means of a photo-etching technique. This arrangement provides the very high emitter periphery-to-emitter area ratio required for high efficiency at high frequencies.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	65	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base-emitter junction reverse-biased (V_{BE} = -1.5 V)	V_{CEV}	65	V
With base open	V_{CEO}	40	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
COLLECTOR CURRENT	I_C	3	A
TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 25°C		23	W
At case temperatures above 25°C		Derate linearly to 0 watts at 200°C	
TEMPERATURE RANGE:			
Storage and operating (junction)		-65 to 200	°C
TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. (0.8 mm) from insulating wafer for 10 s max. . .		230	°C

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C

Characteristic	Symbol	TEST CONDITIONS						LIMITS		Units
		DC Collector Volts		DC Base Volts	DC Current (Milliamperes)					
		V_{CB}	V_{CE}	V_{BE}	I_E	I_B	I_C	Min.	Max.	
Collector-Cutoff Current	I_{CEO}		30			0		–	0.25	mA
Collector-to-Base Breakdown Voltage	BV_{CBO}				0		0.5	65	–	volts
Collector-to-Emitter Breakdown Voltage	BV_{CEO}					0	0 to 200*	40**	–	volts
	BV_{CEV}			−1.5			0 to 200*	65**	–	volts
Emitter-to-Base Breakdown Voltage	BV_{EBO}				0.25		0	4	–	volts
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					100	500	–	1	volt
Collector-to-Base Capacitance Measured at 1 MHz	C_{ob}	30			0			–	20	pF
RF Power Output Amplifier, Unneutralized At 260 MHz (See Fig. 3) 400 MHz (See Fig. 2)	P_{OE}		V_{CC} = 28 28					14.5 • (typ.) 10 ▲	–	watts
Gain-Bandwidth Product	f_T		28				150	400 (typ.)		MHz
Base-Spreading Resistance Measured at 200 MHz	$r_{bb'}$		28				250	6.5 (typ.)		ohms
Collector-to-Case Capacitance	C_s							–	6	pF
DC Forward-Current Transfer Ratio	h_{FE}		5				300	10	–	
Second-Breakdown Collector Current[a] (Base forward-biased)	$I_{S/b}$		28					0.33	–	A

* Pulsed through an inductor (25 mh); duty factor = 50%.
** Measured at a current where the breakdown voltage is a minimum.
• For P_{IE} = 4.0 w; minimum efficiency = 60%.
▲ For P_{IE} = 4.0 w; minimum efficiency = 45%.
[a] Pulse duration = 1 s.

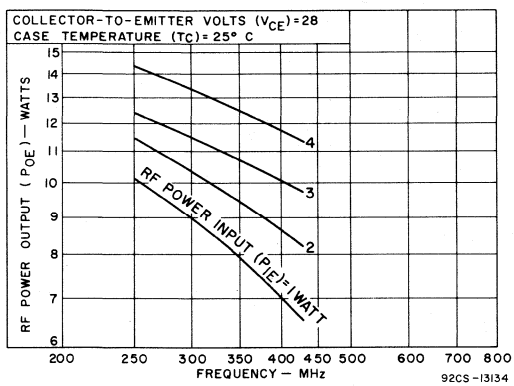
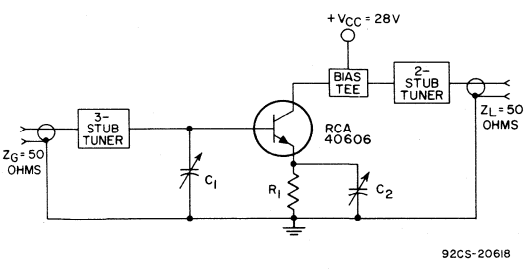
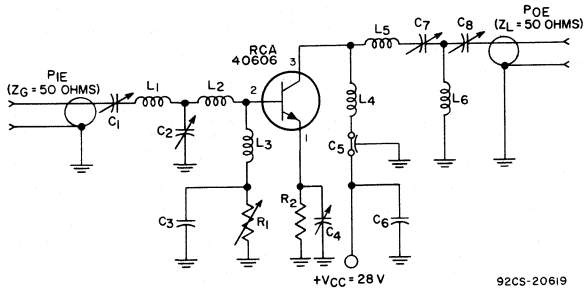


Fig.1—Power output vs. frequency.



C_1, C_2: 7.8–17 pF R_1: 0.56 ohm

Fig.2—RF amplifier circuit for power-output test at 400 MHz.



C_1: 3–35 pF
C_2, C_4, C_8: 8–60 pF
C_3, C_6: 0.005 μF disc ceramic
C_5: 1,000 pF
C_6: 1.5–20 pF
L_1: 3 turns No.18 wire, 1/4 in. (6.35 mm) ID, 1/4 in. (6.35 mm) long
L_2: 3/16 in. (4.76 mm) wide copper strip, 3/8 in. (9.52 mm) long
L_3: Ferrite choke, Z = 450 ohms
L_4: RF choke, 0.47 μH
L_5: 3–1/2 turns No. 16 wire, 1/4 in. (6.35 mm) ID, 7/16 in. (11.11 mm) long
L_6: 1 turn No.16 wire, 1/4 in. (6.35 mm) ID, 3/8 in. (9.52 mm) long
R_1: 50 ohms
R_2: 0.56 ohms

Fig.3–RF amplifier circuit for power-output test at 260 MHz.

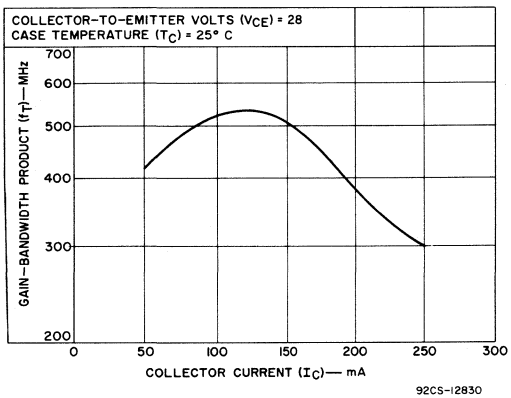


Fig.4–Gain-bandwidth product vs. collector current.

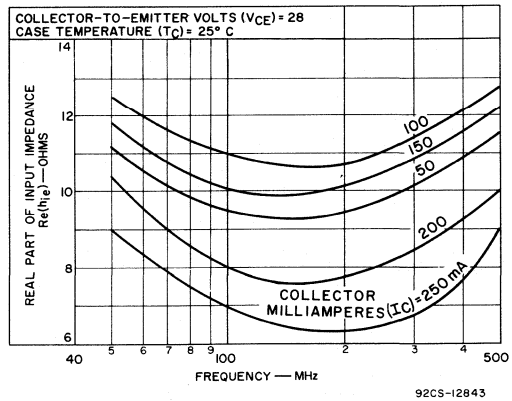


Fig.5–Series input resistance vs. frequency.

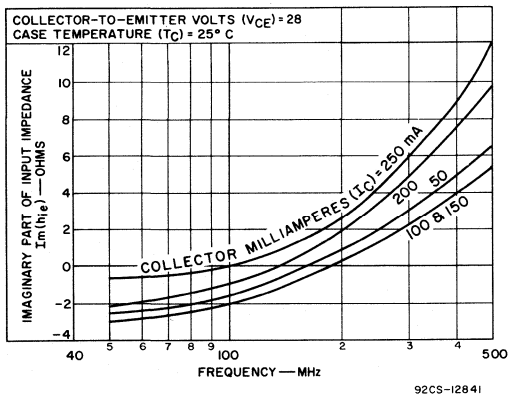


Fig.6–Series input reactance vs. frequency.

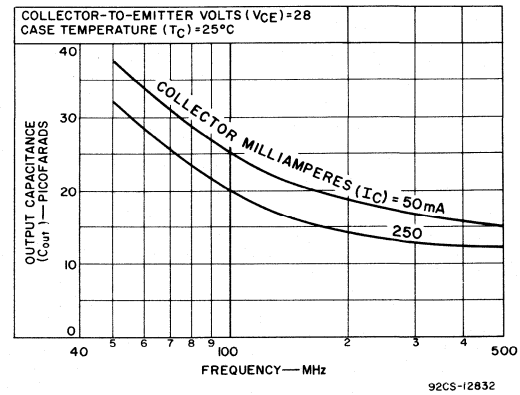


Fig.7–Output capacitance vs. frequency.

RELIABILITY SPECIFICATIONS:

Lot Acceptance Data

Conditioning Screens (100% Testing, see Table I) (a) Attributes Data on Burn-In	(b) Attributes Data on Radiographic Inspection	(c) Variables Data on Burn-In
Group A (Lot Sampling, see Table II) (a) Variables Data	**Group B** (Lot Sampling, see Table III) (a) Attributes Data (From a member of the family)	

Table 1. Description of Total Lot Screening — 100% Testing

TEST	CONDITIONS	MIL-STD-750		LIMITS		UNITS
		METHOD	CONDITIONS	MIN.	MAX.	
1. Read: Collector-to-Emitter Current DC Forward-Current Transfer Ratio	V_{CE} = 30 V, I_B = 0 I_C = 300 mA, V_{CE} = 5 V	– –	– –	– 10	250 –	nA
2. Temp. Cycling	5 cycles, −65°C to +200°C	1051C	–	–	–	
3. High-Temp. Storage	T_A = 200°C, t = 72 hrs.	–	–	–	–	
4. Acceleration	20,000 g; Y_1, Y_2	2006	–	–	–	
5. Helium Leak		–	–	–	–	
6. Gross Leak	Ethylene Glycol, Temp. = 150°C, t = 15 s min.	–	–	–	–	
7. Serialization		–	–	–	–	
8. Radiographic Inspection		–	–	–	–	
9. Read and Record: Collector-to-Emitter Current DC Forward-Current Transfer Ratio	V_{CE} = 30 V, I_B = 0 I_C = 300 mA, V_{CE} = 5 V	– –	– –	– 10	250 –	nA
10. Reverse-Bias Age	T_A = 150°C, V_{CB} = 50 V, t = 96 hrs.	–	–	–	–	
11. Read and Record Reverse-Bias End Points	See Table 1A.	–	–	–	–	
12. Power Age	T_A = 25°C, V_{CB} = 30 V, t = 340 hrs. P_D = 2.6 W free air Interim down period = 168 hrs.	–	–	–	–	
13. Read and Record Power-Age End Points	See Table 1A.	–	–	–	–	
14. Read and Record Subgroups 2, 3 of Group A; Sample Subgroup 4 of Group A		–	–	–	–	

Table 1A. Power Age and Reverse-Bias Age

TEST	SYMBOL	MIL-STD-750		LIMITS		UNITS
		METHOD	CONDITIONS	MIN.	MAX.	
Collector-Cutoff Current	I_{CEO}	3041	V_{CE} = 30 V, I_B = 0	–	250	nA
DC Forward-Current Transfer Ratio	h_{FE}	3076	V_{CE} = 5 V, I_C = 300 mA pulsed	10	–	–

Delta (Δ) Limits:

I_{CEO} and h_{FE} of Table 1A shall be retested after each burn-in test and the data recorded for all devices in the lot. The tests measured shall not have changed during each burn-in test from the initial value by more than the specified amount as follows:

ΔI_{CEO} = ± 100% or 25 nA, whichever is greater
Δh_{FE} = ± 20%

All transistors that exceed the delta (Δ) limits or the limits of Table 1A after each burn-in test shall be removed from the lot and the quantity removed shall be recorded in the lot history.

Table II. Group A Electrical Sampling Inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD	SYMBOL	LIMITS		UNITS
	METHOD	CONDITIONS			MIN.	MAX.	
Subgroup 1			10				
Visual and Mechanical Examination	2071	–	–	–	–	–	–
Subgroup 2			5				
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	250	nA
Collector-to-Base Breakdown Voltage	3001D	I_C = 0.5 mA, I_E = 0	–	$V_{(BR)CBO}$	65	–	V
Emitter-to-Base Breakdown Voltage	3026D	I_E = 0.25 mA, I_C = 0	–	$V_{(BR)EBO}$	4	–	V
Collector-to-Emitter Breakdown Voltage	3011D	I_C = 200 mA[a], I_B = 0	–	$V_{(BR)CEO}$	40[b]	–	V
Collector-to-Emitter Breakdown Voltage	3011A	I_C = 200 mA[a], V_{BE} = -1.5 V, R_{BE} = 33 Ω	–	$V_{(BR)CEV}$	65[b]	–	V
Collector-to-Emitter Saturation Voltage	3071	I_C = 500 mA, I_B = 100 mA	–	V_{CE} (sat)	–	1	V
DC Forward-Current Transfer Ratio	3076	I_C = 300 mA, V_{CE} = 5 V	–	h_{FE}	10	–	–
Second Breakdown Collector Current	–	V_{CE} = 28 V, t = 1 s pulse	–	$I_{S/b}$	0.33	–	A
Subgroup 3			5				
Output Capacitance	3236	V_{CB} = 30 V, I_B = 0	–	C_{obo}	–	20	pF
Common-Emitter, Small-Signal Short Circuit Forward Current Transfer Ratio	–	I_C = 250 mA, V_{CE} = 28 V, f = 100 MHz	–	h_{fe}	2.4	–	–
RF Power Output (Min. Eff. = 45%)	See Fig. 3.	V_{CE} = 28 V, P_{IE} = 4 W, f = 400 MHz	–	P_{OE}	10	–	W
Subgroup 4			15				
Collector-Cutoff Current	3036D	T_A = 150° C ± 3° C, V_{CE} = 30 V	–	I_{CBO}	–	250	μA
DC Forward-Current Transfer Ratio	3076	T_A = -55° C ± 3° C, I_C = 300 mA, V_{CE} = 5 V	–	h_{FE}	10	–	–

[a] Pulsed through a 25 mH inductor; duty factor = 50%

[b] Measured at a current where the breakdown voltage is a minimum

Table III. Group B Environmental Sampling Inspection

EXAMINATION OR TEST	MIL-STD-750 METHOD	MIL-STD-750 CONDITIONS	LTPD	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
Subgroup 1			20				
Physical Dimensions	2066	–		–	–	–	–
Subgroup 2			15				
Solderability	2026	–		–	–	–	–
Thermal Shock (Temp. Cycling)	1051	5 cycles −65°C to +200°C		– –	– –	– –	– –
Seal (Leak Rate)	1071			–	–	1×10^{-7}	atm cc/s
Terminal Strength	2036			–	–	–	–
Moisture Resistance	1021	–		–	–	–	–
End Points:							
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0		I_{CEO}	–	250	nA
Collector-to-Emitter Breakdown Voltage	3011D	I_C = 200 mA[a], I_B = 0		$V_{(BR)CEO}$	40	–	V
DC Forward-Current Transfer Ratio	3076	I_C = 300 mA, V_{CE} = 5 V		h_{FE}	10	–	–
RF Power Output (Min. Eff = 45%)	See Fig. 3	V_{CE} = 28 V, P_{IE} = 4 W, f = 400 MHz		P_{OE}	10	–	W
Subgroup 3			15				
Shock	2016	500 g, 1.0 ms, 5 blows each orientation: X_1, Y_1, Z_1, Y_2, (20 blows total)		–	–	–	–
Vibration Fatigue	2046	Nonoperating		–	–	–	–
Vibration, Variable Frequency	2056	–		–	–	–	–
Constant Acceleration	2006	20,000 g Y_1, Y_2		–	–	–	–
End Points:							
(Same as Subgroup 2)							
Subgroup 6							
High Temperature Life (Nonoperating)	1031	T_{stg} = +200° C, t = 1000 hrs.	–	–	–	–	–
End Points:							
Collector-Cutoff Current	3041D	V_{CE} = 30 V, I_B = 0	–	I_{CEO}	–	2.5	μA
Collector-to-Emitter Breakdown Voltage	3011D	I_C = 200 mA[a], I_B = 0	–	$V_{(BR)CEO}$	40	–	V
DC Forward-Current Transfer Ratio	3076	I_C = 300 mA, V_{CE} = 5 V	–	h_{FE}	9	–	–
RF Power Output (Min. Eff. = 45%)		V_{CE} = 28 V, P_{IE} = 4 W, f = 400 MHz	–	P_{OE}	10	–	W
Subgroup 7							
Operating Life							
Steady-State DC	1026	V_{CB} = 28 V, P_D = 4 W, T_A = 170°C	–	–	–	–	
End Points:							
(Same as Subgroup 6)							

[a] Pulsed through a 25 μH inductor; duty factor = 50%

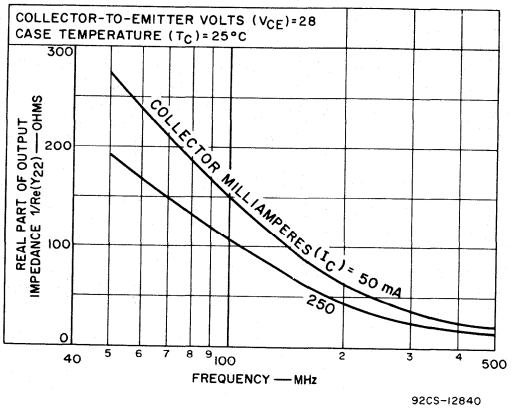


Fig.8—Output resistance vs. frequency.

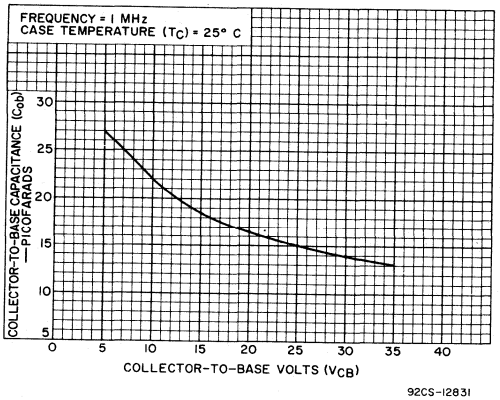
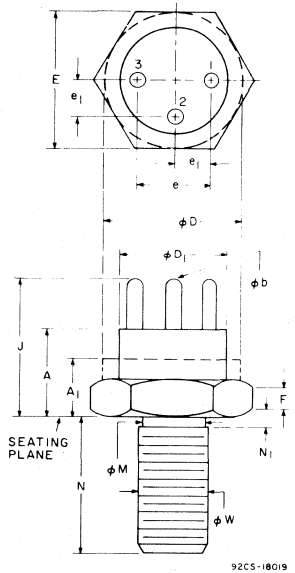


Fig.9—Variation of collector-to-base capacitance.

DIMENSIONAL OUTLINE JEDEC TO-60



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.215	0.320	5.46	8.13	
A_1	—	0.165	—	4.19	2
ϕb	0.030	0.046	0.762	1.17	4
ϕD	0.360	0.437	9.14	11.10	2
$ϕD_1$	0.320	0.360	8.13	9.14	
E	0.424	0.437	10.77	11.10	
e	0.185	0.215	4.70	5.46	
e_1	0.090	0.110	2.29	2.79	
F	0.090	0.135	2.29	3.43	1
J	0.355	0.480	9.02	12.19	
ϕM	0.163	0.189	4.14	4.80	
N	0.375	0.455	9.53	11.56	
N_1	—	0.078	—	1.98	
ϕW	0.1658	0.1697	4.212	4.310	3, 5

NOTES:

1. Dimension does not include sealing flanges
2. Package contour optional within dimensions specified
3. Pitch diameter — 10-32 UNF 2A thread (coated)
4. Pin spacing perimts insertion in any socket having a pin-circle diameter of 0.200 in. (5.08 mm) and contacts which will accommodate pins with a diameter of 0.030 in. (0.762 mm) min., 0.046 in. (1.17mm) max.
5. The torque applied to a 10-32 hex nut assembled on the thread during installation should not exceed 12 inch-pounds.

TERMINAL CONNECTIONS

Mounting Stud, Case, Pin No. 1 — Emitter
Pin No. 2 — Base
Pin No. 3 — Collector

High-Reliability Integrated Circuits

High-Reliability Integrated Circuits

RCA offers high-reliability versions of a broad range of standard COS/MOS and linear integrated circuits that are processed in accordance with MIL-STD-883 (Military Standard for Test Methods, Microelectronics). In addition, twenty-seven COS/MOS integrated circuits are currently being "qualified" to meet the requirements of MIL-M-38510 (Military Standard for Microelectronics or Integrated Circuits). RCA plans to qualify a number of its more than 100 standard linear integrated circuits in accordance with MIL-M-38510 in the future.

RCA also offers a broad line of high-reliability integrated-circuit chips for use in hybrid circuits. Standard chips are normally inspected to MIL-STD-883, Method 2010.1, Condition B Visual. Chips subjected to the more critical Condition A Visual inspections and to SEM (scanning-electron-microscope) inspections are also available.

General Considerations

RCA high-reliability integrated circuits are supplied in hermetically sealed packages that are specially engineered and developed to meet the requirements of military, aerospace, and critical industrial applications. Most COS/MOS devices are supplied in either the dual-in-line package shown in Fig. 4-1(a) or the flat pack shown in Fig. 4-1(b). These packages feature a cereamic body with a welded cap. They are light in weight and can safely withstand the thermal shock levels specified by MIL-STD-883, Method 1011, Condition C. The flat pack and dual-in-line package have been in use since 1964, and the excellent reliability exhibited by these packages has been firmly established. Many currently available RCA high-reliability linear integrated circuits are supplied in the TO-5 style package shown in Fig. 4-1(c).

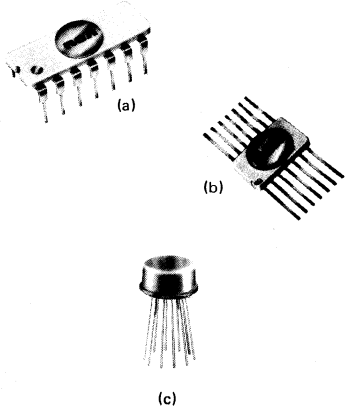


Fig. 4-1– Packages used for RCA high-reliability integrated circuits: (a) dual-in-line ceramic package; (b) ceramic flat pack; (c) TO-5-style package.

For all COS/MOS and many linear integrated circuits, the package in which a particular type is supplied is identified by the letter "D" (dual-in-line ceramic), "K" (ceramic flat pack), or "T" (TO-5 style in the device type-number designation. The charts shown in Figs. 4-2 and 4-3 illustrate how the device type number may be used to define the basic device, the reliability class, the type of package, and the lead finish for RCA high-reliability integrated circuits processed in accordance with MIL-STD-883 or MIL-M-38510, respectively.

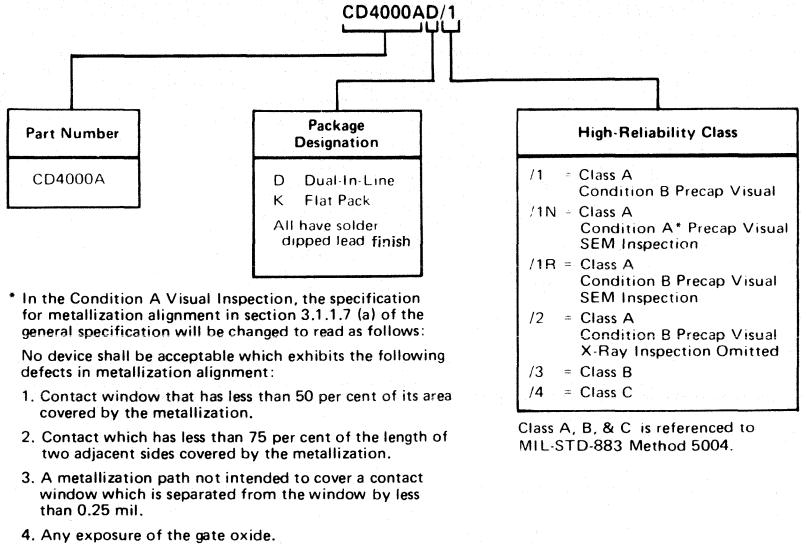
RCA high-reliability integrated-circuit products are currently being used for a broad variety of functions in military, aerospace, and critical industrial applications. Table 4-1 list a few typical examples of the use of RCA high-reliability COS/MOS and linear integrated circuits in satellite and military systems.

Manufacturing Controls

RCA high-reliability integrated circuits are processed in accordance with the Product Assurance Program defined in Appendix A of MIL-M-38510. The program includes the following items:

1. A clearly defined procedure for the conversion of a customer specification into an RCA internal specification with built-in safeguards to assure the customer that the delivered parts meet or exceed his specification requirements.
2. A formalized personnel training and testing program which assures that each operation is performed correctly.
3. A complete inspection of incoming materials, utilities, and work in process using on-site facilities such as scanning-electron-microscope, gas-chromatography, atomic-absorption, and X-ray equipment.
4. Maintenance of cleanliness in work areas, e.g., all critical operations are performed in a Class 100 environment.
5. Rigorous control over changes in design, materials, and processes with documentation kept in active files for a minimum of three years and in inactive files for a minimum of 20 years.
6. Tool and test equipment maintenance and calibration in strict accordance with MIL-C-45662, "Calibration System Requirements".
7. A quality-assurance program in accordance with MIL-Q-9858, "Quality Program Requirements"

Detailed processing and screening requirements for RCA high-reliability integrated circuits are defined subsequently in the discussions of MIL-STD-883 and MIL-M-38510 Requirements.

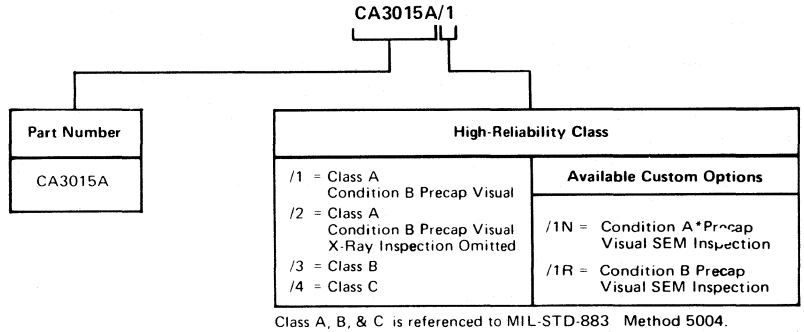


* In the Condition A Visual Inspection, the specification for metallization alignment in section 3.1.1.7 (a) of the general specification will be changed to read as follows:

No device shall be acceptable which exhibits the following defects in metallization alignment:

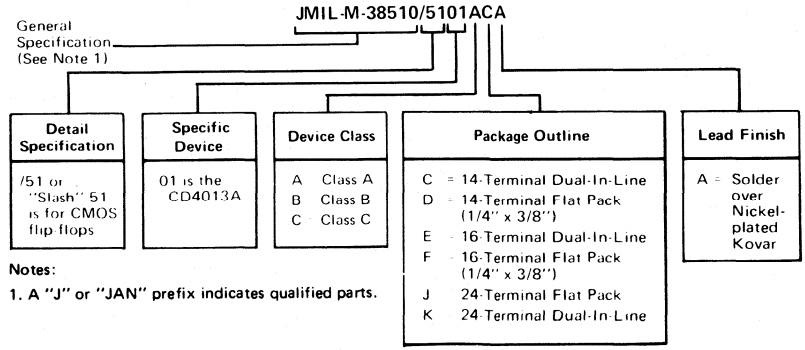
1. Contact window that has less than 50 per cent of its area covered by the metallization.
2. Contact which has less than 75 per cent of the length of two adjacent sides covered by the metallization.
3. A metallization path not intended to cover a contact window which is separated from the window by less than 0.25 mil.
4. Any exposure of the gate oxide.

(a) COS/MOS Integrated Circuits



(b) Linear Integrated Circuits

Fig. 4-2– Guide to the reliability class, package, and lead finish of RCA high-reliability (slash-number series) integrated circuits processed in accordance with MIL-STD-883.



Notes:

1. A "J" or "JAN" prefix indicates qualified parts.

Fig. 4-3– Guide to the reliability class, package, and lead finish of RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-M-38510.

Table 4-1 — A Few Typical Examples of Satellite and Military Applications of RCA High-Reliability Integrated Circuits.

RCA High-Reliability COS/MOS integrated circuits are now being used in, or are being designed into the following systems:	
Satellites	**Military Equipment**
Pioneer F Experimental	Airborne Control
ATS – Series F and G	Data Buoy Platform
NIMBUS	Atmospheric Digital Equipment
HELIOS	F-15 Aircraft Equipment
ITOS	Ground Digital Equipment (Tanks)
HEOS	Oceanographic Digital Equipment
APOLLO-15	Army Digital Equipment
Atmospheric Explorer, AE (Experimenters and Flight-Hardware Usuage, Several Thousand)	Navy Digital Equipment
Classified Satellites	Fuze and Arming Equipment
UK 4 (British/American)	AWAC Program
IMP Satellites	Navy Sonobuoy
Earth Resources Technical Satellite, ERTS	TAC Fire-Control System
Dual Air-Density Satellite (DADS)	PRC-85
	Aircraft Ground Control

RCA High-Reliability Linear Integrated Circuits are now used in, or are being designed into, the following systems:	
Military Communications	**AFGIS Radar (Navy)**
ARC-150	**Missiles**
ARC-164	SAM-D
PRC-85	BULL-DOG
PRC-25	CONDOR
PRC-77	NIKE-X
F-15 Aircraft Equipment	**Other Classified Equipments**

MIL-STD-833 Requirements

RCA Solid State Division offers a broad range of COS/MOS and linear integrated circuits processed and screened in accordance with MIL-STD-883, Method 5004, Class A, B, or C requirements. These devices are used in satellities and other aerospace, military, and critical industrial applications in which maintenance is extremely difficult. RCA high-reliability integrated circuits are provided in four basic screening levels (/1, /2, /3, and /4), as shown in Table 4-2. The basic /1 level has been subdivided to include two higher screening levels (/1N and /1R) as indicated in the table. These levels, which are marked on the device package following the type-number designation, meet the mechanical and electrical screening requirements of MIL-STD-883, is shown in Fig. 4-4. After wafer processing, special visual inspections are performed to MIL-STD-883, Method 2010.1, Condition B or A at both chip and pre-seal inspections to assure a packaged chip of high reliability. In the case of Class A product (RCA levels /1 and /2), parts are tested functionally, and then receive a dc parameter test; significant parameters are recorded.

A 240-hour burn-in at 125°C is performed on all parts. All readings are repeated, and delta shifts calculated. The customer is provided with print-outs of these parameters identified by the serial number on the part. The parts then go through 100-per-cent high- and low-temperature testing under functional and dc operating conditions. Next, 100-per-cent ac testing is accomplished followed by Group A sampling of all test conditions. The Class A product is branded, visually inspected, and retested both functionally and to dc parameters prior to packaging and shipment to the customer. The screening tests for Class B (RCA level /3) and Class C (RCA level /4) devices are reduced as shown in Table 4-3 in which X designates that a test is performed 100 per cent and S indicates that the test is a screen. For Class-B devices, the main difference

Table 4-2 – RCA Integrated-Circuit Screening Levels

RCA Level	MIL-STD-883	Application	Description
	Class A	Aerospace & Missiles	For devices intended for use where maintenance and replacement are extremely difficult or impossible and Reliability is imperative
/1N	Condition A Visual + S.E.M.		
/1R	Condition B Visual + S.E.M.		
/1	Condition B Visual		
/2	Class A (Without Radiographic Inspection)		
/3	Class B	Military & Industrial For example in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive
/4	Class C	Military & Industrial For example, on Ground-Based Electronics	For devices intended for use where replacement can readily be accomplished

imposed before the devices are sealed, and the screening tests required on packaged parts. RCA offers a /2 part which meets Class A requirements of MIL-STD-883 less radiographic inspection since the aluminum metallization and bonding wires do not show up under this inspection.

The product flow for RCA high-reliability integrated circuits processed in accordance with MIL-STD-883

is that burn-in is for 168 hours with GO-NO/GO parameter readings made before and after burn-in. Temperature testing is done on a sampling basis, and visual inspection prior to sealing is not as critical. Class-C devices are tested similarly to Class-B devices less the burn-in, temperature, and ac tests.

product series are 100-per-cent functionally tested at voltage extremes to guarantee 3- and 15-volt operation. Parametric tests are performed at 5 and 10 volts. High and low temperature plus dynamic (ac) testing is performed on high-reliability products.

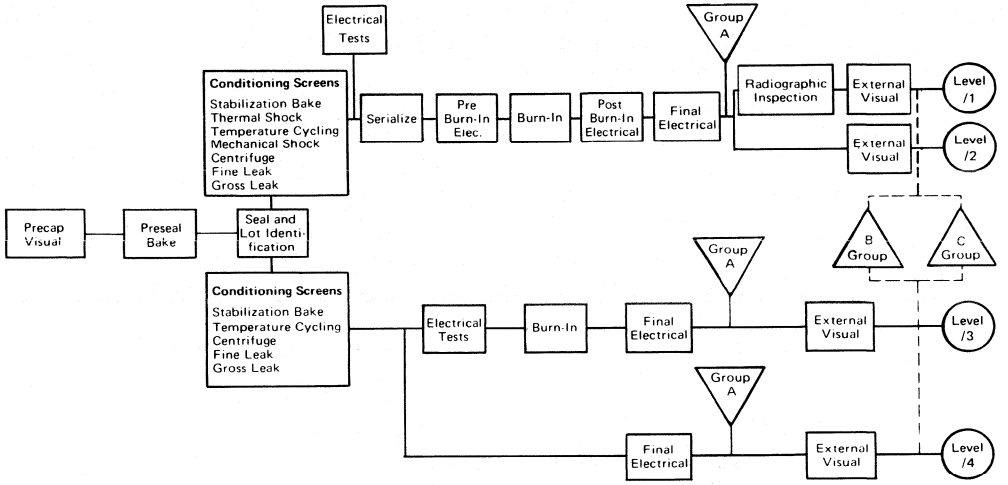


Fig. 4-4– Product flow chart for RCA High-Reliability Integrated circuits processed in accordance with MIL-STD-883.

Table 4-3 – Description of Total Lot Screening

Test	Conditions	MIL-STD-883		Screening Levels					
		Method	Conditions	/1N	/1R	/1	/2	/3	/4
SEM Inspection	–	–	–	X	X	–	–	–	–
Precap Visual	–	2010.1	A	X	–	–	–	–	–
Precap Visual	–	2010.1	B	–	X	X	X	X	X
Preseal Bake	2 hrs. min. at 200°C	–	–	X	X	X	X	X	X
Seal & Lot Identification	–	–	–	X	X	X	X	X	X
Stabilization Bake	48 hrs. at 150°C	1008	C	X	X	X	X	X	X
Thermal Shock	15 cycles	1011	C	X	X	X	X	–	–
Temperature Cycling	10 cycles	1010	C	X	X	X	X	X	X
Mechanical Shock	5 pulses, Y_1 direction	2002	B	X	X	X	X	–	–
Centrifuge	Y_2, Y_1 direction	2001	E	X	X	X	X	–	–
	Y_1 direction only	2001	E	–	–	–	–	X	X
Fine Leak	–	1014	A	X	X	X	X	X	X
Gross Leak	–	1014	C	X	X	X	X	X	X
Electrical Tests	–	–	–	X	X	X	X	X	–
Serialize	–	–	–	X	X	X	X	–	–
Pre Burn-in Electrical	see Table IX	–	–	X	X	X	X	–	–
Burn-in	240 hours	1015	D or E	X	X	X	X	–	–
	168 hours	1015	D or E	–	–	–	–	X	–
Post Burn-in Electrical	Delta Requirements (See Table IX)	–	–	X	X	X	X	–	–
Final Electrical	–	–	–	–	–	–	–	–	–
a) 25°C	see Table VII	–	–	X	X	X	X	X	X
b) -55 and +125°C	see Table VII	–	–	X	X	X	X	X	S
Radiographic Inspection	1 view	2012	–	X	X	X	–	–	–
External Visual	–	2009	–	X	X	X	X	X	X

COS/MOS Integrated Circuits—All RCA high-reliability COS/MOS products are subjected to 100-per-cent production electrical tests after group A, quality testing and branding. Table 4-4 shows the test criteria for all product series. At a temperature of 25°C, all

Table 4-5 presents the group A electrical sampling criteria which are used to retest a portion of the product to assure that the 100-per-cent or other test parameters meet guaranteed limits. The prime factor is LTPD (Lot-Tolerance-Per Cent-Defective); the referenced numbers specify the required sample size. Again, for special

tests of temperature extremes and dynamic (ac) tests, either small quantities are tested, or high-reliability test data are used as judgment information.

Table 4-6 lists pre-burn-in and post-burn-in tests and delta limits for critical device parameters.

Group B and C testing is similar to that of MIL-STD-883 for all COS/MOS product series. The purpose of Group B and C tests is to show quality conformance of the product being manufactured over specific periods of time. Tables 4-7 and 4-8 present the ten subgroup tests referenced to MIL-STD-883, the test conditions, and acceptance criteria for all high-reliability COS/MOS products.

Table 4-4 – All Product Production Testing

Temperature	Test	Test Criteria Hi-Rel levels /1, /2	Hi-rel level /3	Hi-rel level /4
+25°C	Selected static parameters	100%	100%	100%
+125°C	Selected static parameters	100%	100%	–
−55°C	Selected static parameters	100%	100%	–
+25°C	Selected dynamic parameters	100%	100%	–

Table 4-5 – Group-A Electrical-Sampling Inspection

Sub group	Test	Condition	Hi-rel levels /1, /2	LTPD Hi-rel level /3	Hi-rel level /4
1	Selected static parameters	T_A = +25°C	5	5	5
2	Selected static parameters	T_A = +125°C	5	7	10
3	Selected static parameters	T_A = −55°C	5	7	10
4	Selected dynamic parameters	T_A = +25°C	5	5	5

Table 4-6 – Pre- and Post-Burn-in Electrical Tests and Delta Limits (T_A = 25°C) for COS/MOS High-Reliability Integrated Circuits.

CRITICAL PARAMETERS (at V_{DD} = 10 V)	SYMBOLS	LIMIT VALUES: For specific CD4000A Series Types and corresponding Δ limits for High-Reliability Versions (See Note)									
Quiescent Device Current	Total I_L (max)	0.1	0.5	1	2	5	10	15	25	50	Units μA
	ΔI_L	0.05	0.2	0.3	0.5	1.0	1.3	1.5	2.5	5.0	μA
Threshold Voltage "N" Channel	ΔV_{TH}"N"	◄ ±0.3 ►									V
"P" Channel	ΔV_{TH}"P"	◄ ±0.3 ►									V
Device Drain Current: Total	Total $I_{DS(Min)}$	0.1–0.5		0.5–2		2–5		5–10	10–25	25–50	mA
"N" Channel	ΔI_{DS}"N"	±0.1		±0.5		±0.75		±1	±2	±5	mA
"P" Channel	ΔI_{DS}"P"	±0.1		±0.5		±0.75		±1	±2	±5	mA

Note: For example, if a specific CD4000A Series Type has a max. quiescent device current of 0.5 μA at T_A = 25° C, RCA will test to a Δ limit of 0.2 μA for the high-reliability version of that type. In a similar manner, if a type has quiescent device current rating of 5 μA, RCA will test to a Δ limit of 1.0 μA.

Table 4-7 – Group-B Environmental-Sampling Inspection* for COS/MOS High-Reliability Integrated Circuits

Sub group	Test	MIL-STD-883 Ref.	Conditions	Hi-rel levels /1, /2	Hi-rel level /3	LTPD Hi-rel level /4
1	Physical dimensions	2008	Test cond. A per applicable data sheet	10	15	20
2	Marking permanency	2008	Test cond. B per Par. 3.2.1.			4 devices (no failures)
	Visual and mechanical	2008	Test cond. B 10X mag.			1 device (no failures)
	Bond strength	2011	Test cond. D 10 devices minimum	5	15	20
3	Solderability	2003		10	15	15
4	Lead fatigue	2004	Test cond. B2 any 5 leads	10	15	15
	Fine leak	1014	Test cond. A	10	15	15
	Gross leak	1014	Test cond. C			

* Group B tests limited to a production period not to exceed 6 weeks.

Table 4-8 – Group-C Environmental-Sampling Inspection* for COS/MOS High-Reliability Integrated Circuits

Sub group	Test	MIL-STD-883 Ref.	MIL-STD-883 Conditions	Hi-rel levels /1, /2	Hi-rel levels /3	LTPD Hi-rel level /4
1	Thermal shock Temperature cycling Moisture resistance Critical elec. tests	1011 1010 1004	Test cond. C Test cond. C No voltage applied	10	15	15
2	Mechanical shock Vibration, var. freq. Constant accelera-tion critical elec, tests	2002 2007 2001	Test cond. B, 0.5ms Test cond. A Test cond. F	10	15	15
3	Salt atmosphere	1009	Test cond. A omit initial conditioning	10	15	15
4	High temp. storage critical elec. tests	1008	Test cond. C, 1000 hrs	7	15	15
5	Operating life, critical elec. tests	1005	T_A 125°C, 1000 hrs test circuit**	5	5	10
6	Steady-state bias critical elec. tests	1015	Test cond. A, 72 hrs. at T_A 150°C	7		

*Group C tests performed at 3-month intervals.
**Operating-life circuits are included in specific type bulletins.

Linear Integrated Circuits—Table 4-9 is a general guide to parameters that are tested for broad classifications of RCA high-reliability linear integrated circuits.

For RCA levels 1 and 2 (Class A) devices, the Table indicates the typical parameters that are recorded before and after burn-in. A device is rejected for failure to comply with these limits. The column headed MAX Δ shows the maximum change permitted in selected device parameters during burn-in. In installations where replacement is difficult or impossible, any readjustment to components for drifting is equally difficult or impossible.

For RCA level 3 (Class B) devices, only the minimum and/or maximum limits apply for burn-in. No values are recorded, and the tests are go/no-go.

RCA level 4 (Class C) devices are not subjected to burn-in.

Table 4-9 – Pre- and Post-Burn-In Electrical-Test and Delta Limits for RCA High-Reliability Linear Integrated Circuits* (Typical Parameters)

OPERATIONAL AMPLIFIERS

Characteristics	Symbol	Test Conditions	Limits Standard Min.	Limits Standard Max.	Limits Premium Min.	Limits Premium Max.	Limits Premium MaxΔ	Units
Operational Transconductance Amplifiers (Example: CA3080A)								
Input Offset Voltage	V_{IO}	I_{ABC} = 500 mA**	–	5	–	2	±2	mV
Input Offset Current	I_{IO}	I_{ABC} = 500 mA**	–	0.5	–	0.5	±0.05	μA
Input Bias Current	I_I	I_{ABC} = 500 mA**	–	5	–	5	±0.25	μA
Transconductance	gm	I_{ABC} = 500 mA**	6700	13000	7700	12000	±3000	μmho
Operational Voltage Amplifiers (Example: CA3015A)								
Input Offset Voltage	V_{IO}	–	–	5	–	2	±1	mV
Input Offset Current	I_{IO}	–	–	5	–	1.6	±1	μA
Input Bias Current	I_I	–	–	24	–	6	±1	μA
Device Dissipation	P_D	No Load	110	240	110	240	±25	mW
		Output Shorted	320	600	320	600	±50	

DIFFERENTIAL AMPLIFIERS (Example: CA3028B)

Characteristics	Symbol	Limits Min.	Limits Max.	Limits MaxΔ	Units
Input Bias Current	I_I	–	80	±8	μA
Input Offset Voltage	V_{IO}	–	5	±2	mV
Quiescent Operating Current (I_O)	I_6 or I_8	2.5	4	±0.4	mA
Input Current (term. 7)	I_7	1	2.1	±0.2	mA
Device Dissipation	P_D	120	220	±24	mW

Table 4-9 — Pre- and Post-Burn-In Electrical-Test and Delta Limits for RCA High-Reliability Linear Integrated Circuits* (Typical Parameters) (Continued)

DEVICE ARRAYS

Characteristics	Symbol	Test Conditions	Limits Min.	Limits Max.	Max.Δ	Units
Diode Arrays (Example: CA3039)						
Forward Voltage Drop (Any Diode)	V_F	I_F=0.2 ma		720	±10	mV
Forward Voltage Drop (Any Diode)	V_F	I_F=1 ma		780	±10	mV
Forward Voltage Drop (Any Diode)	V_F	I_F=20 ma		950	±10	mV
Transistor Arrays (Example: CA3018 A)						
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μa, I_C = 0	5		±0.5	V
Collector-Cutoff Current	I_{CEO}	V_{CE}=10 V, I_B = 0		0.5	±0.15	μA
Input Current	I_I	I_C=1 ma, V_{CE}=3 V	5	25	±3	μA
Base-to-Emitter Voltage	V_{BE}	I_C = 1 ma, V_{CE} = 3 V	0.6	0.8	±0.10	V

* Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests and delta limits. Level /3 requires pre-burn-in electrical tests only.

** Programming Current

MIL-M-38510 Requirements for High-Reliability COS/MOS Integrated Circuits

Since 1970, RCA has been working closely with various aerospace and military agencies to qualify and provide COS/MOS devices to MIL-M-38510 specifications. Among these agencies are the NASA Goddard Space Flight Center, NASA Marshall Space Flight Center, NASA Headquarters Center in Washington, Rome Air Development Center, and the Defense Electronic Supply Center (DESC) at Dayton, a branch of the Defense Supply Agency.

MIL-M-38510 is the general specification for integrated circuits and the top document for MIL-STD-883. This general specification, introduced a year after MIL-STD-883 was in existence, adds a number of quality constraints not included in MIL-STD-883, which is a specification of test methods, procedures, and screening tests. Parts are provided to MIL-M-38510 under a series of /050 numbers of which nine are in existence. These nine numbers cover twenty-seven COS/MOS types. Parts meet requirements similar to those of Classes A, B, and C of MIL-STD-883, Method 5004 screening, except that additional requirements, including more test conditions and tightened limits, are imposed. The additional criteria for each class of product are designated by an X in Table 4-10. Also provided in MIL-M-38510 tests are PDA's (Per-Cent Defective Allowed) of 10 per cent for the three burn-in operations performed on Class-A product, and 10 per cent for the one burn-in of Class-B product. Table 4-11 provides a list of the COS/MOS devices for which MIL-M-38510 /050-number specification sheets have been written.

Fig. 4-5 shows a product-flow diagram for RCA COS/MOS integrated circuits processed in accordance with MIL-M-38510.

Table 4-12 compares the general processing requirements for COS/MOS integrated circuits of MIL-STD-883 and MIL-M-38510, and Table 4-13 compares the detailed screening requirements of these specifications for Class A COS/MOS integrated circuits.

In the processing of high-reliability COS/MOS integrated circuits, the wafer processing and metallization steps, the wafer finishing operations, and the wafer testing are the same as for standard-product COS/MOS devices. The major difference is that, for Class A parts, an SEM inspection step is inserted after the wafer processing and metallization, as shown in Fig. 4-6. After these four basic operations are completed, the tested wafer is subjected to the special high-reliability processing. As shown in Fig. 4-7, thirty-eight additional processing and screening operations are required for Class A COS/MOS parts.

Table 4-10 – MIL-M-38510 requirements in addition to those of MIL-STD-883

Requirements	Class A	Class B	Class C
Product assurance plan	X	X	X
Manufacturing Certification	X	X	X
Line certification	X		
SEM inspection GSFC-S-311-P 12	X		
Radiographic NHB5300.4(3E)	X		
Two bias burn-in 36 hrs	X		–
Tighter DC electrical	X	X	X
Tighter AC electrical	X	X	X

Table 4-11 – COS/MOS devices for which specification sheets have been written.

Detailed Electrical Specification, MIL-M-38510	Device Covered
MIL-M-38510/050	
01	CD4011A
02	CD4012A
03	CD4023A
MIL-M-38510/051	
01	CD4013A
02	CD4027A
MIL-M-38510/052	
01	CD4000A
02	CD4001A
03	CD4002A
04	CD4025A
MIL-M-38510/053	
01	CD4007A
02	CD4019A
MIL-M-38510/054	
01	CD4008A
MIL-M-38510/055	
01	CD4009A
02	CD4010A
03	CD4049A
04	CD4050A
MIL-M-38510/056	
01	CD4017A
02	CD4018A
03	CD4020A
04	CD4022A
05	CD4024A
MIL-M-38510/057	
01	CD4006A
02	CD4014A
03	CD4015A
04	CD4021A
05	CD4031A
MIL-M-38510/058	
01	CD4016A

No other detailed electrical specifications have been defined by NASA or military agencies at this time. RCA plans to qualify most of the COS/MOS line in the future.

Table 4-12 – Comparison of MIL-STD-883 and MIL-M-38510 Processing and Screening Requirements for RCA High-Reliability COS/MOS Integrated Circuits.

	MIL-STD-883 METHOD	RCA MIL-STD-883 LEVEL						MIL-M-38510 CLASS		
		1N	1R	1	2	3	4	A	B	C
● Wafer										
SEM Inspection	GSFC-S-311-P-12*	X	X	–	–	–	–	X	–	–
● Assembly										
Precap Visual (Cond. A)	2010.1A	X	–	–	–	–	–	X	–	–
Precap Visual (Cond. B)	2010.1B	–	X	X	X	X	X	–	X	X
● Preconditioning										
Thermal Shock	1011C	X	X	X	X	–	–	X	–	–
Temperature Cycle	1010C	X	X	X	X	X	X	X	X	X
Mechanical Shock	2002B	X	X	X	X	–	–	X	–	–
Centrifuge Y1	2001E	–	–	–	–	X	X	–	X	X
Centrifuge Y1 & Y2	2001E	X	X	X	X	–	–	X	–	–
Fine Leak	1014A	X	X	X	X	X	X	X	X	X
Gross Leak	1014C	X	X	X	X	X	X	X	X	X
● Test and Burn-In										
Initial Test		X	X	X	X	X	–	X	X	–
Serialize		X	X	X	X	–	–	X	–	–
Bias Burn-In, Two 36-Hr. Deltas		–	–	–	–	–	–	X	–	–
Operating Burn-In, 240-Hr. Deltas	1015 D,E	X	X	X	X	–	–	X	–	–
Operating Burn-In 168 Hrs.	1015 D,E	–	–	–	–	X	–	–	X	–
Final Electrical DC 25°C		X	X	X	X	X	X	X	X	X
Final Electrical AC 25°C		X	X	X	X	X	S	X	X	S
Final Electrical DC −55°C		X	X	X	X	X	S	X	X	S
Final Electrical AC −55°C		–	–	–	–	–	–	S	S	S
Final Electrical DC +125°C		X	X	X	X	X	S	X	X	S
Final Electrical AC +125°C		–	–	–	–	–	–	S	S	S
● X-ray Inspection										
One View	2012	X	X	X	–	–	–	–	–	–
Two Views	NHB53004(3E)*	–	–	–	–	–	–	X	–	–

S – Sample X = 100% Testing – Not Performed

*These specifications, developed by NASA, are required by MIL-M-38510.

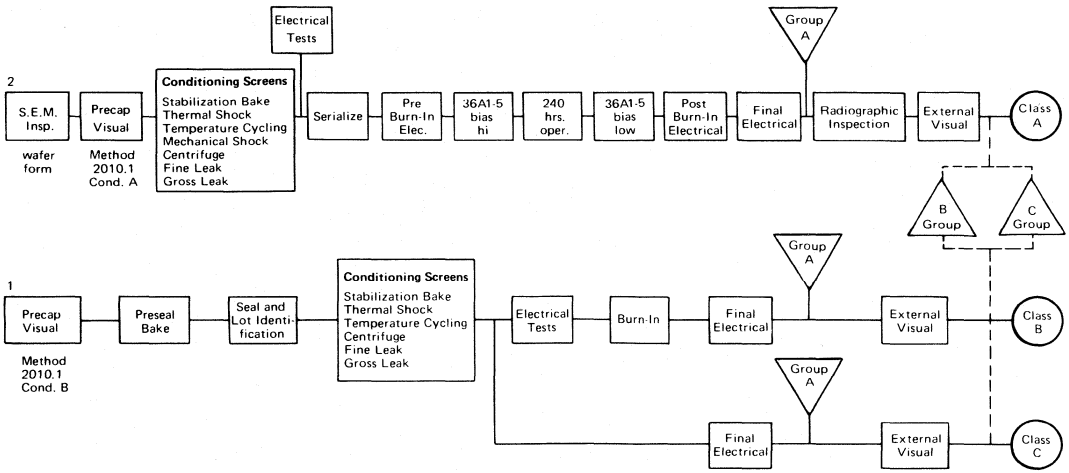


Fig. 4-5– Product flow diagram for RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-M-38510.

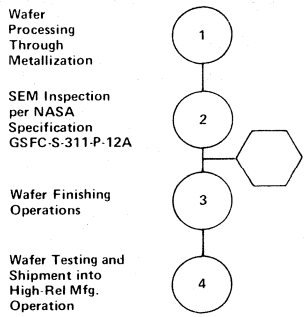


Fig. 4-6– Basic processing operations for high-reliability COS/MOS integrated circuits that require SEM inspection.

Fig. 4-7– COS/MOS High-Reliability Flow Chart for Flat Pack MIL-M-38510 Class A Devices.

Table 4-13 – Comparison of MIL-STD-883 and MIL-M-38510 Detailed Screening Requirements for Class A COS/MOS Devices.

SCREENING PROCEDURES	RCA LEVEL /1N PRESENT MIL-STD-883	CLASS A MIL-M-38510
1. SEM Inspection	Yes	Yes
2. Visual, Precap	2010.1 Cond. A	2010.1 Cond. A
3. Pre-conditioning	MIL-STD-883	MIL-STD-883
4. Bias Burn-in High	None	36 hrs @ 150°C, Δ(2) } PDA(1)
5. Bias Burn-in Low	None	36 hrs @ 150°C, Δ(2) } 5%
6. Operating Burn-in 240 Hrs @ 125°C	Criteria 10% Lot Reject Max; If Exceeded, Repeat Allowed	PDA 5% Max; if over 5% Reject Entire Lot Δ(2)
7. DC Elect. Tests	Measurements on Selected Inputs and Outputs	Measurements on all Inputs and Outputs
8. DC Test-Limit Resolution	50 nA Minimum 10 mV Minimum	1 nA Minimum 1 mV Minimum
9. AC Dynamic Tests	Measurements on Selected Inputs and Outputs	Measurements on all Inputs and Outputs
10. AC Test Limits	At 15-pF Load	At 50-pF Load
11. Radiographic	View in One Dimension	View in Two Dimensions
12. Parts Qualification Requirement		9 Detailed Electrical Specifications
13. Group B Qualification Conformance	10 Generic Families for 50 COS/MOS Types	9 Generic Families for 27 COS/MOS Types

(1) PDA – Per-Cent Defective Allowable
(2) Δ – Delta Variables, Data Required

COS/MOS Life-Test Data

Table 4-14 provides a summary of Group B 125°C operating-life data for 1972 on RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-STD-883. These high-reliability COS/MOS devices were processed to meet RCA level /2 requirements. The data shown, therefore, are representative of the life capability of 1972 shipments of RCA high-reliability COS/MOS integrated circuits.

Table 4-15 shows long-life reliability data for RCA high-reliability COS/MOS integrated circuits that have been operating continuously since 1970 in a ring-counter application that exercises the circuits in a functional mode. The data obtained from this test, which is still underway, indicate the long-term reliability of RCA COS/MOS integrated circuits.

Table 4-14 – Operating-Life Data on RCA High-Reliability COS/MOS Integrated Circuits.

Device Tested:	1,122 from the CD4000A Family	
Specification:	High-reliability per RCA COS/MOS Reliability Report RIC-102 (MIL-STD-883, METHOD 5004)	
Test Hours:	1,000 hours each device * *	
Total Device Hours:	1,055,372 hours	
Inoperable Failures:	Zero	
125°C Failure Rate =	0.086%/1000 hours	At 60% confidence
MTTF =	1,150,000 hours	
55°C Failure Rate * =	0.0126%/1000 hours	At 60% confidence
MTTF =	7,900,000 hours	
25°C Failure Rate =	0.0037%/1000 hours	At 60% confidence
MTTF =	26,800,000 hours	

* Actual tests conducted at 125°C. Failure rates derived for a 55°C operating temperature were obtained using acceleration factors of 6.8 and 23 for the 25°C operating temperature.

Acceleration factors were obtained from Report AD 614103, "Reliability of Integrated Circuits used in Missile Systems", Clearing House for Federal Scientific and Technical Information.

* * 231 units had less than 1000 hours.

Table 4-15 — Long Life Reliability Data on RCA COS/MOS Integrated Circuits (Data obtained from 75 CD4001A integrated circuits tested at 125°C in a ring-counter application.)

Specification:	RCA commercial, full military-temperature range (-55°C to +125°C) per RCA COS/MOS Reliability Report RIC-101A	
Test Hours:	24,000 hours (AS OF MAY 1973)	
Total Device Hours:	1,784,000 hours * *	
Inoperable Failures:	Zero	
125°C Failure Rate =	0.051%/1000 hours	At 60% confidence
MTTF =	1,940,000 hours	
55°C Failure Rate * =	0.0075%/1000 hours	At 60% confidence
MTTF =	13,300,000 hours	
25°C Failure Rate * =	0.0022%/1000 hours	At 60% confidence
MTTF =	46,000,000 hours	

Notes:
* Actual tests conducted at 125°C. Failure rates derived for a 55°C operating temperature were obtained using acceleration factors of 6.8 and 23 for the 25°C operating temperature.

Acceleration factors were obtained from Report AD 614103, "Reliability of Integrated Circuits used in Missile Systems", Clearing House for Federal Scientific and Technical Information.

* * Two parts were destroyed at the 16,000-hour point as a result of operator error. Only 73 parts, therefore, were operated to 24,000 hours.

High-Reliability Terms and Definitions

MIL-STD-883 — Military Standard for Test Methods, Microelectronics. This standard defines the best methods used to achieve three classes of reliability: Class A, Class B, and Class C. This specification defines standard test methods and procedures for high-reliability testing and processing.

Class A (MIL-STD-883) — The highest reliability category or level. RCA levels /1 and /2 follow MIL-STD-883 Class A; level /2 is the same as level /1 with the exception that X-ray inspection is omitted.

Class B (MIL-STD-883) — The intermediate reliability category or level. This class is the most widely used. RCA level /3 corresponds to MIL-STD-883, Class B.

Class C (MIL-STD-883) — The lowest reliability category or level. RCA level /4 follows MIL-STD-883, Class C. Level /4 or Class C parts have no burn-in.

MIL-M-38510 — Military Standard for Microelectronics or Integrated Circuits, first issued in 1969. MIL-M-38510 also defines three classes of reliability, Class A, Class B, and Class C, which are patterned after the MIL-STD-883 format. The MIL-M-38510 requirements differ from the MIL-STD-883 requirements in two significant ways.

MIL-M-38510 has detailed electrical specifications, or "slash sheets"

MIL-M-38510 requires Manufacturer's Certification for Class B and C devices and both Manufacturer's and Line Certification for Class A devices. Although the general specification has been available since 1969, the detailed electrical specifications have just recently been issued for various technologies, including COS/MOS.

The general specification includes basic material, such as definition of classes and general requirements common to all slash sheets.

Slash Sheets Detailed electrical specifications that define exact test conditions and limits. Approved parts are shipped against exact nomenclature specified in the specification. The term slash sheet is derived from the fact that the part number is MIL-M-38510/XXXXX, or "MIL-M-38510 SLASH XXXXX"

Slash sheets must have a governmental sponsor. The COS/MOS sponsor is NASA, who has developed the detailed specifications for nine generic families that include 27 COS/MOS circuits.

Manufacturing Certification (Appendix A) MIL-M-38510 specification requires that the supplier's Product-Assurance Program Requirements are being adhered to. This certification is conducted by DESC (Defense Electronic Supply Center) and is one of the prerequisites for qualification approval.

Line Certification This certification is conducted by NASA to insure that the requirements of NHB 5300.4 (3C) "Line Certification Requirements for Microcircuits" are being adhered to. Line certification is one of the prerequisites for obtaining Class A qualification approval.

QPL (General Definition) Qualified Parts List. High-reliability users often develop a QPL which tells designers within the company which parts are qualified and can be used.

Interim Qualification or Part-II Qual for MIL-M-38510 Before any supplier is fully qualified to supply a part, it is possible to obtain Interim Qualifications. Interim, or Part-II, Qualification is obtained by receiving Manufacturing Certification (and Line Certification for Class A parts) and submitting a sample of tested parts with data. It is not necessary to go through the entire processing and burn-in cycle to obtain Interim Qualification. (RCA has received Part II Qualification for a number of COS/MOS circuits.) When any supplier receives Final Qualification (i.e., submits approved parts that have received the complete processing and testing per the slash sheet), Interim, Part II, Qualification for that part is withdrawn, and only fully qualified parts can be supplied against the specification.

Final Qualification or QPL I for MIL-M-38510 Final Qualification is obtained when all requirements of both the general and detailed specifications are met.

SEM Scanning Electron Microscope. SEM inspection is a requirement for MIL-M-38510 Class A parts. (RCA has SEM facilities at both the Somerville, N.J., and Findlay, Ohio, locations.)

SEM Specification GSFC-S-311-P12 SEM inspection procedure including accept-reject criteria. This specification was written by NASA Goddard Space Flight Center and is the industry standard.

PDA Per-Cent Defective Allowed. If this per cent is exceeded, a lot fails. This term usually applies to burn-in.

Condition B Visual Refers to MIL-STD-883, Method 2010.1, Precap Inspection. Used for RCA 883/1, 2, 3, 4 and MIL-M-38510 Class B and C parts.

Condition A Visual Used for MIL-M-38510, Class A parts. The criteria for metallization, foreign matter, oxide and diffusion faults, and bonding is considerably tighter than Condition B. Condition A Visual is a requirement for MIL-M-38510 Class A parts.

Group A Tests Quality audit of test parameters prior to shipment to the warehouse, in accordance with MIL-STD-883, Method 5005.

Group B Tests These tests are designed to test the mechanical quality of the packaged devices in accordance with

MIL-STD-883, Method 5005. The tests include:

Physical dimensions
Marking permanency
Visual and mechanical
Bond strength
Solderability
Lead fatigue
Hermeticity

Group C Tests These tests are designed to test both the mechanical and electrical characteristics of the packaged device as an indicator of long-term stability. The tests, which are conducted in accordance with MIL-STD-883, Method 5005, include:

Thermal shock
Temperature cycling
Moisture resistance
Mechanical shock
Vibration, variable-frequency
Constant acceleration
Salt atmosphere
High-temperature storage
Operating life test
Steady-state reverse bias

Delta Tests or Limits Refers to specifications that define the maximum shift of key parameters during burn-in.

MTTF or MTBF MTTF — Mean Time to Failure
MTBF — Mean Time between Failure
Both terms are interchangeable and define reliability. Reciprocal of failure rate. Expressed in hours.

LTPD Lot Tolerance Per Cent Defective—sampling-plan term. An LTPD of 5 means that a lot 5-per-cent bad will pass incoming inspection only 10% of the time.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA741/..., CA747/..., CA748/..., CA1558/...

High-Reliability Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers

For Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Input bias current (all types): 500 nA max.**
- **Input offset current (all types): 200 nA max.**

RCA-CA741, CA747, CA748, and CA1558 "Slash" (/) Series types are high-reliability linear integrated circuit High-Gain Single and Dual Operational Amplifiers intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard types described in Data Bulletin File No. 531 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package types CA741, CA747, CA748, and CA1558 can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

Applications:

- **Comparator**
- **DC amplifier**
- **Integrator or differentiator**
- **Multivibrator**
- **Narrow-band or band-pass filter**
- **Summing amplifier**

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on page 5.

The CA741, CA748, and CA1558 Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix) and in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN ("S" suffix). The CA747 is supplied in the 10-lead TO-5 style package ("T" suffix). All the types are also available in chip form ("H" suffix).

RCA TYPE NO.	NO. OF AMPLI.	PHASE COMP.	PACKAGE TYPE	OFFSET VOLT. NULL	A_{OL} (MIN.)	V_{IO} (MAX.)	T_A OPERATING RANGE	COMPATIBLE WITH INDUSTRY TYPE(S)
CA1558T	dual	internal	8-lead TO-5	no	50,000	5 mV	–55 to 125°C	MC1558, S5558
CA741	single	internal	8-lead TO-5	yes	50,000	5 mV	–55 to 125°C	μA741
CA747	dual	internal	10-lead TO-5	no	50,000	5 mV	–55 to 125°C	μA747
CA748	single	external	8-lead TO-5	yes	50,000	5 mV	–55 to 125°C	μA748

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

DC SUPPLY VOLTAGE (between V^+ and V^- terminals):
CA741T, CA747T, CA748T, CA1558T . . . . . 44 V
Differential Input Voltage . . . . . ±30 V
DC Input Voltage* . . . . . ±15 V
Output Short-Circuit Duration . . . . . Indefinite
DEVICE DISSIPATION:
Up to 75°C (CA741T, CA748T) . . . . . 500 mW
Up to 30°C (CA747T) . . . . . 800 mW
Up to 30°C (CA1558T) . . . . . 680 mW

Above Indicated Temperatures . . . . . Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- CA741T . . . . . ±0.5 V
TEMPERATURE RANGE:
Operating . . . . . -55 to +125°C
Storage . . . . . -65 to +150 °C
LEAD TEMPERATURE (During Soldering)
At distance 1/16±1/31 inch (1.59±0.79 mm) from case for 10 seconds max . . . . . 300 °C

*If Supply voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.
▲Voltage values apply for each of the dual operational amplifiers.

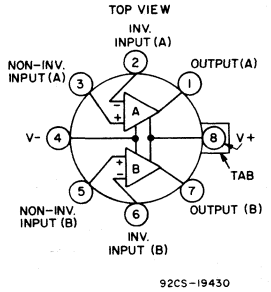


Fig. 1a — Functional diagram of CA1558T with internal phase compensation.

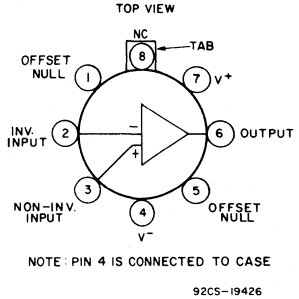


Fig. 1b — Functional diagram of CA741T with internal phase compensation.

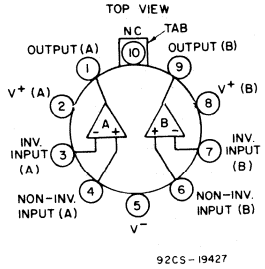


Fig. 1d — Functional diagram of CA747T with internal phase compensation.

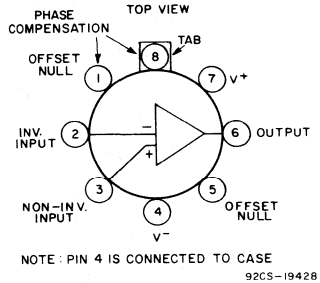


Fig. 1e — Functional diagram of CA748T with external phase compensation

Fig. 1 — Functional diagrams of operational amplifiers.

ELECTRICAL CHARACTERISTICS *at* $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	SUPPLY VOLTS $V^+ = +15$ V, $V^- = -15$ V	TYP.	UNITS
Input Offset Voltage	V_{IO}	$R_S \leq 10$ kΩ	1	mV
Input Offset Current	I_{IO}		20	nA
Input Bias Current	I_{IB}		80	nA
Input Resistance	R_I		2	MΩ
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	200,000	
Common-Mode Input Voltage Range	V_{ICR}		±13	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10$ kΩ	90	dB
Supply Voltage Rejection Ratio	V_{RR}	$R_S \leq 10$ kΩ	30	μV/V
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10$ kΩ	±14	V
		$R_L \geq 2$ kΩ	±13	
Supply Current			1.7	mA
Device Dissipation	P_D		50	mW
Input Capacitance	C_I		1.4	pF
Offset Voltage Adjustment Range			±15	mV
Output Resistance	R_O		75	Ω
Output Short-Circuit Current			25	mA
Transient Response Risetime	t_r	Unity Gain, $V_I = 20$ mV	0.3	μs
Overshoot		$R_L = 2$ kΩ, $C_L \leq 100$ pF	5.0	%
Slew Rate: Closed Loop	SR	$R_L \geq 2$ kΩ	0.5	V/μs
Open Loop▲			40	

*Values apply for each of the dual operational amplifiers.

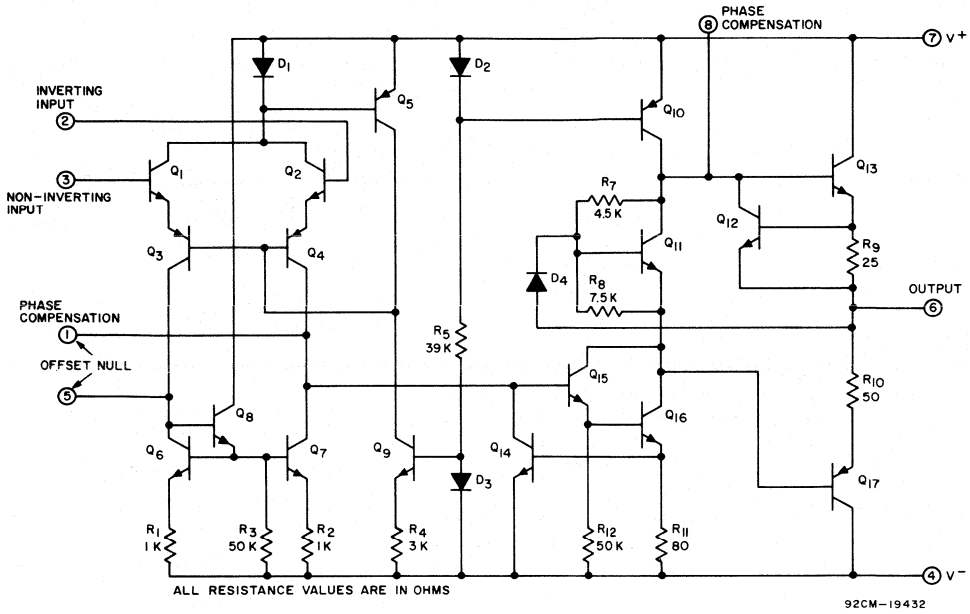


Fig. 2 – Schematic diagram of operational amplifier with external phase compensation for CA748T.

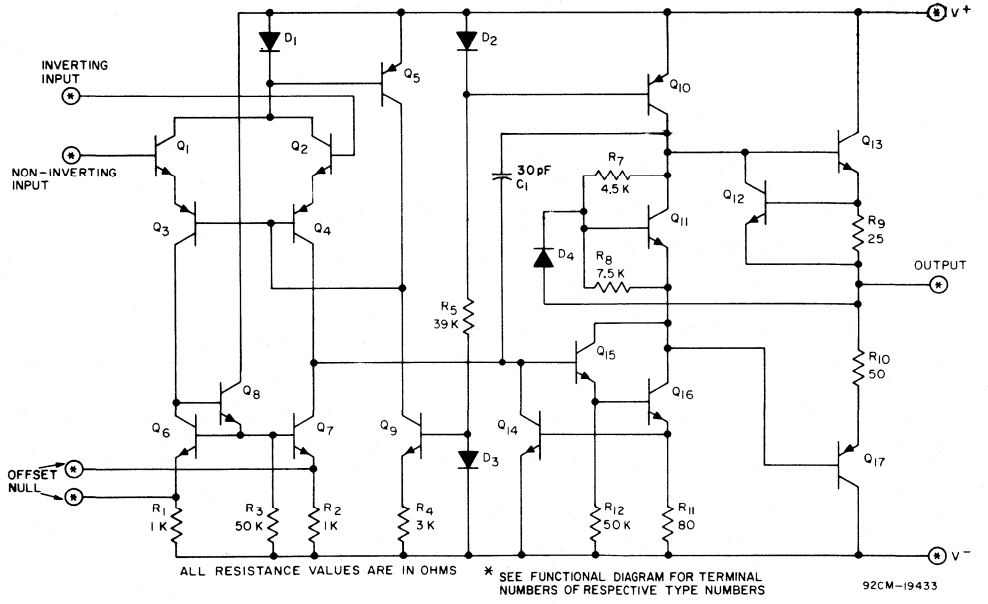


Fig. 3 – Schematic diagram of operational amplifiers with internal phase compensation for CA741T and for each amplifier of the CA748T and CA1558T.

Table I Available Screening Level Options (Indicated by Check (√) Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE TO-5 STYLE: WITH 8 STRAIGHT LEADS (T) SUFFIX	WITH 8 DUAL-IN-LINE FORMED LEADS (DIL-CAN) (S) SUFFIX	WITH 10 STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE					
CA741, CA747, CA748, CA1558	Custom	/1N	√	√	√
		/1R	√	√	√
	Standard Equivalent to MIL-STD-883 Classes A, B,&C	/1	√	√	√
		/2	√	√	√
		/3	√	√	√
		/4	√	√	√
CHIP				*(H) Suffix*	
CA741, CA747, CA748	Custom	/N		√	
		/R		√	
	Standard Chip			√	

Table II Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA741 H/N

CA741 H N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	H= Chip Version	/N For Description, /R R1C-202

Packaged Device, CA741T/1N

CA741 T /1N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	T = TO-5 Style with straight leads S = TO-5 Stylw with Dual-In-Line Formed Leads	/1N /1R For /1 Description, /2 See /3 R1C-202 /4

*Table III Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits** For *All Types*

ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$, $V^+ = +15V$, $V^- = -15$ V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	LIMITS MAX. Δ	UNITS
Input Offset Voltage	V_{IO}		–	5	±1	mV
Input Offset Current	I_{IO}		–	200	±24	nA
Input Bias Current	I_I		–	500	±60	nA
Device Dissipation	P_D			85	±18	mW

*Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig 9.

Table IV ***Final Electrical Tests for All Types***

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +15\ V, V^- = -15\ V$	LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM −55	MINIMUM +25	MINIMUM +125	MAXIMUM −55	MAXIMUM +25	MAXIMUM +125	UNITS
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	6	5	6	mV
Input Offset Current	I_{IO}	–	–	–	–	500	200	200	nA
Input Bias Current	I_I	–	–	–	–	1500	500	500	nA
Device Dissipation	P_D	–	–	–	–	100	85	75	mW
DYNAMIC									
Open-Loop Differential Voltage Gain	A_{OL}	$R_L = 2\ k\Omega, V_O = +10\ V$	25000	50000	25000	–	–	–	

Table V ***Group A. Electrical Sampling Inspection For All Types***

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +15\ V, V = -15\ V$	LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM −55	MINIMUM +25	MINIMUM +125	MAXIMUM −55	MAXIMUM +25	MAXIMUM +125	UNITS
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	6	5	6	mV
Input Offset Current	I_{IO}	–	–	–	–	500	200	200	nA
Input Bias Current	I_I	–	–	–	–	1500	500	500	nA
Supply Current		–	–	–	–	3.8	3.8	2.5	mA
Device Dissipation	P_D	–	–	–	–	100	85	75	mW
DYNAMIC									
Open-Loop Differential Voltage Gain	A_{OL}	–	25000	50000	25000	–	–	–	
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	–	–	200	–	–	–	–	kHz
Common-Mode Rejection Ratio	CMRR	–	70	70	70	–	–	–	dB
Maximum Output-Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$	±12 ±10	±12 ±10	±12 ±10	– –	– –	– –	V
Input Resistance	R_I	–	–	0.3	–	–	–	–	MΩ
Common-Mode Input-Voltage Range	V_{ICR}	–	±12	±12	±12	–	–	–	V

Table VI **Group C Electrical Characteristics Sampling Tests**

$T_A = +25°C$ $V_{CC} = +12\ V$ $V_{EE} = -12V$

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Input Offset Voltage	V_{IO}	–	–	8	mV
Input Offset Current	I_{IO}	–	–	240	μA
Input Bias Current	I_I	–	–	800	μA
Open-Loop Differential Voltage Gain	A_{OL}	f = 1 kHz	33000	–	
Supply Current			–	3	mA

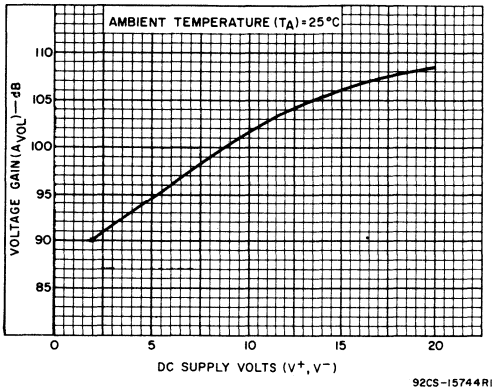


Fig. 4 — Open-loop voltage gain vs. supply voltage for all types.

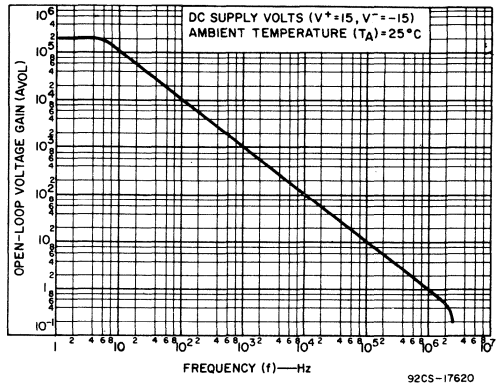


Fig. 5 — Open-loop voltage gain vs. frequency for all types.

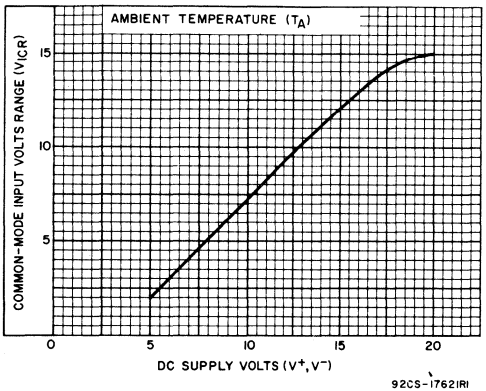


Fig. 6 — Common-mode input voltage range vs. supply voltage for all types.

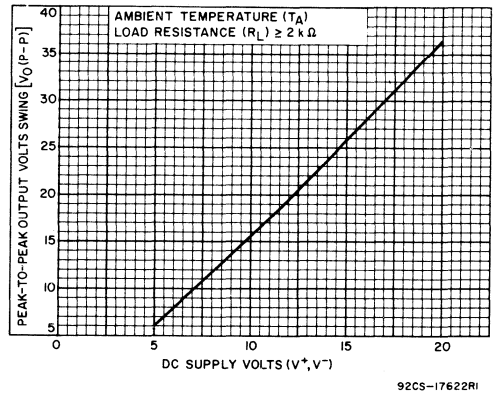


Fig. 7 — Peak-to-peak output voltage vs. supply voltage for all types.

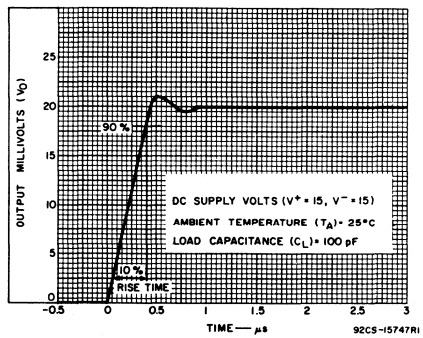


Fig. 8 — Output voltage vs. transient response time for CA 741

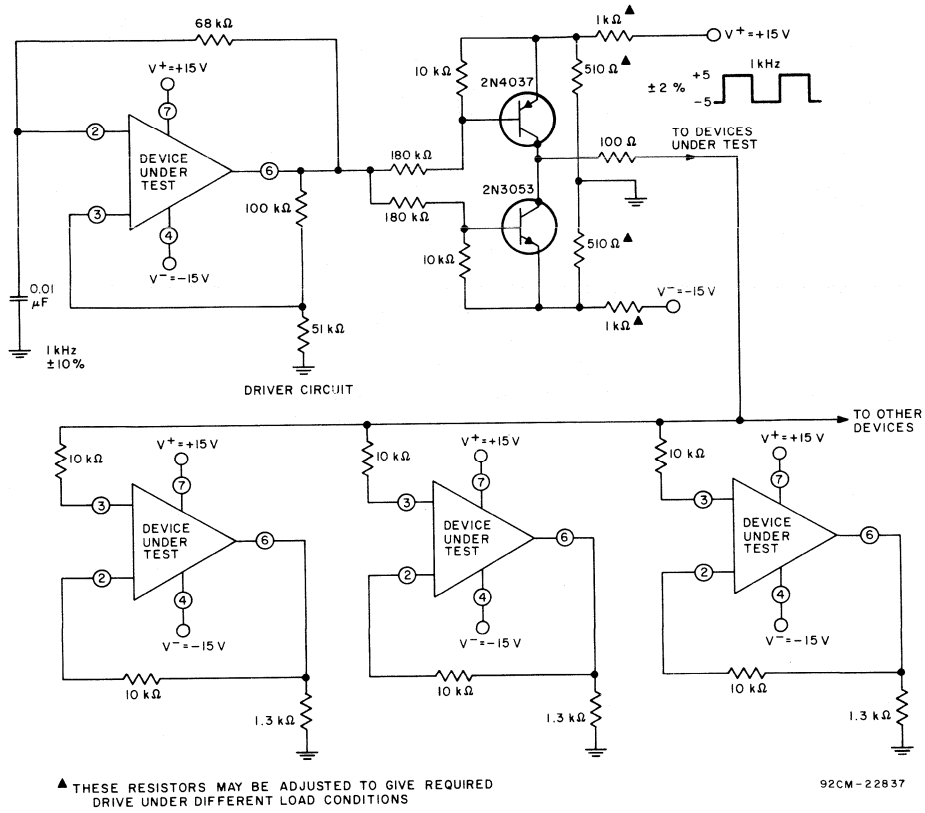


Fig. 9 — Burn-in and operating life test circuit for CA741, CA747, CA748, CA1558.

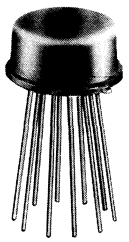
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3000/. . .



H-1528

10-Lead TO-5 Style Package

High-Reliability DC Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Input Impedance** . . . . . **195 KΩ typ.**
- **Voltage Gain** . . . . . **37 dB typ.**
- **Common-Mode Rejection Ratio** . . . . . **98 dB typ.**
- **Input Offset Voltage** . . . . . **1.4 mV typ.**
- **Push-Pull Input and Output**
- **Frequency Capability**
  DC to 30 MHz (with external C and R)
- **Wide AGC Range** . . . . . **90 dB typ.**

RCA-CA3000 "Slash" (/) Series type is a high-reliability linear integrated circuit DC Amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3000 described in Data Bulletin File No. 121 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3000 can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3000 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications

- **Schmitt Trigger**
- **RC-Coupled Feedback Amplifier**
- **Mixer**
- **Comparator**
- **Modulator**
- **Crystal Oscillator**
- **Sense Amplifier**
- **See Companion Application Note ICAN-5030 "Applications of RCA-CA3000 IC DC Amplifier."**

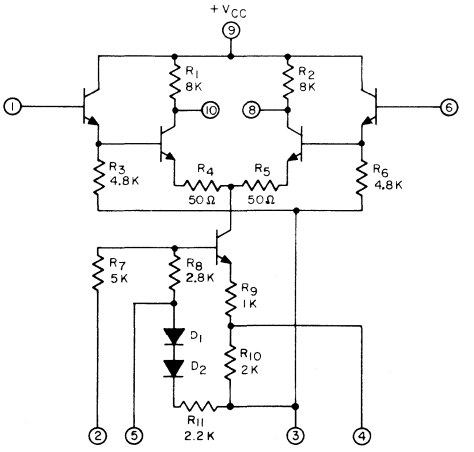


Fig. 1 – Schematic diagram

Table 1 – Available Screening Level Options (Indicated by Check (√) Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 10-LEAD TO-5 STYLE WITH STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3000	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes A, B, &C	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3000	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2 – Description of RCA Linear IC High-Reliability Part Numbers

Chip Version, CA3000 H/N

CA3000 H / N /

	PACKAGE SUFFIX LETTER	SCREENING LEVEL
Part Number (Type Designation)	H= Chip Version	/N, /R — For Description, See RIC-202

Packaged Device, CA3000 T/1N

CA3000 T / 1N /

	PACKAGE SUFFIX LETTER	SCREENING LEVEL
Part Number (Type Designation)	T =TO-5 Style with straight leads	/1N, /1R, /1, /2, /3, /4 — For Description, See RIC-202

Absolute Maximum Voltage and Current Limits at $T_A = 25^\circ$ C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 9 is 0 to −12 volts.

Terminal No.	1	2	3	4	5	6	7	8	9	10
1		*	+16▲ 0	*	*	+4 -4	Internal Connection Do not use	*	0 -12	+1 -12
2			+16 -5	*	*	*		*	0 -16	*
3				+5 -5	+5 -10	0 -16		*	0 -16	*
4					*	*		*	0 -16	*
5						*		*	0 -16	*
6								+1 -12	0 -12	*
7	Internal Connection Do not use									
8									0 -16	*
9										+16 0
10										
Case	Connected to Terminal #3 – Do Not Ground									

Maximum Current Ratings

Terminal No.	I_{IN} mA	I_{OUT} mA
1	1	0.1
2	–	–
3	–	–
4	–	–
5	1	0.1
6	–	–
7	–	–
8	–	–
9	–	–
10	–	–

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ This rating applies to the more positive of Terminals #1 or #6.

Maximum Ratings, Absolute-Maximum Values – Cont'd.

Operating-Temperature Range . . . . . -55°C to +125°C
Storage-Temperature Range . . . . . -65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16" ±1/32"
(1.59 mm ±0.79 mm)
from case for 10 s max. . . . . 265°C

Maximum Single-Ended Input-Signal Voltage . . . . . ±2 V
Maximum Common-Mode Input-Signal Voltage . . . . . ±2 V
Maximum Device Dissipation . . . . . 300 mW

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, V^+ = +6 V, V^- = −6 V, unless otherwise specified*

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		LIMITS TYPE CA3000				TYPICAL CHARACTERISTICS CURVES
				Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS								
Input Offset Voltage	V_{IO}			-	1.4	8	mV	2
Input Offset Current	I_{IO}			-	1.2	10	μA	2
Input Bias Current	I_I			-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS						
		4	5					
		NC	NC	-	2.6	-	V	4
		NC	V-	-	4.2	-	V	4
		V-	NC	-	-1.5	-	V	4
		V-	V-	-	0.6	-	V	4
Device Dissipation	P_T	NC	NC	-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS								
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz		28	32	-	dB	5
		Double-Ended Output f = 1 kHz		-	37	-	dB	5
Bandwidth at -3 dB Point	BW			-	650	-	kHz	6
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz		-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		80	98	-	dB	7
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz		70K	195K	-	Ω	8
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz		5.5K	8K	10.5K	Ω	9
Total Harmonic Distortion	THD	f = 1 kHz		-	0.2	5	%	10
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz		80	90	-	dB	NONE

Table 3 – Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions $V^+ = +6$ V, $V^- = -6$ V		Limits for Indicated Temp.(°C)						Units
				Minimum			Maximum			
				-55	+25	+125	-55	+25	+125	
STATIC										
Input Offset Voltage	V_{IO}	–		–	–	–	6.5	5	6.5	mV
Input Offset Current	I_{IO}	–		–	–	–	20	10	20	μA
Input Bias Current	I_I	–		–	–	–	70	36	25	μA
Quiescent Operating Voltage	V_8 or V_{10}	Terminal 4	Terminal 5							
		NC	NC	1.5	1.5	1.5	3.2	3.2	3.2	V
Device Dissipation	P_T	Terminal 4	Terminal 5							
		NC	NC	30	25	20	60	60	50	mW
		NC	$-V_{EE}$	25	20	15	55	55	50	mW
		$-V_{EE}$	NC	55	50	45	105	105	90	mW
		$-V_{EE}$	$-V_{EE}$	35	35	25	70	70	65	mW
DYNAMIC All tests at 1 kHz, except BW										
Differential Voltage Gain	A_{Diff}		Single-Ended Output	–	28	–	–	–	–	dB
			Double-Ended Output	–	33	–	–	–	–	dB
Maximum Output Voltage	V_{OUT} (p-p)			–	5	–	–	–	–	V_{p-p}
Bandwidth at -3 dB Point	BW			–	600	–	–	–	–	kHz
Common-Mode Rejection Ratio	CMR			–	70	–	–	–	–	dB
Single-Ended Input Impedance	Z_{IN}			–	70 k	–	–	–	–	Ω
Single-Ended Output Impedance	Z_{OUT}			–	5.5 k	–	–	10.5 k	–	Ω
Total Harmonic Distortion	THD			–	–	–	–	5	–	%
AGC Range (Maximum Voltage Gain to Complete Cut-off)	AGC			–	80	–	–	–	–	dB

*Table 4 — Pre Burn-in Electrical and Post Burn-in Electrical Tests, and Delta Limits**

Electrical Characteristics, at T_A = 25° C, V^+ = +6 V, V^- = -6 V						
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Offset Current	I_I	–	–	36	±4	μA
Quiescent Operating Voltage	V_8 or V_{10}	Terminal 4: NC Terminal 5: NC	1.5	3.2	±0.3	V
Device Dissipation	P_T	Terminal 4: NC Terminal 5: NC	25	60	±6	mW

*Levels 1 and 2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level 3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 11.

Table 5 — Final Electrical Tests

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = +6 V, V^- = -6 V	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
				MINIMUM			MAXIMUM			
				−55	+25	+125	−55	+25	+125	
Static	Input Offset Voltage	V_{IO}	–	–	–	–	6.5	5	6.5	mV
Static	Input Offset Current	I_{IO}	–	–	–	–	20	10	20	μA
Static	Input Bias Current	I_I	–	–	–	–	70	36	25	μA
Static	Quiescent Operating Voltage	V_8 or V_{10}	Terminals 4 and 5 No connection	1.5	1.5	1.5	3.2	3.2	3.2	V
Static	Device Dissipation	P_T	Terminals 4 and 5 No Connection	30	25	20	60	60	50	mW
Dynamic	Differential Voltage Gain Single Ended Output	A_{Diff}	f = 1 kHz	–	28	–	–	–	–	dB

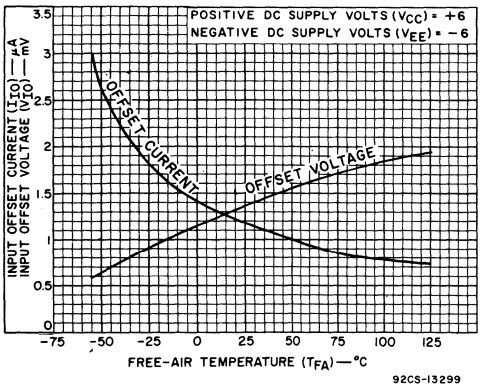


Fig. 2 — Input offset voltage and current vs temperature

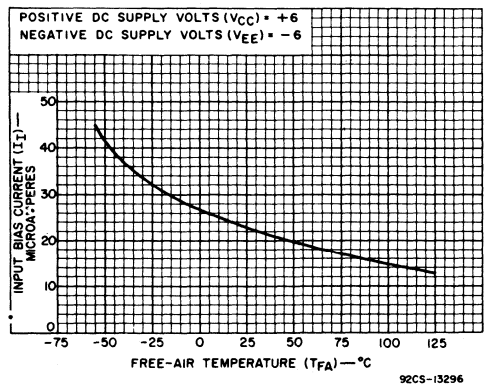


Fig. 3 — Input bias current vs temperature

STATIC CHARACTERISTICS

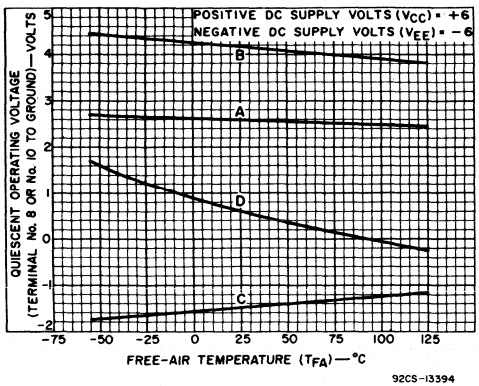


Fig. 4 — Quiescent operating voltage vs temperature

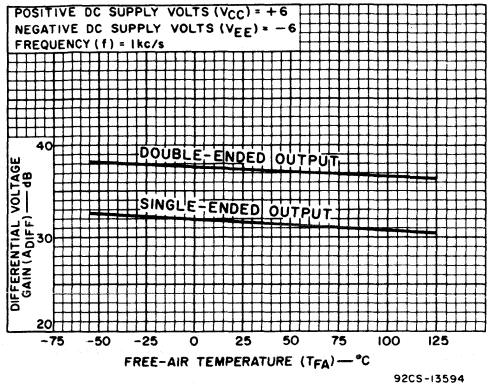


Fig. 5 — Differential voltage gain vs temperature

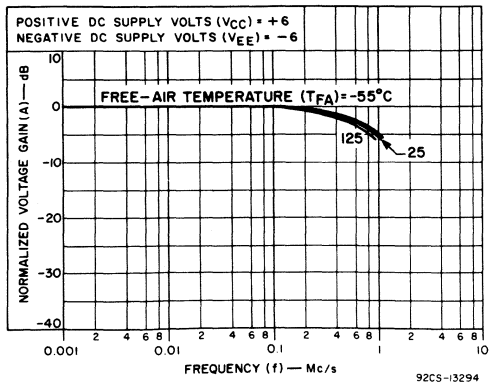


Fig. 6 — Bandwidth at -3 dB point vs temperature

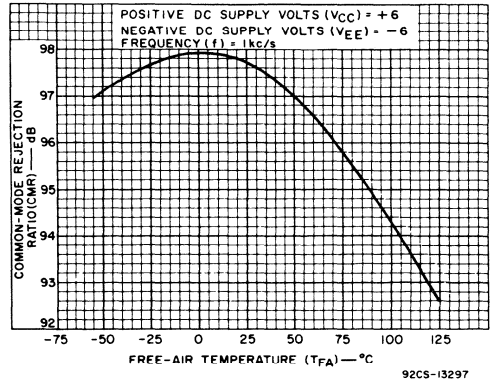


Fig. 7 — Common-mode rejection ratio vs temperature

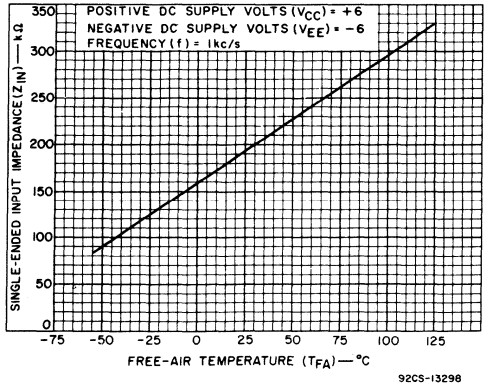


Fig. 8 — Single-ended input impedance vs temperature

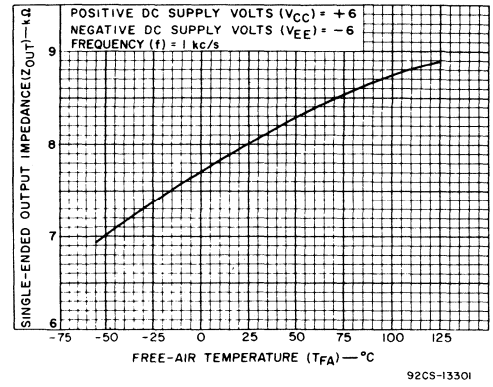


Fig. 9 — Single-ended output impedance vs temperature

DYNAMIC CHARACTERISTICS

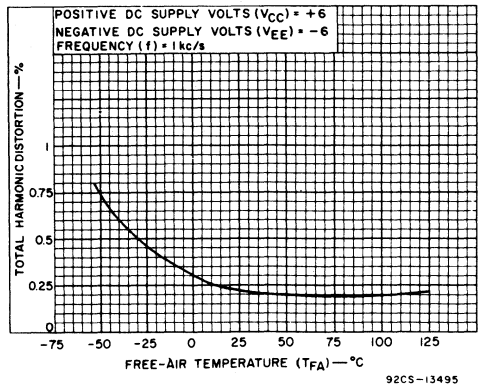


Fig. 10 — Total harmonic distortion vs temperature

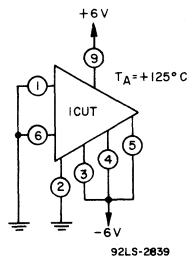


Fig. 11 — Burn-in and operating life test circuit

Table 6 — Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

Characteristic	Symbol	TEST CONDITIONS V^+ = +6 V, V^- = -6 V	Limits		Units
			Min.	Max.	
Input Offset Voltage	V_{IO}		–	5	mV
Input Offset Current	I_{IO}		–	10	μA
Input Bias Current	I_I		–	36	μA
Quiescent Operating Voltage	V_8 or V_{10}		1.5	3.2	V
Device Dissipation	P_T		25	60	mW
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single Ended Output f = 1 kHz	28	–	dB

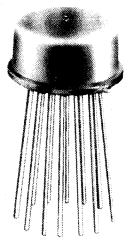
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3001/. . .



H-1463

12-Lead TO-5 Style Package

High-Reliability Video Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Push-Pull Input & Output**
- **AGC Range** . . . . . **60 dB typ.**
- **Bandwidth** . . . . . **29 MHz**
- **Input Resistance** . . . . . **150 kΩ typ.**
- **Output Resistance** . . . . . **45 Ω typ.**
- **Voltage Gain** . . . . . **19 dB typ.**
- **Input Offset Voltage** . . . . . **1.5 mV typ.**

RCA-CA3001 "Slash" (/) Series type is a high-reliability linear integrated circuit Video Amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3001 described in Data Bulletin File No. 122 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

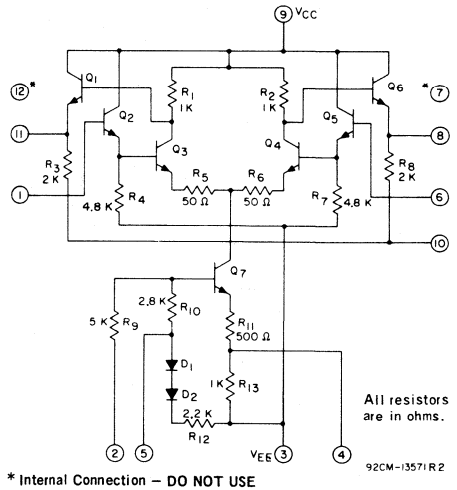
The package type CA3001 can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3001 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications

- **DC, IF, & Video Amplifier**
- **Schmitt Trigger**
- **Mixer**
- **Modulator**
- **See Companion Application Note ICAN-5038 "Applications of the RCA-CA3001 IC Video Amplifier"**



* Internal Connection – DO NOT USE

Fig. 1 – Schematic diagram.

Table 1 – Available Screening Level Options (Indicated by Check [√] Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 12-LEAD TO-5 STYLE WITH STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3001	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes A, B, &C	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3001	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2 – Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA3001 H/N

CA3001 H /N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	H= Chip Version	/N, /R — For Description See R1C-202 and DATABOOK SSD-207

Packaged Device, CA3001 T/1N

CA3001 T /1N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	T = TO-5 Style with straight leads S = TO-5 Style with Dual-In-Line Formed Leads	/1N, /1R, /1, /2, /3, /4 — For Description, See R1C-202 and DATABOOK SSD-207

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS *at* $T_A = 25°C$

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals. All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			
8	25 mA		1, 2, 6, 10 3 9	0 -6 +6 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9	0 -6 +6 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

MAXIMUM RATINGS, *Absolute-Maximum Values — Cont'd.*

OPERATING TEMPERATURE RANGE	–55°C to +125°C
STORAGE TEMPERATURE RANGE	–65°C to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max.	265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±2.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	±2.5 V
MAXIMUM DEVICE DISSIPATION	300 mW

ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Not Connected Unless Specified			LIMITS TYPE CA3001				TYPICAL CHARACTERISTICS CURVES
					Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:									
Input Offset Voltage	V_{IO}				-	1.5	-	mV	2
Input Offset Current	I_{IO}				-	1	10	μA	2
Input Bias Current	I_I				-	16	36	μA	3
Output Offset Voltage	V_{OO}				-	54	300	mV	4
Quiescent Operating Voltage	V_8 OR V_{11}	TERMINALS MODE	4	5					
		A	NC	NC	3.8	4.4	5	V	5
		B	NC	V_{EE}	-	4.8	-	V	5
		C	V_{EE}	NC	-	2.7	-	V	5
		D	V_{EE}	V_{EE}	-	4	-	V	5
Device Dissipation	P_T	A	NC	NC	60	78	120	mW	6
		B	NC	V_{EE}	-	71	-	mW	6
		C	V_{EE}	NC	-	110	-	mW	6
		D	V_{EE}	V_{EE}	-	86	-	mW	6
DYNAMIC CHARACTERISTICS:									
Differential Voltage Gain (Single-ended input and output)	A_{DIFF}	f = 1.75 MHz f = 20 MHz			16 10	19 14	- -	dB dB	7, 8
Bandwidth at -3 dB Point	BW				16	29	-	MHz	NONE
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1.75 MHz			-	5	-	V_{P-P}	NONE
Noise Figure	NF	f = 1.75 MHz, R_S = 1 KΩ			-	5	8	dB	9
		f = 11.7 MHz, R_S = 1 KΩ			-	7.7	-	dB	9
Common-Mode Rejection Ratio	CMR	f = 1 KHz			70	88	-	dB	10
Input Impedance Components:									
Parallel Input Resistance	R_{IN}	f = 1.75 MHz			50	140	-	KΩ	11
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz			-	3.4	7	pF	11
Output Resistance	R_{OUT}	f = 1.75 MHz			-	45	70	Ω	NONE
AGC Range (Maximum voltage gain to complete cutoff)	AGC	f = 1.75 MHz			55	60	-	dB	NONE

Table 2. Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions V_{CC} = +6V, V_{EE} = -6V		Limits for Indicated Temp. (°C)						Units
				Minimum			Maximum			
				-55	+25	+125	-55	+25	+125	
Static										
Input Unbalance Current	I_{IU}	–		–	–	–	23	10	5	µA
Input Bias Current	I_I	–		–	–	–	66	36	22	µA
Output Offset Voltage	V_{oo}	–		–	–	–	420	300	260	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4	Terminal 5							
		NC	NC	3.8	3.8	3.8	4.8	4.8	4.8	V
Device Dissipation	P_T	Terminal 4	Terminal 5							
		NC	NC	60	60	50	125	115	110	mW
		NC	$-V_{EE}$	55	55	45	120	105	105	mW
		$-V_{EE}$	NC	80	80	70	175	160	155	mW
		$-V_{EE}$	$-V_{EE}$	60	60	50	135	125	125	mW
Dynamic										
Differential Voltage Gain (single-ended input and output)	A_{Diff}	f = 1.75 MHz		–	16	–	–	–	–	dB
		f = 20 MHz		–	10	–	–	–	–	dB
Bandwidth at -3 dB Point	BW			–	16	–	–	–	–	MHz
Maximum Output Voltage Swing	V_{OUT} (p-p)	f = 1.75 MHz		–	4	–	–	–	–	V_{p-p}
Noise Figure	NF	f = 1.75 MHz, R_s = 1kΩ		–	–	–	–	8	–	dB
Common-Mode Rejection Ratio	CMR	f = 1 kHz		–	70	–	–	–	–	dB
Common Mode Input Voltage Range	V_{CMR}	f = 1 kHz		–	-.35 to +2.5	–	–	–	–	V
Parallel Input R	R_{IN}	f = 1.75 MHz		–	50	–	–	–	–	kΩ
Parallel Input C	C_{IN}	f = 1.75 MHz		–	–	–	–	7	–	pF
Output Resistance	R_{OUT}	f – 1.75 MHz		–	–	–	–	70	–	Ω
AGC Range (max. voltage gain to complete cutoff)	AGC	f = 1.75 MHz		–	55	–	–	–	–	dB

*Table 3 — Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits**

Electrical Characteristics, at T_A = 25°C, V^+ = +6 V, V^- = −6 V						
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Max.	Max.Δ	
Input Offset Current	I_{IO}	–	–	10	±2	μA
Input-Bias Current	I_I	–	–	36	±4	μA
Output Offset Voltage	V_{oo}	–	–	300	±100	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4: NC Terminal 5: NC	3.8	4.8	±0.5	V
Device Dissipation	P_T	Terminal 4: NC Terminal 5: NC	60	115	±12	mW

*Level /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 12.

Table 4 — Final Electrical Tests

	Characteristic	Symbol	Test Conditions V^+ = +6 V, V^- = −6 V	Limits for Indicated Temp. (°C)						Units
				Minimum			Maximum			
				-55	+25	+125	-55	+25	+125	
Static	Input Offset Current	I_{IO}	–	–	–	–	–	10	–	μA
Static	Input Bias Current	I_I	–	–	–	–	66	36	22	μA
Static	Output Offset Voltage	V_{oo}	–	–	–	–	420	300	260	mV
Static	Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4: NC Terminal 5: NC	3.8	3.8	3.8	4.8	4.8	4.8	V
Static	Device Dissipation	P_T	Terminal 4: NC Terminal 5: NC	–	60	–	–	115	–	mW
Dynamic	Differential Voltage Gain (single-ended input & output)	A_{Diff}	f = 1.75 MHz	–	16	–	–	–	–	dB

Table 5 — Group C Electrical Characteristics Sampling Tests (T_A = 25°C, V_C = +6 V, V_{EE} = −6 V)

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Input Bias Current	I_I	–	–	36	μA
Output Offset Voltage	V_{00}	–	–	300	mV
Quiescent Operating Voltage	V_8 or V_{11}	Terminal 4 5 NC NC	3.8	4.8	V
Device Dissipation	P_T	Terminal 4 5 NC NC	60	115	mW
Voltage Gain	A_{Diff}	f = 1.75 MHz	16	–	dB

TYPICAL STATIC CHARACTERISTICS

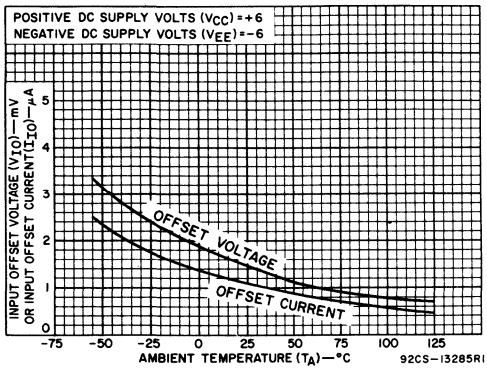


Fig. 2 — Input offset voltage and current vs. temperature.

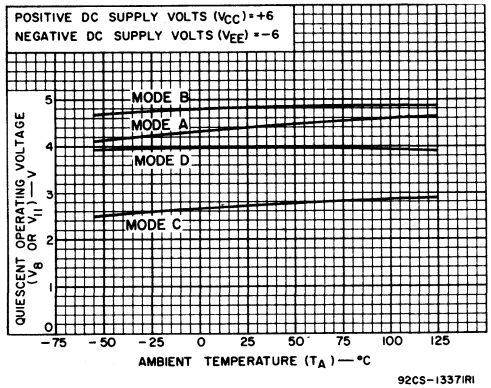


Fig. 5 — Quiescent operating voltage vs. temperature.

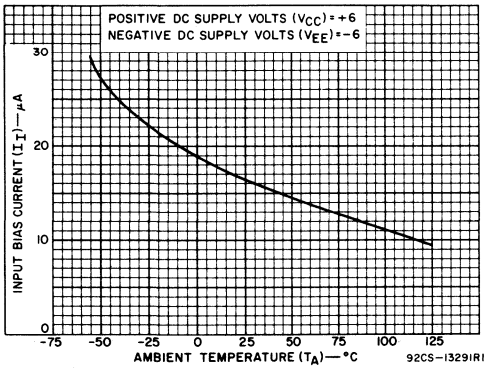


Fig. 3 — Input bias current vs. temperature.

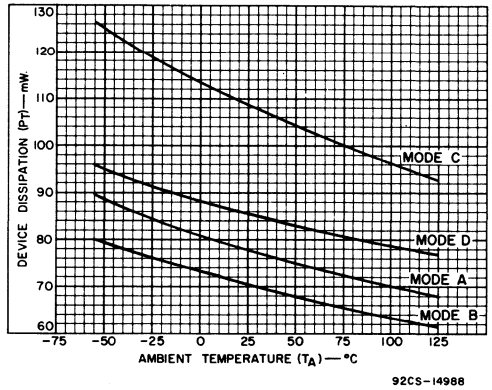


Fig. 6 — Device dissipation vs. temperature.

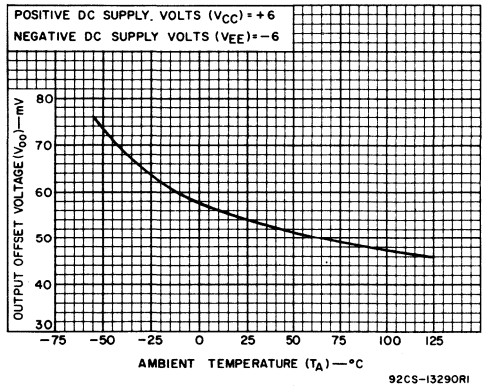


Fig. 4 — Output offset voltage vs. temperature.

TYPICAL DYNAMIC CHARACTERISTICS

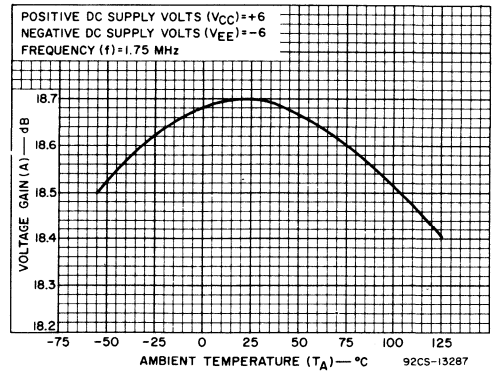


Fig. 7 — Differential voltage gain vs. temperature.

TYPICAL DYNAMIC CHARACTERISTICS – Cont'd.

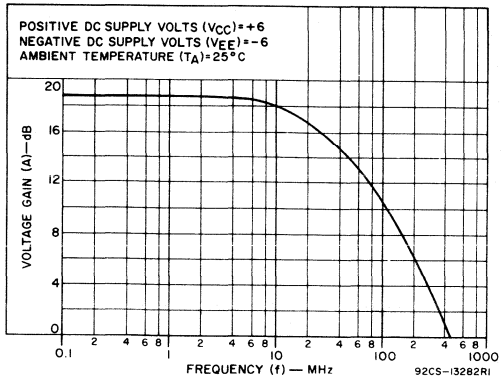


Fig. 8 – Differential voltage gain vs. frequency.

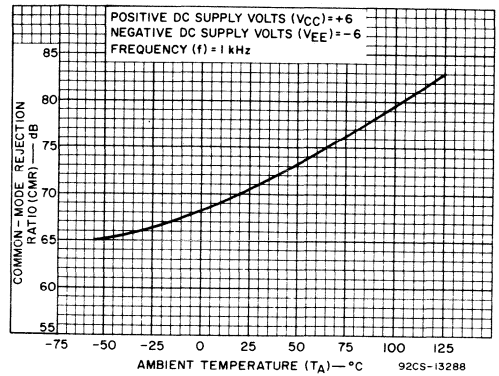


Fig. 10 – Common-mode rejection ratio vs. temperature.

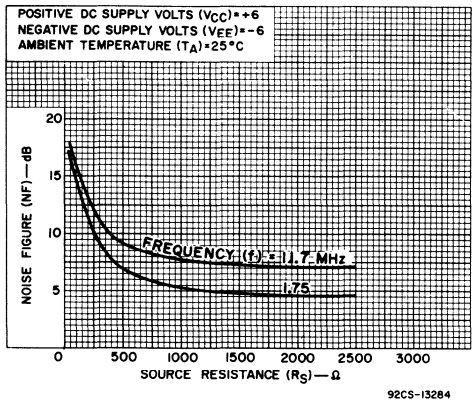


Fig. 9 – Noise figure vs. source resistance and frequency.

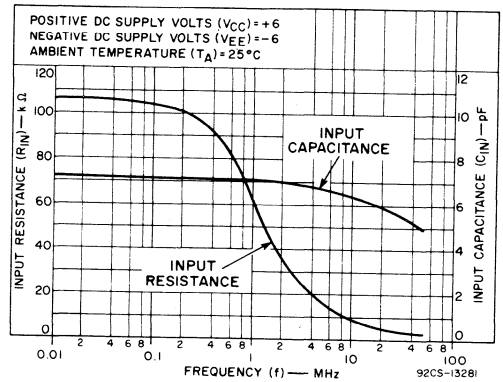


Fig. 11 – Input impedance components vs. frequency.

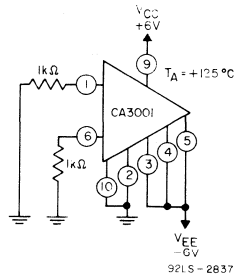


Fig. 12 – Burn-in and operating life test circuit.

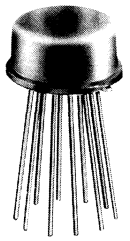
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3002/. . .



H-1528

10-Lead TO-5 Style Package

High-Reliability IF Amplifier

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Input Resistance — 100 kΩ typ.**
- **Output Resistance — 70 Ω typ.**
- **Voltage Gain — 24 dB typ. @ 1.75 MHz**
- **Push-Pull Input, Single-Ended Output**
- **-3 dB Bandwidth — 11 MHz typ.**
- **AGC Range — 80 dB typ.**
- **Useful Frequency Range DC to — 15 MHz**

RCA-CA3002 Slash (/) Series type is a high-reliability integrated-circuit IF Amplifier intended for applications in aerospace, military, and critical industrial equipment. It is electrically and mechanically identical with the standard type CA3002 described in Data Bulletin File No. 123 but is specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3002 can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels—/N, /R, and standard chip. These screening levels and detailed information test methods, procedures, and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Part Number are given on the following page.

The CA3002 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix), or in chip form ("H" suffix).

- **Product Detector**
- **AM Detector**
- **IF & Video Amplifier**
- **Schmitt Trigger**
- **See Companion Application Note ICAN-5038 "Application of RCA-3002 IC IF Amplifier"**

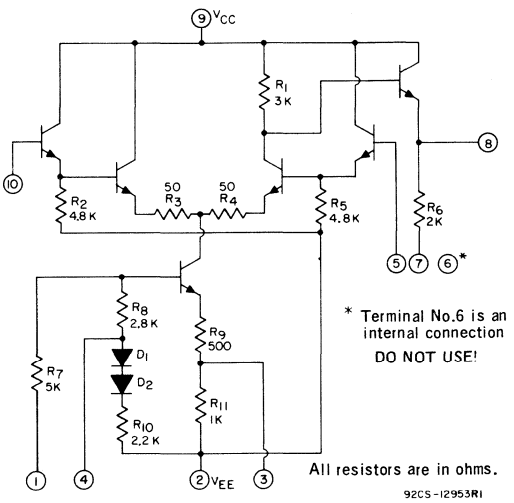


Fig. 1 Schematic Diagram

Table 1 – Available Screening Level Options (Indicated by Check [√] Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 10-LEAD TO-5 STYLE WITH STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3002	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes A, B, &C	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3002	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2 – Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA3002 H/N

CA3002 H / N /

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL	
	H= Chip Version	/N /R	For Description, See R1C-202

Packaged Device, CA3002 T/IN

CA3002 T / IN /

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL	
	T =TO-5 Style with straight leads	/1N /1R /1 /2 /3 /4	For Description, See R1C-202

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, at $T_A = 25°C$

Indicated voltage or current limits for each terminal can be applied under the specified operating conditions for other terminals.

All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$,) or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-8 V	0 V	2, 7 5, 10 9	-8 0 +6
2	-10 V	0 V	1, 5, 10 9	0 +6
3	-8.5 V	0 V	1, 5, 10 7 9	0 -6 +6
4	-8 V	0 V	1, 5, 10 2, 7 9	0 -8 +6
5	-3.5 V	+3.5 V	1, 10 2, 7 9	0 -6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL No.2 (SUBSTRATE) DO NOT GROUND			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
6	INTERNAL CONNECTION DO NOT USE			
7	-12 V	0 V	1, 5, 10 2 9	0 -6 +6
8	20 mA		1, 5, 7, 10 2 9 200 Ω Resistor Between Terminals 7 & 8	0 -6 +6
9	0 V	+10 V	1, 5, 10 2, 3, 7	0 -6
10	-3.5 V	+3.5 V	1, 5 2, 7 9	0 -6 +6

Operating-Temperature Range . . . . . -55°C to +125°C
Storage-Temperature Range . . . . . -65°C to +150°C
Maximum Input-Signal Voltage . . . . . ±3.5 V
Maximum Device Dissipation . . . . . 300 mW

Lead Temperature (During Soldering):
At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max. . . . . 265°C

ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$, $V^+ = +6$ V, $V^- = -6$ V*

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS TERMINALS No.3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED	LIMITS CA3002 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
STATIC CHARACTERISTICS:							
Input Unbalance Voltage	V_{IU}		-	2.2	-	mV	2
Input Unbalance Current	I_{IU}		-	2.2	10	μA	2
Input Bias Current	I_I		-	20	36	μA	3
Quiescent Operating Voltage		MODE / TERMINAL 2 / TERMINAL 4					
		A / V_{EE} / NC	-	2.8	-	V	4
		B / V_{EE} / V_{EE}	-	3.9	-	V	4
Device Dissipation	P_T		-	55	-	mW	None
DYNAMIC CHARACTERISTICS:							
Differential Voltage Gain (Single-Ended Input and Output)	A_{DIFF}	f = 1.75 MHz	19	24	-	dB	5 & 6
Bandwidth at -3 dB Point	BW	-	-	11	-	MHz	7
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	-	-	5.5	-	V_{P-P}	None
Noise Figure	NF	f = 1.75 MHz R_S = 1 kΩ	-	4	8	dB	8
Input Impedance Components: Parallel Input Resistance	R_{IN}	f = 1.75 MHz	-	100k	-	Ω	None
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz	-	4	-	pF	None
Output Resistance	R_{OUT}	f = 1.75 MHz	-	70	-	Ω	9 & 10
3rd Harmonic Intermodulation Distortion	IMD		-30	-40	-	dB	11
AGC Range (Maximum Voltage Gain to Complete Cutoff	AGC	f = 1.75 MHz	60	80	-	dB	12

*Table 3 – Pre-Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT $T_A = 25°C$, $V^+ = +6$ V, $V^- = -6$ V	LIMITS MIN.	MAX.	MAX. Δ	UNITS
Input Bias Current	I_I	$V^+ = +6$ V, Terminal No. 2 = -6 V, Terminal No. 1 to ground	—	31	±10	μA
Total Drain Current	I_T	$I_2 = I_9 = I_T$	5.0	15.8	±1.5	mA

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 13.

Table 4 – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6\ V, V^- = -6\ V$	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Input Unbalance Current	I_{IU}	$I_{IO} - I_5 = I_{IU}$	–	–	–	35	10	10	μA
Input Bias Current	I_I		–	–	–	85	35	30	μA
Total Drain Current	I_T	$I_2 + I_9 = I_T$	–	–	–	167	15.8	15.0	mA

Table 5 – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6\ V, V^- = -6\ V$	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Static									
Input Unbalance Current	I_{IU}	$I_{IO} - I_5 = I_{IU}$	–	–	–	35	10	10	μA
Input Bias Current	I_I		–	–	–	85	35	30	μA
Total Drain Current	I_T	$I_2 + I_9 = I_T$	–	–	–	16.7	15.8	15.0	mA
Max Output Voltage	$+V_{OM}$		–	4.6	–	–	5.4	–	V
Min. Output Voltage	$+V_{OM}$	Terminal No. 1 Ground	–	–	–	–	0.05	–	V
Dynamic									
Noise Figure	NF	f = 1.75 MHz, R_S = 1 kΩ	–	–	–	–	8	–	dB
Voltage Gain	A	f = 1.75 MHz, single-ended input and output	–	19	–	–	–	–	dB
AGC Range (Maximum Voltage gain to complete cutoff)	AGC	f = 1.75 MHz	–	60	–	–	–	–	dB

Table 6 – Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +6\ V, V^- = -6\ V$	LIMITS		UNITS
			MIN.	MAX.	
Input Unbalance Current	I_{IU}	$I_{IO} - I_5 = I_{IU}$	–	10	μA
Input Bias Current	I_I		–	35	μA
Total Drain Current	I_T	$I_2 + I_9 = I_T$	5.0	15.8	mA
Voltage Gain	A	f = 1.75 MHz, single-ended input and output	19	–	dB

STATIC CHARACTERISTICS

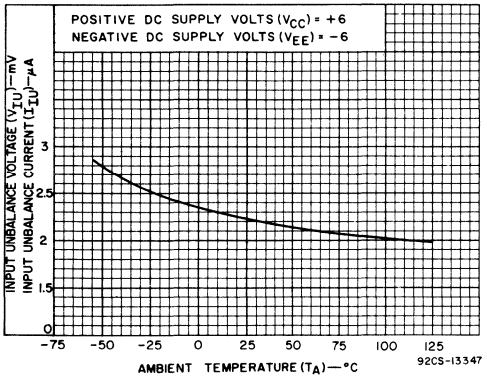


Fig. 2 — Input unbalance voltage & current vs temperature.

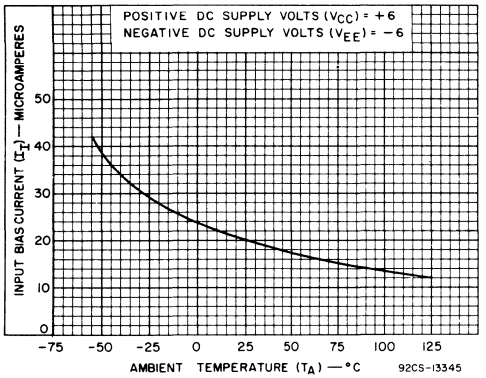


Fig. 3 — Input bias current vs temperature.

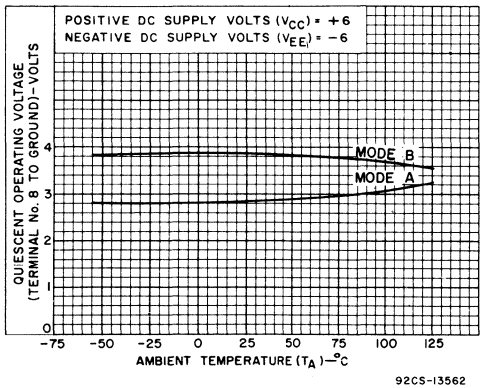


Fig. 4 — Quiescent operating voltage vs temperature.

DYNAMIC CHARACTERISTICS

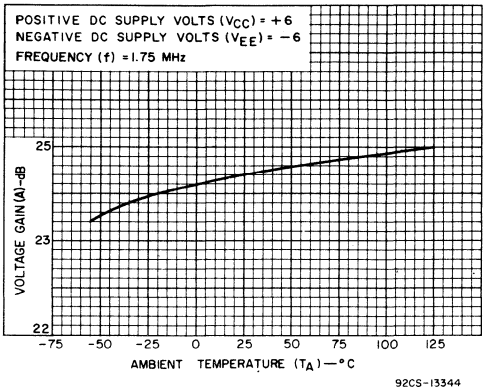


Fig. 5 — Differential voltage gain vs temperature.

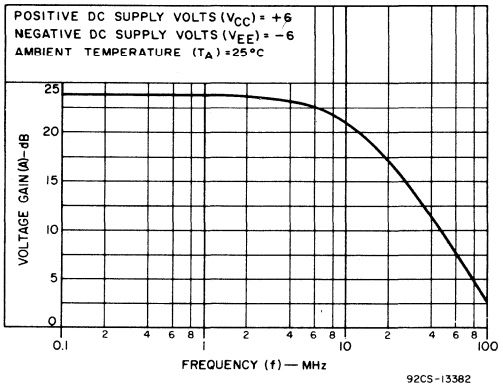


Fig. 6 — Differential voltage gain vs frequency.

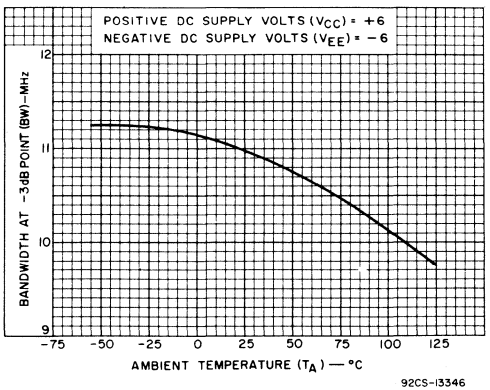


Fig. 7 — Bandwidth at -3 dB point vs temperature.

DYNAMIC CHARACTERISTICS

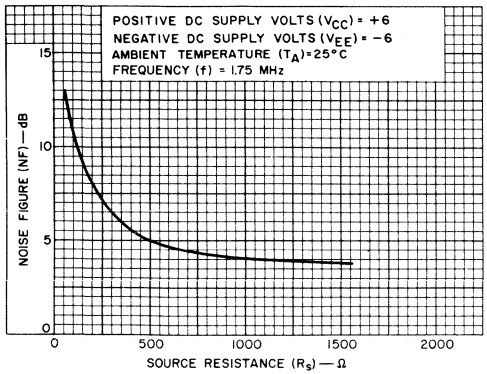


Fig. 8 — Noise figure vs source resistance.

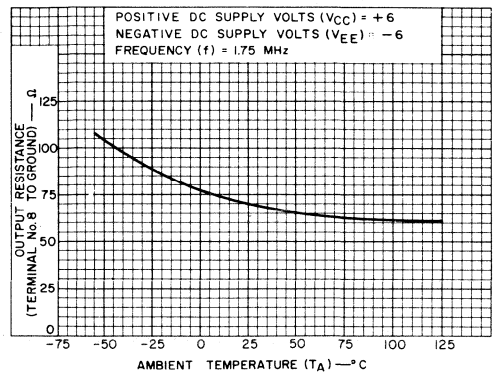


Fig. 9 — Output resistance vs temperature.

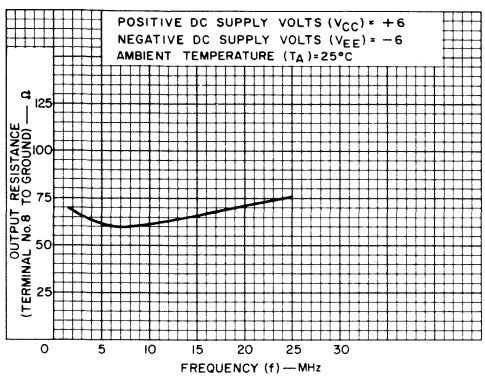


Fig. 10 — Output resistance vs frequency.

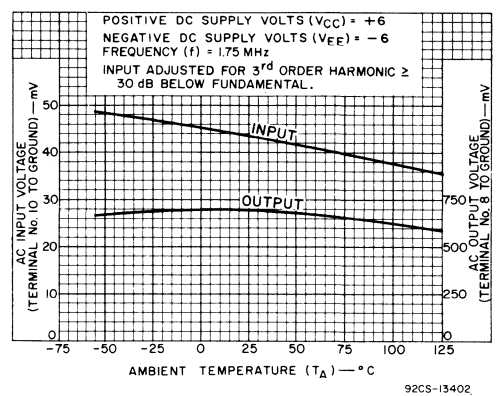


Fig. 11 — 3rd harmonic intermodulation distortion vs temperature.

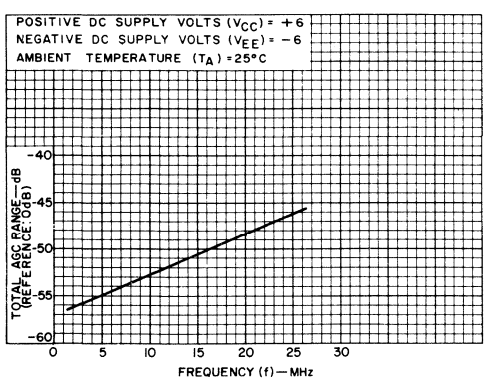


Fig. 12 — AGC range vs frequency.

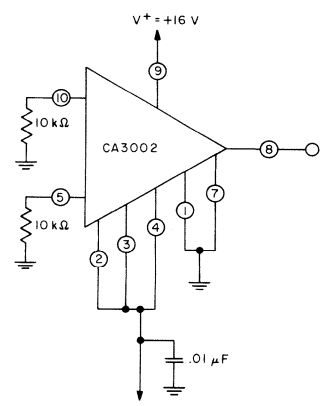


Fig. 13 — Burn-in and operating life test circuit.

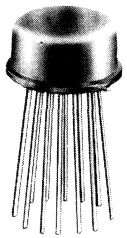
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3004/. . .



12-Lead TO-5 Style Package

High-Reliability RF Amplifier

For Aerospace, Military and Critical Industrial Equipment

Features:

- **Operation from DC to 100 MHz**
- **RF, IF, and Video frequency capability**
- **Balanced differential amplifier configuration with controlled constant-current source**

Applications:

- **Detector**
- **Push-Pull Input and Output**
- **Wide and Narrow-Band Amplifier**
- **AGC**
- **Mixer**
- **Limiter**
- **Modulator**
- **Companion Application Note ICAN-5022 "Applications of RCS-CA3004, CA3005, and CA3006 IC RF Amplifiers"**

RCA-CA3004 "Slash" (/) Series type is a high-reliability linear integrated circuit RF Amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3004 described in Data Bulletin File No. 124 but is specially processed and tested to meet the electrical, mechanical and enviromental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3004 can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High- Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on page 3.

The CA3004 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

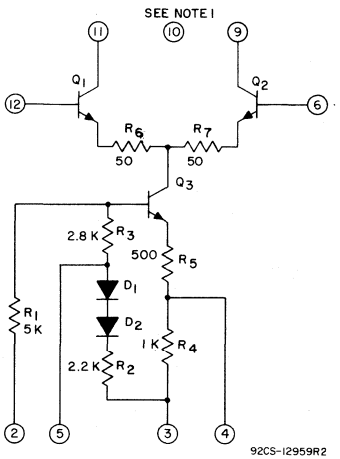


Fig. 1 – Schematic Diagram

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at $T_A = 25°C$

Voltage limits shown for each terminal can be applied under the indicated circuit conditions for other terminals. All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	NO CONNECTION			
2	-9.5	0	6	0
			12	0
			3	-9.5
			9	+6
			10	+6
			11	+6
3	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
4	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
5	-6	0	2,6,12	0
			3	-6
			9	+6
			10	+6
			11	+6
6	-3.5	+3.5	2	0
			3	-6
			9	+6
			10	+6
			11	+6
			12	0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
7	NO CONNECTION			
8	NO CONNECTION			
9	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
10	0	+12	2	0
			3	-6
			6	0
			9	+6
			11	+6
			12	0
11	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
12	-3.5	+3.5	2	0
			3	-6
			6	0
			9	+6
			10	+6
			11	+6
CASE	INTERNALLY CONNECTED TO TERMINAL NO.3 (SUBSTRATE) DO NOT GROUND			

MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE . . . . . −2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

OPERATING-TEMPERATURE RANGE . . . . −55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . −65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max. . . . . 265°C

Table 1 – Available Screening Level Options (Indicated by Check (√) Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 12-LEAD TO-5 STYLE WITH STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3004	Custom	/1N	√
		/1R	√
	Standard	/1	√
	Equivalent to	/2	√
	MIL-STD-883	/3	√
	Classes A, B, &C	/4	√
CHIP			*(H) Suffix*
CA3004	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2 – Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA3004H/N

CA3004 H /N /

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	H= Chip Version	/N /R For Description, See R1C-202

Packaged Device CA3004 T/IN

CA3004 T /1N /

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	T =TO-5 Style with straight leads	/1N /1R /1 /2 /3 /4 For Description, See R1C-202

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$, $V^+ = +6V$, $V^- = -6$ V unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Terminals No.4 and No.5 Open Unless Otherwise Specified		LIMITS TYPE CA3004 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
STATIC CHARACTERISTICS								
Input Offset Voltage	V_{IO}			–	1.7	5	mV	Fig.2
Input Offset Current	I_{IO}			–	0.125	5	μA	Fig.2
Input Bias Current	I_I			–	21	40	μA	Fig.3
Quiescent Operating Current	I_9 or I_{11}	TERMINALS 4	5					
		NC	NC	–	1	–	mA	Fig. 4
		V^-	NC	–	2.7	–	mA	Fig. 4
		NC	V^-	–	0.45	–	mA	Fig. 4
		V^-	V^-	–	1.25	–	mA	Fig. 4
Quiescent Operating Current Ratio	I_9/I_{11}			–	1.1	–	–	Fig. 5
Device Dissipation	P_T			–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS								
Power Gain	G_P	f = 100 MHz		10	12	–	dB	Fig. 6
Noise Figure	NF	f = 100 MHz		–	6.3	9	dB	Fig. 7
Common Mode Rejection Ratio	CMRR	f = 1 kHz		–	98	–	dB	Fig. 8
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz		-60	–	–	dB	NONE

*Table 3 – Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS T_A = 25°C, V^+ = +6 V, V^- = –6 V	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Offset Voltage	V_{IO}		–	5	±2	mV
Input Bias Current	I_I		–	40	±4	μA
Device Dissipation	P_D		–	45	±5	mW

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 9.

Table 4 – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = +6V, V^- = –6 V	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
STATIC									
Device Dissipation	P_D		–	16	–	–	45	–	mW
Input Offset Current	I_{IO}		–	–	–	9	5	7	μA
Input Bias Current	I_I		–	–	–	60	40	40	μA
DYNAMIC									
Power Gain		f = 100 MHz	–	10	–	–	–	–	dB
Noise Figure	NF	f = 100 MHz	–	–	–	–	9	–	dB

Table 5 – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS T_A = 25°C, V^+ +6V, V^- = –6 V	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}		–	–	–	5	5	5	mV
Input Offset Current	I_{IO}		–	–	–	9	5	7	μA
Input Bias Current	I_I		–	–	–	60	40	40	μA
DYNAMIC									
Power Gain		f = 100 MHz	–	10	–	–	–	–	dB
Noise Figure	NF	f = 100 MHz	–	–	–	–	9	–	dB
AGC Range (Max. Voltage gain to Complete Cutoff)	AGC		–	-60	–	–	–	–	dB

Table 6. Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = +6 V, V^- = −6 V	LIMITS		UNITS
			MIN.	MAX.	
Device Dissipation	P_D		–	45	mW
Power Gain	G_P	f = 100 MHz	10	–	dB
Input Bias Current	I_I		–	40	μA

TYPICAL STATIC CHARACTERISTICS

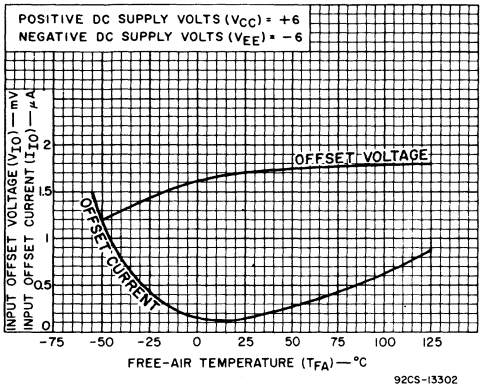


Fig. 2 — Input offset voltage and current vs temperature.

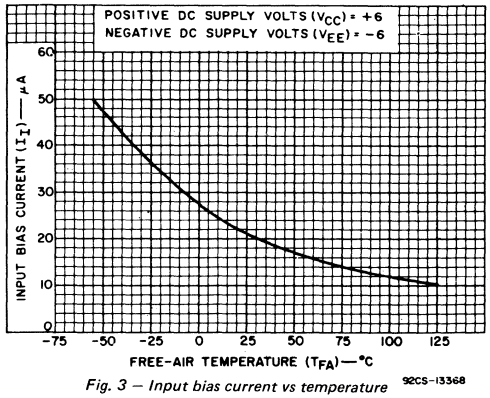


Fig. 3 — Input bias current vs temperature

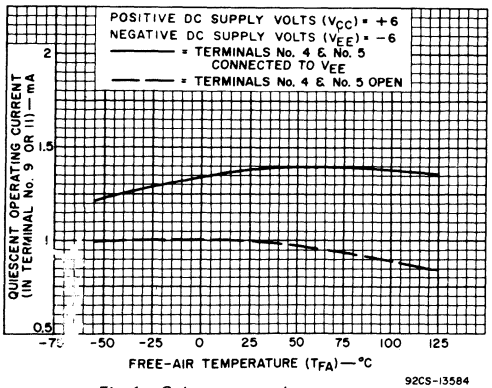


Fig. 4 — Quiescent operating current vs temperature.

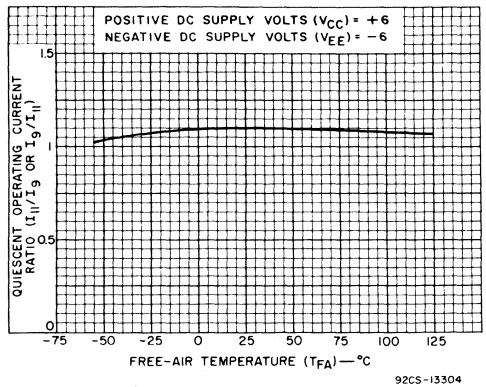


Fig. 5 — Quiescent operating current ratio vs temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPE CA3004

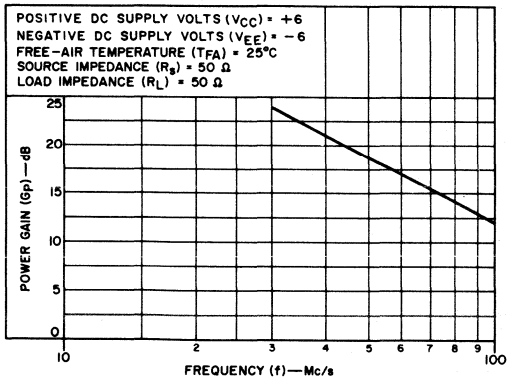


Fig. 6 – Power Gain Vs Frequency

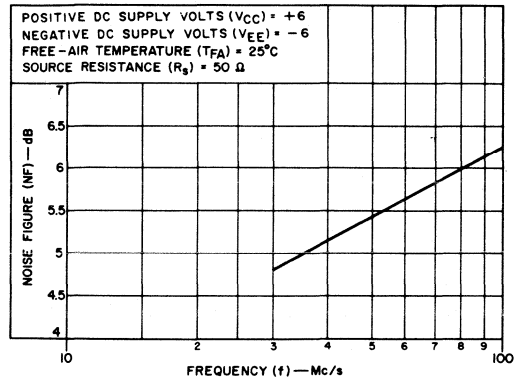


Fig. 7 – Noise Figure Vs Frequency

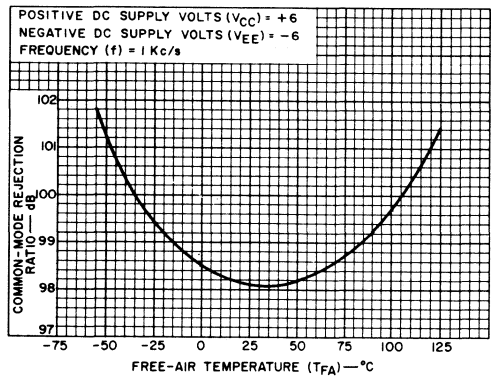


Fig. 8 – Common-Mode Rejection Ratio

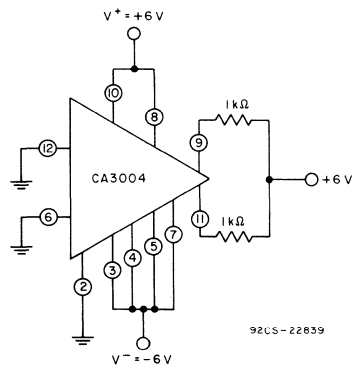


Fig. 9 – Burn-In and Operating Life Test Circuit

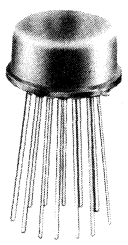
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3015A/...



H-1463
12-Lead TO-5 Style Package

High-Reliability Operational Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Open-loop voltage gain** . . . . . **70 dB typ.**
- **Common-mode rejection ratio** . . . . . **103 dB typ.**
- **Input impedance** . . . . . **10 kΩ typ.**
- **Input offset voltage** . . . . . **1 mV typ.**
- **Input offset current** . . . . . **0.5 μA typ.**
- **Input bias current** . . . . . **4.7 μA typ.**
- **Static power drain at ± 12 V** . . . . . **175 mW typ.**

RCA-CA3015A "Slash" (/) Series type is a high-reliability linear integrated circuit operational amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3015A described in Data Bulletin File No. 310 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3015A can be supplied to six screening levels — /1N, /1R, /1, /2, /3, and /4 — which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels — /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3015A Slash (/) Series type is supplied in the 8-lead TO-5 style package ("T" suffix), in 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix) or in chip form ("H" suffix).

Applications:

- **Narrow-band and band-pass amplifier**
- **Operational functions**
- **Feedback amplifier**
- **DC and video amplifier**
- **Multivibrator**
- **Oscillator**
- **Comparator**
- **Servo driver**
- **Scaling adder**
- **Balanced modulator-driver**

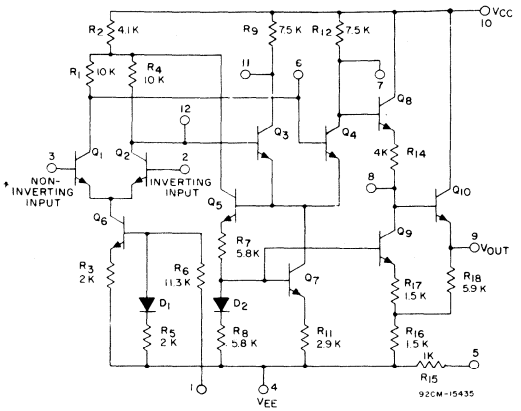


Fig. 1 — Schematic diagram.

Table 1 Available Screening Level Options (Indicated by Check (√) Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 12-LEAD TO-5 STYLE WITH STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3015	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes "A", "B", & "C"	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3015	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2
Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA3015 H/N

CA3015 H / N /

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL	
	H= Chip Version	/N /R	For Description, see R1C-202

Packaged Device, CA3015 T/IN

CA3015 T / IN /

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL	
	T =TO-5 Style with straight leads S = TO-5 Style with Dual-In-Line Formed Leads (DIL-CAN)	/IN /IR /1 /2 /3 /4	For Description, See R1C-202

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Operating-Temperature Range . . . . . -55°C to +125°C
Storage-Temperature Range . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32"
(1.59 mm ± 0.79 mm)
from case for 10 s max. . . . . 265°C

Maximum Input-Signal Voltage . . . . . -8 V, +1 V

MAXIMUM DEVICE DISSIPATION:

At Ambient Temperatures	Up to 70°C	700 mW
	Above 70°C	Derate at 6.7 mW/°C
At Case Temperatures	Up to 125°C	830 mW

Maximum Voltage Ratings at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 12 with respect to terminal 10 is 0 to -15 volts.

TERMINAL No.	12	1	2	3	4▲	5	6	7	8	9	10	11
12		*	+15 -1	*	*	*	+5 -5	*	*	*	0 -15	+1 -15
1			*	*	+20 -5	*	*	*	*	*	*	*
2				+5 -5	+18 -5 Note 2	*	*	*	*	*	*	*
3					+18 -5 Note 2	*	+1 -15	*	*	*	*	*
4▲						0 -30 Note 3	*	*	0 -30	0 -30	0 -32	*
5							*	*	*	*	0 -30	*
6								+1 -15	*	*	0 -20	*
7									+20 -5	*	0 -20	*
8										+1 -5	0 -30	*
9											0 -32	*
10												+20 0
11												

Maximum Current Ratings

TERMINAL No.	I_{IN} mA	I_{OUT} mA
12	1	1
1	–	–
2	1	0.1
3	1	0.1
4▲	–	–
5	–	–
6	1	1
7	3	3
8	3	3
9	30	30
10	–	–
11	3	3

▲ CA3015A Case is internally connected to the substrate (Terminal Lead #4), DO NOT GROUND.

Note 1: For normal circuit operation, external voltages should **not** be applied to terminals 5,6,8, and 12.

Note 2: This rating applies **only** to the more positive terminal of terminals 2 or 3.

Note 3: Carefully observe maximum dissipation ratings.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS *AT* $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS $V^+ = +12$ V, $V = -12$ V TERMINAL NO. 5 NOT CONNECTED UNLESS OTHERWISE SPECIFIED	CA3015A MIN.	CA3015A TYP.	CA3015A MAX.	UNITS	TYPICAL CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS:							
Input Offset Voltage	V_{IO}		–	1	2	mV	2
Input Offset Current	I_{IO}		–	0.5	1.6	μA	2
Input Bias Current	I_I		–	4.7	6	μA	3
Input Offset Voltage Sensitivity: Positive Negative	$\Delta V_{IO}/\Delta V_{CC}$ $\Delta V_{IO}/\Delta V_{EE}$		– –	0.096 0.156	0.5 0.5	mV/V	none
Device Dissipation	P_T	Terminal 8 shorted to Terminal 12	– –	175 500	– –	mV	none
DYNAMIC CHARACTERISTICS:							
Open-Loop Differential Voltage Gain	A_{OL}		66	70	–	dB	4
Open-Loop Bandwidth at -3 dB Point	BW_{OL}		200	320	–	kHz	6 & 7
Slew Rate	SR	$R_S = 1$ kΩ	–	7	–	V/μs	none
Common-Mode Rejection Ratio	CMRR		80	103	–	dB	5
Maximum Output-Voltage Swing	$V_{O(P-P)}$		–	14	– –	V_{P-P}	6
Input Impedance	Z_{IN}		7.5	10	–	kΩ	7
Output Impedance	Z_{OUT}		–	85	–	Ω	8
Common-Mode Input-Voltage Range	V_{CMR}		–	+0.65 -8	–	V	none
Noise Figure	NF	$R_s = 1$ kΩ	–	11	16	dB	

TYPICAL STATIC CHARACTERISTICS

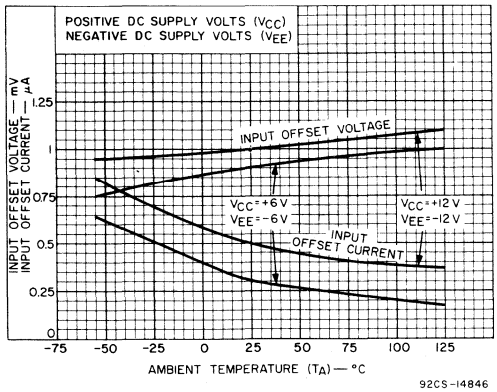


Fig. 2 — Input offset voltage and current

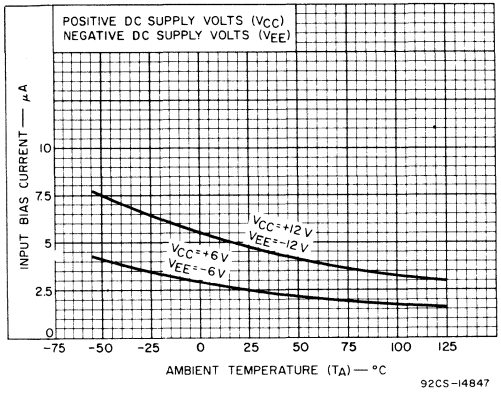


Fig. 3 — Input bias current

Table 3
Pre Burn-In and Post Burn-In Electrical Tests, and Delta Limits*

ELECTRICAL CHARACTERISTICS, at T_A = V^+ = +12V, V^- = -12V						
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max.Δ	
Input Offset Voltage	V_{IO}		–	2	±1	mV
Input Offset Current	I_{IO}		–	1.6	±1	μA
Input Bias Current	I_I		–	6	±1	μA
Device Dissipation	P_T		110	240	±25	mW
		5 shorted to 9	320	600	±50	

*Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 9.

Table 4
Final Electrical Tests

CHARACTERISTICS	SYMBOL	TEST CONDITIONS V^+ = +12V, V^- = -12 V	LIMITS FOR INDICATED TEMP.,(°C)						UNITS
			Minimum			Maximum			
			-55	+25	+125	-55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	3	2	3	mV
Input Offset Current	I_{IO}	–	–	–	–	3	1.6	2	μA
Input Bias Current	I_I	–	–	–	–	14	6	8	μA
Device Dissipation	P_T		115	110	95	280	240	235	mW
		5 shorted to 9	330	320	–	700	600	–	mW
DYNAMIC									
Open-Loop Differential Voltage Gain	A_{OL}	f = 1 kHz	–	66	–	–	–	–	dB

Table 5
Group C Electrical Sampling Tests

T_A = +25°C V^+ = +12 V V^- = -12V					
CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	V_{IO}	–	–	2	mV
Input Offset Current	I_{IO}	–	–	1.6	μA
Input Bias Current	I_I	–	–	6	μA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	–	–	0.5	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	–	–	0.5	mV/V
Device Dissipation	P_T	–	110	240	mW
		Terminal 5 shorted to 9	320	600	mW
Open-Loop Differential Voltage Gain	A_{OL}	f = 1 kHz	66	–	dB
Common-Mode Rejection Ratio	CMR	f = 1 kHz	80	–	dB

Table 6
Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions $V^+ = +12$ V, $V^- = -12$ V	Limits for Indicated Temperature (°C)						Units
			Minimum			Maximum			
			-55	+25	+125	-55	+25	+125	
STATIC									
Input Offset Voltage	V_{IO}	–	–	–	–	3	2	3	mV
Input Offset Current	I_{IO}	–	–	–	–	3	1.6	2	μA
Input Bias Current	I_I	–	–	–	–	14	6	8	μA
Input Offset Voltage Sensitivity Positive	$\frac{\triangle V_{IO}}{\triangle V^+}$	–	–	–	–	–	0.5	–	mV/V
Negative	$\frac{\triangle V_{IO}}{\triangle V^-}$	–	–	–	–	–	0.5	–	mV/V
Device Dissipation	P_T	–	115	110	95	280	240	235	mW
		5 shorted to 9	330	320	–	700	600	–	mW
DYNAMIC All tests are at 1 kHz except BW_{OL}									
Open-Loop Differential Voltage Gain	A_{OL}	–	–	66	–	–	–	–	dB
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	–	–	200	–	–	–	–	kHz
Common-Mode Rejection Ratio	CMR	–	–	80	–	–	–	–	dB
Maximum Output-Voltage Swing	$V_{O(P-P)}$	–	–	12	–	–	–	–	V_{P-P}
Input Impedance	Z_{IN}	–	–	7.5	–	–	–	–	kΩ
Output Impedance	Z_{OUT}	–	–	–	–	–	120	–	Ω
Common-Mode Input-Voltage Range	V_{CMR}	–	–	+0.35 to -8	–	–	–	–	V
Noise Figure	NF		–	–	–	–	16	–	dB

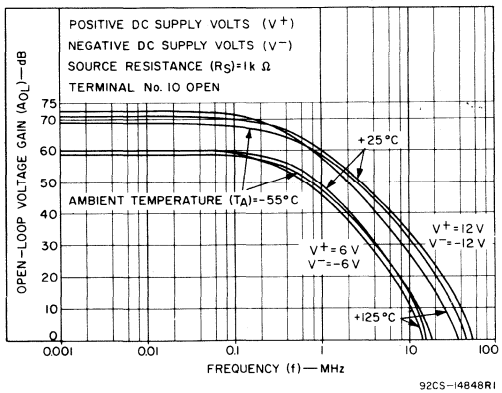


Fig.4 – Open loop voltage gain vs. frequency

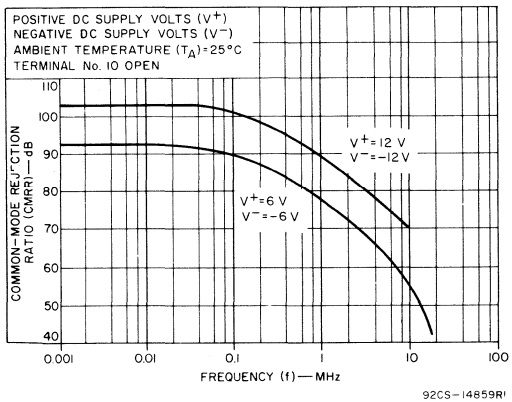
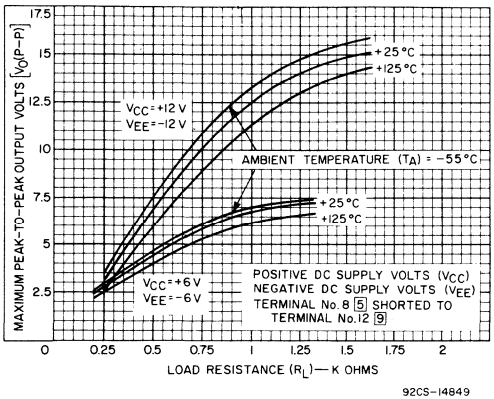


Fig.5 – Common-mode rejection ratio vs. frequency



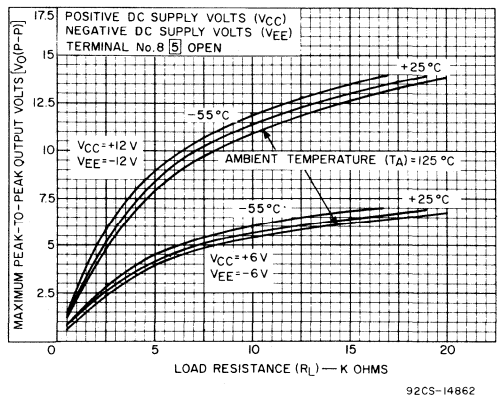


Fig.6 — Maximum Peak-To-Peak Output Voltage vs. Load Resistance

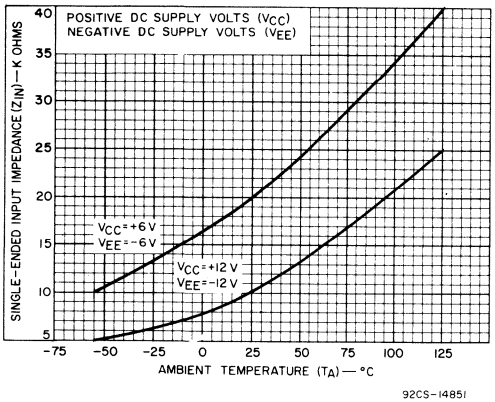


Fig.7 — Single-ended input impedance vs. temperature.

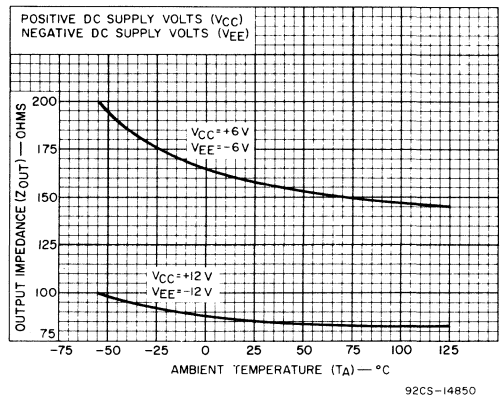


Fig.8 — Output impedance vs. temperature.

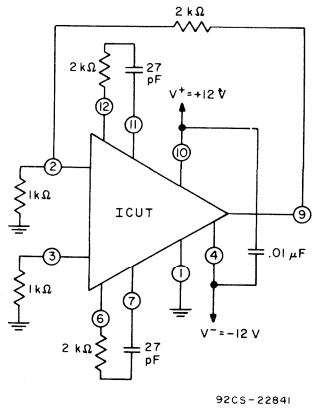


Fig.9 — Burn-in and operating life test circuit.

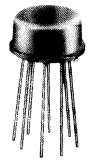
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3019/...



H-1528

10-LEAD TO-5 STYLE PACKAGE

High-Reliability Diode Array Diode Quad and Two Individual Diodes

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Excellent diode match**
- **Low leakage current**
- **Low pedestal voltage when gating**

RCA-CA3019 "Slash" (/) Series type is a high-reliability linear integrated circuit Diode Array consisting of a diode quad and two individual diodes. It is intended for telemetry, data processing, instrumentation and communications applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3019 described in Data Bulletin File No. 236 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

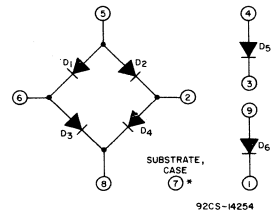
The package type CA3019 can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3019 Slash (/) Series type is supplied in the 10-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications:

- **Modulator**
- **Mixer**
- **Balanced modulator**
- **Analog switch**
- **Diode gate for chopper-modulator applications**
- **See companion application note ICAN-52911 application of the RCA CA3019 IC Diode Array**



* Connect to most negative circuit potential.

Fig. 1 – Schematic diagram.

Table 1 – Available Screening Level Options (Indicated by Check [√] Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 10-LEAD TO-5 STYLE WITH LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3019	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes "A", "B", & "C"	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3019	Custom	/N	√
		/R	√
	Standard chip		√

Table 2 – Description of RCA Linear IC High-Reliability Part Number

Packaged Device, CA3019 T/1N

CA3019 T √1N

	PACKAGE SUFFIX LETTER	SCREENING LEVEL
Part Number (Type Designation)	T = TO-5 Style with straight leads S = TO-5 Style with Dual-In-Line Formed Leads (DILCAN)	/1N /1R /1 /2 /3 /4 For Description, See RIC-202

Chip Version, CA3019H /N

CA3019 H √N /

	PACKAGE SUFFIX LETTER	SCREENING LEVEL
Part Number (Type Designation)	H = Chip Version	/N /R For Description, See RIC-202

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

Any one diode unit	20 max.	mW
Total for device	120 max.	mW

TEMPERATURE RANGE:

Storage	−65 to +150	°C
Operating	−55 to +125	°C

LEAD TEMPERATURE *(During Soldering)*:

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max. . . . . 265°C

Absolute-Maximum Voltage Limits at $T_A = 25°C$

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3	+12	7	-6
2	-3	+12	7	-6
3	-3	+12	7	-6
4	-3	+12	7	-6
5	-3	+12	7	-6
6	-3	+12	7	-6
7	-18	0	1, 2, 3, 6, 8	0
8	-3	+12	7	-6
9	-3	+12	7	-6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

ELECTRICAL CHARACTERISTICS, at an Ambient Temperature, T_A, of 25°C
CHARACTERISTICS APPLY FOR EACH DIODE UNIT, UNLESS OTHERWISE SPECIFIED.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3019		TYPICAL CHARACTERISTICS CURVES
			Typ.	Units	Fig.
DC Forward Voltage Drop	V_F	DC Forward Current (I_F) = 1 mA	0.73	V	2
DC Reverse Breakdown Voltage	$V_{(BR)R}$	DC Reverse Current (I_R) = -10 μA	6	V	-
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	DC Reverse Current (I_R) = -10 μA	80	V	-
DC Reverse (Leakage) Current	I_R	DC Reverse Voltage (V_R) = -4 V	0.0055	μA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	DC Reverse Voltage (V_R) = -4 V	0.010	μA	-
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F1} - V_{F2} \rvert$	DC Forward Current (I_F) = 1 mA	1	mV	-
Single Diode Capacitance	C_D	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = -2 V	1.8	pF	4
Diode Quad-to-Substrate Capacitance	C_{DQ-I}	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = -2 V			
		Terminal 2 or 6 to Terminal 7	4.4	pF	5
		Terminal 5 or 8 to Terminal 7	2.7	pF	6
Series Gate Switching Pedestal Voltage	V_S		10	mV	-

*Table 3 – Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Each Diode: DC Forward Voltage Drop	V_F	I_F = 1 mA	–	0.78	±0.010	V
		I_F = 0.2 mA	–	0.72	±0.010	V
		I_F = 20 mA	–	0.95	±0.010	V

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 7.

Table 4 – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
Each Diode:									
DC Forward Voltage Drop	V_F	I_F = 0.2 mA	–	–	–	–	0.72	–	V
		I_F = 1 mA	0.76	–	0.41	0.97	0.79	0.60	V
		I_F = 20 mA	–	–	–	–	0.95	–	V
DC Reverse Leakage Current	I_R	V_R = –4 V	–	–	–	–	10	–	μA
DC Reverse Leakage Current To Substrate	I_R	V_R = –4 V	–	–	–	–	10	–	μA
Between Any Two Diodes: Diode Offset Voltage	$\lvert V_{F1} - V_{F2} \rvert$	I_F = 1 mA	–	–	–	–	5	–	mV
Isolation-to-Substrate Breakdown Voltage		–50 V through a 25 KΩ to terminal 10. Ground terminal 1 through 9, 11 and 12. Measure voltage at terminal 10	–	50	–	–25	–25	–25	V

Table 5 – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
Each Diode:									
DC Forward Voltage Drop	V_F	I_F = 0.2 mA	–	–	–	–	0.72	–	V
		I_F = 1 mA	0.76	–	0.41	0.97	0.78	0.60	V
		I_F = 20 mA	–	–	–	–	0.95	–	V
DC Reverse Leakage Current	I_R	V_R = –4 V	–	–	–	–	10	–	μA
DC Reverse Leakage Current To Substrate	I_R	V_R = –4 V	–	–	–	–	10	–	μA
Between Any Two Diodes: Diode Offset Voltage	$\lvert V_{F1} = V_{F2} \rvert$	I_F = 1 mA	–	–	–	–	5	–	mV
Isolation-to-Substrate Breakdown Voltage		–50 V through a 25 KΩ to terminal 7. Ground terminal 1 through 6, 8 and 9. Measure voltage at terminal 7	–	50	–	–25	–25	–25	V

Table 6 – Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Each Diode:					
DC Forward Voltage Drop	V_F	I_F = 0.2 mA	0.39	0.73	V
		I_F = 1 mA	0.49	0.79	V
		I_F = 20 mA	0.59	0.96	V
DC Reverse Leakage Current	I_R	V_R –4 V	–	10	μA
DC Reverse Leakage Current To Substrate	I_R	V_R = –4 V	–	10	μA
Between Any Two Diodes: Diode Offset Voltage	$V_{F1} - V_{F2}$	I_F = 1 mA	–	5	mV
Isolation-to-Substrate Breakdown Voltage		–50 V through a 25 KΩ to terminal 7, Ground terminal 1 through 6, 8 and 9. Measure voltage at terminal 7	–	–25	V

TYPICAL CHARACTERISTICS

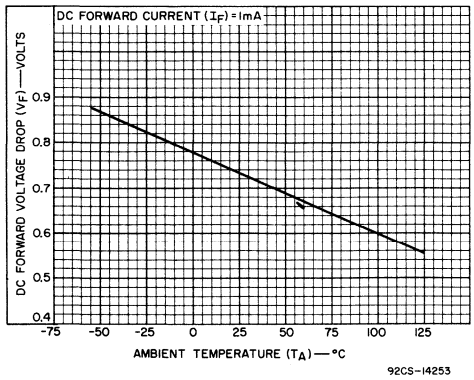


Fig. 2 – DC Forward Voltage Drop (any Diode) vs Temperature for CA3019.

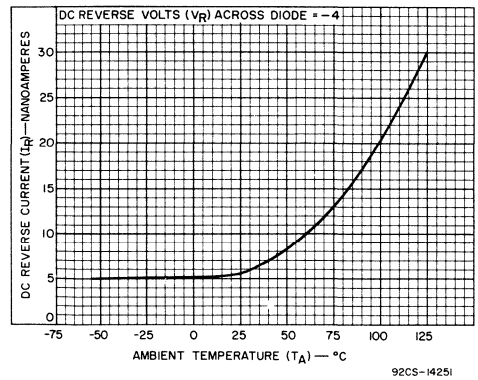


Fig. 3 – Reverse (Leakage) Current (any Diode) vs Temperature for CA3019.

TYPICAL CHARACTERISTICS – Cont'd

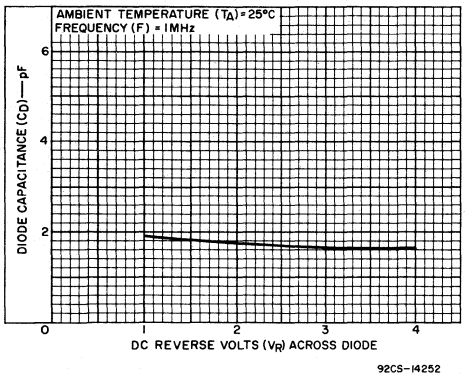


Fig. 4 – Diode capacitance (any diode) vs reverse voltage for CA3019.

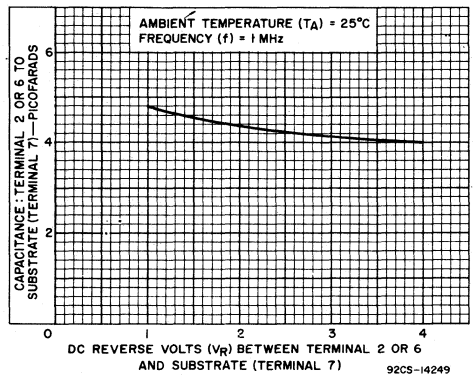


Fig. 5 – Diode quad-to-substrate capacitance vs reverse voltage for CA3019.

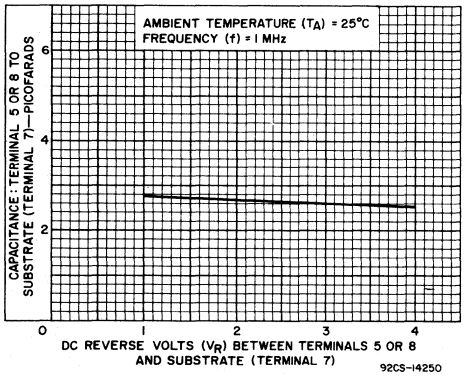


Fig. 6 – Diode quad-to-substrate capacitance vs reverse voltage for CA3019.

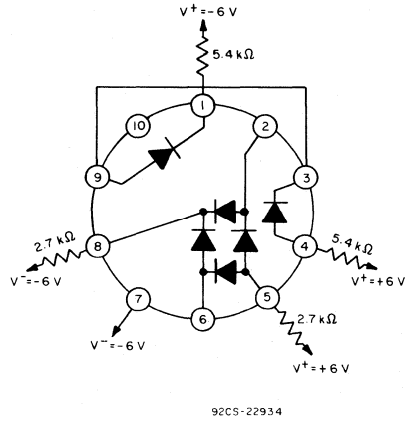


Fig. 7 – Burn-In and operating life test circuit

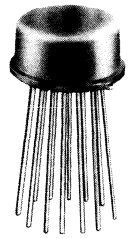
RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3026/. . .



12 Lead TO-5 Style Package

H-1463

High-Reliability
Transistor Array
Dual Independent Differential Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Maximum input offset voltage — ±5 mV**
- **Full military temperature range capability — -55°C to +125°C**

RCA-CA3026 "Slash" (/) Series type is a high-reliability linear integrated circuit Dual Independent and Differential Amplifier is intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3026 described in Data Bulletin File No. 388 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD883.

The package type CA3026 can be supplied to six screening levels -- /1N, /1R, /1, /2, /3, and /4 -- which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels -- /N, /R, and standard chip. These screening levels and detailed information on test methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on page 4.

The CA3026 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications:

- **Dual sense amplifiers**
- **Dual Schmitt triggers**
- **Multifunction combinations — RF/Mixer/Oscillator; Converter/II**
- **IF amplifiers (differential and/or cascode)**
- **Product detectors**
- **Doubly balanced modulators and demodulators**
- **Balanced quadrature detectors**
- **Cascade limiters**
- **Synchronous detectors**
- **Pairs of balanced mixers**
- **Synthesizer mixers**
- **Balanced (push-pull) cascode amplifiers**

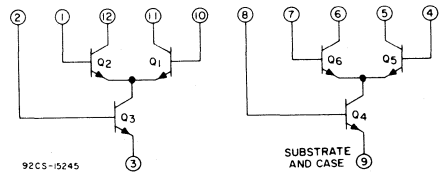


Fig. 1 — Schematic Diagram

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, *Absolute-Maximum Values, at $T_A = 25°C$*

POWER DISSIPATION,		
Any one transistor	300	mW
Total package	600	mW
For $T_A > 55°C$	Derate at 5	mW/°C
TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +200	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1 and horizontal terminal 3 is +15 to −5 volts.

CA3026 TERMINAL No. → / ↓	10	11	12	1	2	3	4	5	6	7	8	Note 1 9
10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*
11			*	*	*	+20 0	*	*	*	*	*	+20 0
12				+20 0	*	+20 0	*	*	*	*	*	+20 0
1					*	+15 -5	*	*	*	*	*	*
2						+1 -5	*	*	*	*	*	*
3							*	*	*	*	*	*
4								0 -20	*	+5 -5	*	+15 -5
5									*	*	*	+20 0
6										+20 0	*	+20 0
7											*	+15 -5
8												+1 -5
9												*
9												Ref Sub-strate

Maximum Current Ratings

CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
10	5	0.1
11	50	0.1
12	50	0.1
1	5	0.1
2	5	0.1
3	0.1	-50
4	5	0.1
5	50	0.1
6	50	0.1
7	5	0.1
8	5	0.1
9	0.1	50

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No. 9 is connected to the emitter of Q4, the reference substrate, and the case; therefore, should not be grounded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3026 LIMITS			UNITS	TYPICAL CHARACTERISTICS CURVES
			MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS							
For Each Differential Amplifier							
Input Offset Voltage	V_{IO}	V_{CB} = 3 V $I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	0.3	2	μA	7
Input Bias Current	I_I		-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q_1)}}{I_{C(Q_2)}}$ or $\frac{I_{C(Q_5)}}{I_{C(Q_6)}}$		-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	1.1	-	μV/°C	5
For Each Transistor							
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V, I_C = 50 μA I_C = 1 mA I_C = 3 mA I_C = 10 mA	- - - -	0.630 0.715 0.750 0.800	0.700 0.800 0.850 0.900	V	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-	-1.9	-	mV/°C	4
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V	-
DYNAMIC CHARACTERISTICS							
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V V_{EE} = -6 V V_x = -3.3 V f = 1 kHz	-	100	-	dB	
AGC Range, One Stage	AGC		-	75	-	dB	
Voltage Gain, Single Stage Double-Ended Output	A		-	32	-	dB	
AGC Range, Two Stage	AGC		-	105	-	dB	
Voltage Gain, Two Stage Double-Ended Output	A		-	60	-	dB	
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)							
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ	11
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-	11

ELECTRICAL CHARACTERISTICS at T_A = 25°C – Cont'd.

DYNAMIC CHARACTERISTICS CONT'D.							
1/f Noise Figure (For Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)							
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Each Collector $I_C \approx$ 1.25 mA f = 1 MHz	-	-20+j0	-	mmho	13a
Input Admittance	y_{11}		-	0.22+j0.1	-	mmho	13b
Output Admittance	y_{22}		-	0.01+j0	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-0.003 +j0	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)							
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Total Stage $I_C \approx$ 2.5 mA f = 1 MHz	-	68-j0	-	mmho	14a
Input Admittance	y_{11}		-	0.55+j0	-	mmho	14b
Output Admittance	y_{22}		-	0+j0.02	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	0.004-j0.005	-	μmho	14d
Noise Figure	NF	f = 100 MHz	-	8	-	dB	-

Table 1. Available Screening Level Options (Indicated by Check (√) Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 12-LEAD TO-5 STYLE WITH STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3026	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes "A", "B", & "C"	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3026	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2. Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA3026 H/N

CA3026 H /N

	PACKAGE SUFFIX LETTER	SCREENING LEVEL
Part Number (Type Designation)	H= Chip Version	/N /R For Description, See R1C-202 and DATABOOK SSD-207

Packaged Device, CA3026 T/IN

CA3026 T /1N

	PACKAGE SUFFIX LETTER	SCREENING LEVEL
Part Number (Type Designation)	T =TO-5 Style with straight leads	/1N /1R /1 /2 /3 /4 For Description, See R1C-202 and DATABOOK SSD-207

Table 4. Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Input Bias Current For Each Transistor Q1, Q2, Q5, and Q6	I_I	V_{CE} = 3V, I_E = 2mA	–	24	±6.0	μA
Base-to-Emitter Voltage For Each Transistor Q3 and Q4	V_{BE}	V_{CE} = 3V, I_E = 1mA	0.7	0.8	±0.1	V
Input Offset Voltage For Each Differential Amplifier	V_{IO}	V_{CE} = 3V, I_E = 2mA	–	5	±2	mV

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 13.

Table 5. Group A Electrical Sampling Inspection Tests and Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
For Each Transistor:									
Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	0.1	0.1	20	μA
Collector To-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E = 0	–	20	–	–	–	–	V
Emitter-To-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	–	5	–	–	–	–	V
Collector-To-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μ A, I_{C1} = 0	–	20	–	–	–	–	V
Collector-To-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	–	–	–	–	V
Input Bias Current For Transistors Q3 and Q4	I_I	V_{CE} = 3 V, I_E = 2mA	–	–	–	50	25	20	μA
Input Bias Current For Transistors Q1, Q2, Q5, and Q6	I_I	V_{CE} = 3 V, I_E = 2mA	–	–	–	50	25	20	μA
Base-To-Emitter Voltage For Transistors Q3 and Q4	V_{BE}	V_{CE} = 3 V, I_E = 1mA	0.7	0.7	0.4	1.05	0.8	0.75	V
For Each Differential Amplifier									
Input Offset Current	I_{IO}	V_{CE} = 3 V, I_E = 2mA	–	–	–	–	2	–	μA
Input Offset Voltage	V_{IO}	V_{CE} = 3 V, I_E = 2mA	–	–	–	–	5	–	mV

TYPICAL STATIC CHARACTERISTICS – Cont'd.

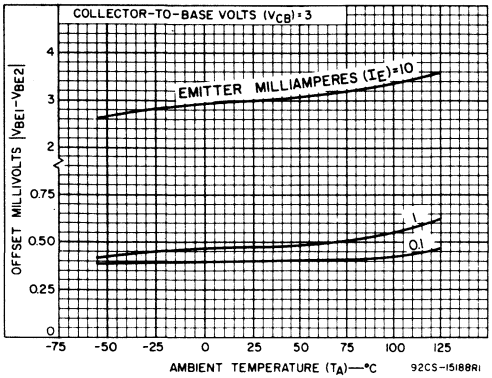


Fig. 5 – Offset voltage characteristic vs ambient temperature for differential pairs.

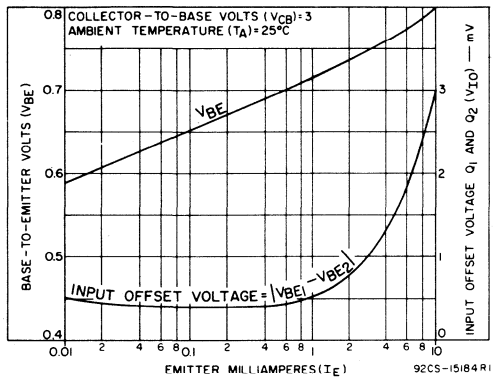


Fig. 6 – Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

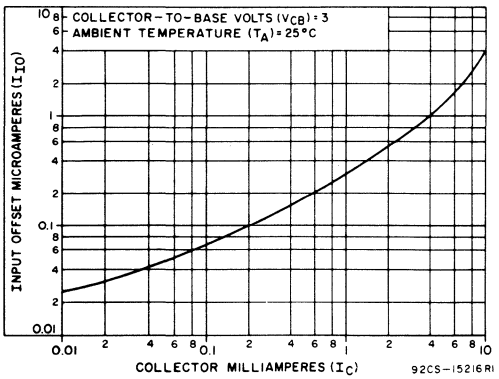


Fig. 7 – Input offset current for matched differential pairs vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS

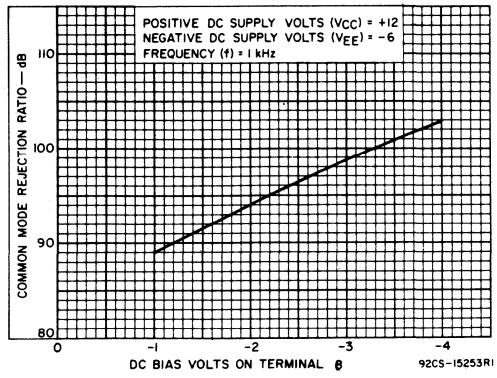


Fig. 8 – Common-mode rejection ratio

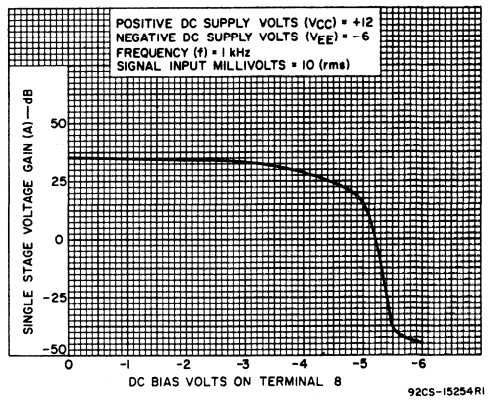


Fig. 9 – Single-stage voltage gain

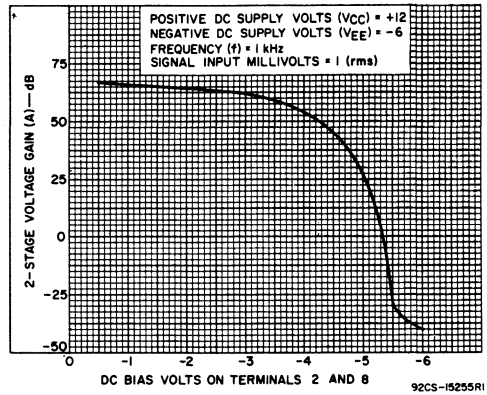


Fig. 10 – Two-stage voltage gain.

Table 6. Group C Electical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
For Each Transistor: Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.2	μA
Input Bias Current For Transistors Q1, Q2, Q5, & Q6	I_I	V_{CE} = 3 V, I_E = 2mA	–	28	μA
Base-to-Emitter Voltage For Transistors Q3 and Q4	V_{BE}	V_{CE} = 3 V, I_E = 1mA	0.65	0.85	V
For Each Differential Amplifier: Input Offset Voltage	V_{IO}	V_{CE} = 3 V, I_E = 2mA	–	6	mV

TYPICAL STATIC CHARACTERISTICS

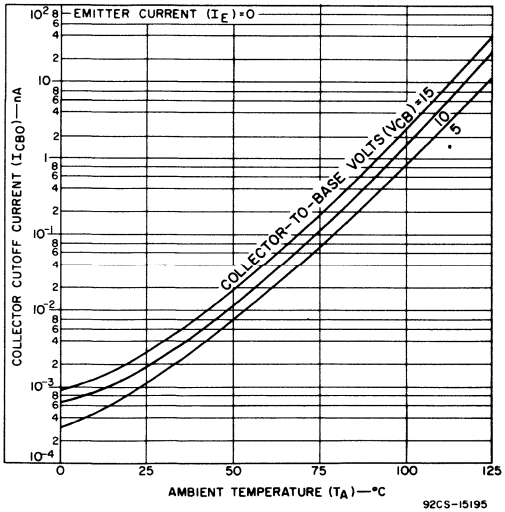


Fig. 2 – Collector-to-base cutoff current vs ambient temperature for each transistor.

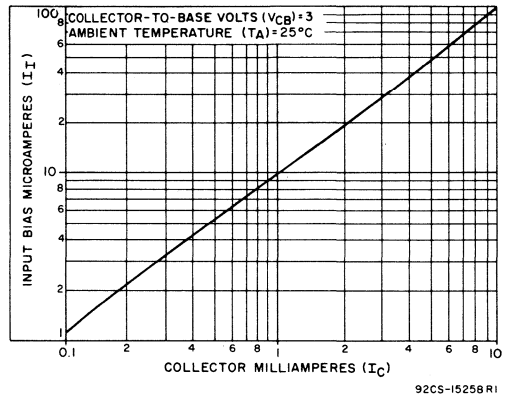


Fig. 3 – Input bias current characteristic vs collector current for each transistor.

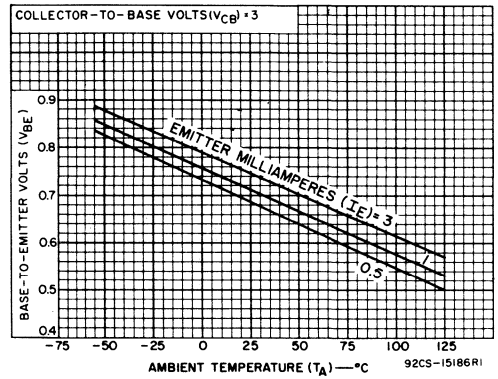


Fig. 4 – Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

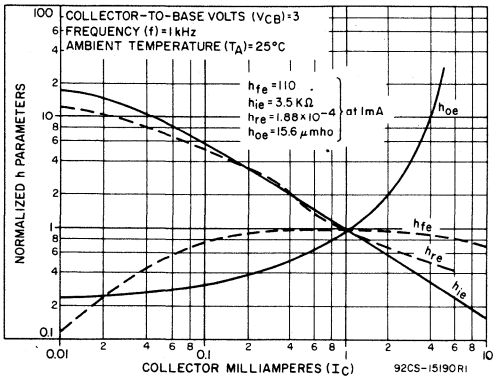


Fig. 11 — Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

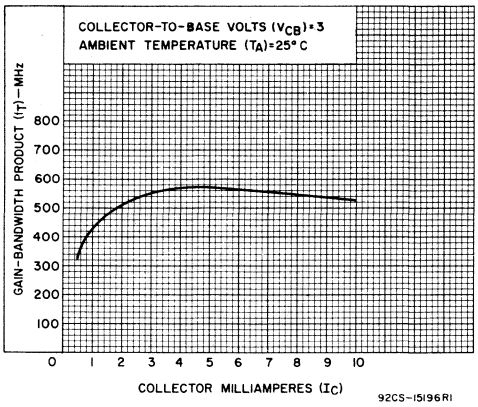


Fig. 12 — Gain-bandwidth product (f_T) vs collector current.

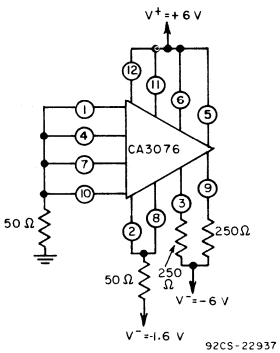


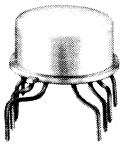
Fig. 13 — Burn-in and operating life test circuit.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CA3028B/. . .



8-LEAD TO-5 Style Package with Dual-In-Line Formed Leads

H-1787

8-LEAD TO-5 Style Package

H-1528

High-Reliability Differential/Cascode Amplifier

For Applications In Aerospace, Military and Critical Industrial Equipment

Features:

- **Controlled for input offset voltage, input offset current, and input bias current**
- **Balanced differential amplifier configuration with controlled constant-current source to provide unexcelled versatility**
- **Single- and dual-ended operation**
- **Operation from DC to 120 MHz**
- **Balanced-AGC capability**
- **Wide operating-current range**

RCA-CA3028B "Slash" (/) Series type is a high-reliability linear integrated circuit Differential/Cascode Amplifier intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3028B described in Data Bulletin File No. 382 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3028B can be supplied to six screening levels — /1N, /1R, /1, /2, /3, and /4 — which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels — /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3028B Slash (/) Series type is supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

Applications:

- **RF and IF amplifiers (differential or cascode)**
- **DC, audio, and sense amplifiers**
- **Converter in the Commerical FM Band**
- **Oscillator** ■ **Mixer** ■ **Limiter**
- **See Application Note, ICAN 5337 "Application of the RCA CA3028 integrated circuit amplifier in the HF and VHF ranges."**

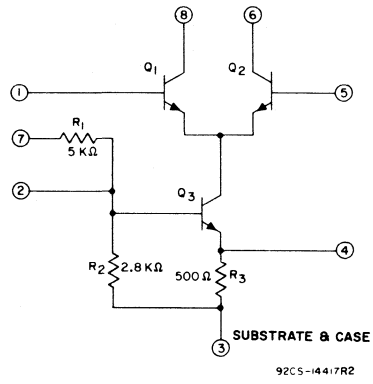


Fig. 1 — Schematic diagram.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- At T_A up to 85°C . . . . . 450 mW
- At T_A > 85°C derate linearly . . . . . 5 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating . . . . . −55 to +125°C
- Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max. . . . . 265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15	0 to -15	0 to -15	+5 to -5	*	*	+20 to 0
2			+5 to -11	+5 to -1	+15 to 0	*	+15 to 0	*
3‡				+10 to 0	+15 to 0	+30● to 0	+15 to 0	+30● to 0
4					+15 to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

● Limit is +24V

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

Table 1. Available Screening Level Options (Indicated by Check (√) Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 8-LEAD TO-5 STYLE: WITH STRAIGHT LEADS (T) SUFFIX	PACKAGE 8-LEAD TO-5 STYLE: WITH DUAL-IN-LINE FORMED LEADS "DIL-CAN" (S) SUFFIX
PACKAGED DEVICE				
CA3000	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883 Classes A, B, &C	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
CHIP			*(H) SUFFIX*	
CA3000	Custom	/N		√
		/R		√
	Standard Chip			√

Table 2. Description of RCA Linear IC High-Reliability Part Number

Packaged Device, CA3028BT/1N

CA3028B / T / 1N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL	
	T = TO-5 Style with straight leads S = TO-5 Style with Dual-In-Line formed leads (DIL-CAN)	/1N /1R /1 /2 /3 /4	For Description, See R1C-202

Chip Version, CA3028BH/N

CA3028B / H / N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL	
	H= Chip Version	/N /R	For Description, See R1C-202

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS TYPE CA3028B MIN.	LIMITS TYPE CA3028B TYP.	LIMITS TYPE CA3028B MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS								
		V^+	V^-					
Input Offset Voltage	V_{IO}	6 V 12 V	6 V 12 V	– –	0.98 0.89	5 5	mV	2
Input Offset Current	I_{IO}	6 V 12 V	6 V 12 V	– –	0.56 1.06	5 6	µA	2
Input Bias Current	I_I	6.V 12 V	6 V 12 V	– –	16.6 36	40 80	µA	3
Quiescent Operating Current	I_6 or I_8	6 V 12 V	6 V 12 V	1 2.5	1.25 3.3	1.5 4	mA	4 5
Input Current (Terminal No. 7)	I_7	6 V 12 V	6 V 12 V	0.5 1	0.85 1.65	1 2.1	mA	–
Device Dissipation	P_T	6 V 12 V	6 V 12 V	24 120	36 175	42 220	mW	6

ELECTRICAL CHARACTERISTICS AT T_A = 25°C – Cont'd.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS TYPE CA3028B Min.	Typ.	Max.	UNITS
DYNAMIC CHARACTERISTICS							
Power Gain	G_P	f = 100 MHz, V_{CC} = +9V	Cascode	16	20	-	dB
			Diff.-Ampl.	14	17	-	
		f = 10.7 MHz, V_{CC} = +9V	Cascode	35	39	-	dB
			Diff.-Ampl.	28	32	-	
Noise Figure	NF	f = 100 MHz, V_{CC} = +9V	Cascode	-	7.2	9	dB
			Diff.-Ampl.	-	6.7	9	
Input Admittance	Y_{11}	f = 10.7 MHz, V_{CC} = +9V	Cascode	-	0.6 + j 1.6	-	mmho
			Diff.-Ampl.	-	0.5 + j 0.5	-	
Reverse Transfer Admittance	Y_{12}		Cascode	-	0.0003 - j0	-	mmho
			Diff.-Ampl.	-	0.01 - j0.0002	-	
Forward Transfer Admittance	Y_{21}		Cascode	-	99 - j18	-	mmho
			Diff.-Ampl.	-	-37 + j0.5	-	
Output Admittance	Y_{22}		Cascode	-	0. + j0.08	-	mmho
			Diff.-Ampl.	-	0.04 + j0.23	-	
Power Output (Untuned)	P_o	f = 10.7 MHz	Diff.-Ampl. 50 Ω Input-Output	-	5.7	-	μW
AGC Range (Max. Power Gain to Full Cutoff)	AGC	V_{CC} = +9V	Diff.-Ampl.	-	62	-	dB
Voltage Gain at f = 10.7 MHz	A	f = 10.7 MHz, V_{CC} = +0V, R_L = 1 kΩ	Cascode	-	40	-	dB
			Diff.-Ampl.	-	30	-	
Voltage Gain Differential at f = 1 kHz	A	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		35	38	42	dB
		V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		40	42.5	45	
Max. Peak-to-Peak Output Voltage at f = 1 kHz	V_o(P-P)	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		7	11.5	-	V_{P-P}
		V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		15	23	-	
Bandwidth at -3 dB point	BW	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	7.3	-	MHz
		V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	8	-	
Common-Mode Input-Voltage Range	V_{CMR}	V_{CC} = +6V, V_{EE} = -6V		-2.5	(-3.2 - 4.5)	4	V
		V_{CC} = +12V, V_{EE} = -12V		-5	(-7 - 9)	7	
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V		60	110	-	dB
		V_{CC} = +12V, V_{EE} = -12V		60	90	-	
Input Impedance at f = 1 kHz	Z_{IN}	V_{CC} = +6V, V_{EE} = -6V		-	5.5	-	kΩ
		V_{CC} = +12V, V_{EE} = -12V		-	3	-	
Peak-to-Peak Output Current	I_{P-P}	V_{CC} = +9V, f = 10.7 MHz, e_{in} = 400 mV		2.5	4	6	mA
		V_{CC} = +12V	Diff.-Ampl.	4.5	6	8	

TABLE II. GROUP A ELECTRICAL SAMPLING INSPECTION

Characteristics	Symbol	Test Conditions		Limits for Indicated Temp. (°C)						Units
				Minimum			Maximum			
		V_{CC}	V_{EE}	-55	+25	+125	-55	+25	+125	
Static										
Input Offset Voltage	V_{IO}	+6	-6	–	–	–	7	5	7.5	mV
		+12	-12	–	–	–	5	5	6	
Input Offset Current	I_{IO}	+6	-6	–	–	–	10	5	7.5	μA
		+12	-12	–	–	–	12	6	9	
Input Bias Current	I_I	+6	-6	–	–	–	70	40	35	μA
		+12	-12	–	–	–	130	80	55	
Quiescent Oper. Current	I_6 or I_8	+6	-6	0.5	1.0	0.5	2.0	1.5	2.0	mA
		+12	-12	2.0	2.5	1.5	4.5	4.0	4.0	
Input Current (terminal 7)	I_7	+6	-6	0.5	0.5	0.35	1.5	1.0	1.2	mA
		+12	-12	1.0	1.0	0.75	2.5	2.1	2.0	
Device Dissipation	P_T	+6	-6	20	24	20	45	42	45	mW
		+12	-12	120	120	105	230	220	210	
Dynamic										
Power Gain	G_P	V_{CC} = +9V, f = 10.7 MHz, Cascode		–	35	–	–	–	–	dB
		V_{CC} = +9V, f = 10.7 MHz, Diff-Ampl		–	28	–	–	–	–	
		V_{CC} = +9V, f = 100 MHz, Cascode		–	16	–	–	–	–	
		V_{CC} = +9V, f = 100 MHz, Diff-Ampl		–	14	–	–	–	–	
Noise Figure	NF	V_{CC} = +9V, f = 100 MHz, Cascode		–	–	–	–	9	–	dB
		V_{CC} = +9V, f = 100 MHz, Diff-Ampl		–	–	–	–	9	–	
		V_{CC}	V_{EE}	Freq. kHz	R_L kΩ					
Voltage Gain (Differential)	A	+6	-6	1	2	–	35	–	–	42	–	dB
		+12	-12		1.6	–	40	–	–	45	–	
Max. Peak-to-Peak Output Voltage	$V_{O(P-P)}$	+6	-6	1	2	–	7	–	–	–	–	$V_{(P-P)}$
		+12	-12		1.6	–	15	–	–	–	–	
Common-Mode Input-Voltage Range	V_{CMR}	+6	-6			–	-2.5 to +4	–	–	–	–	V
		+12	-12			–	-5 to +7	–	–	–	–	
Common-Mode Rejection Ratio	CMR	+6	-6			–	60	–	–	–	–	dB
		+12	-12			–	60	–	–	–	–	

Table 3. PRE BURN-IN ELECTRICAL AND POST BURN-IN ELECTRICAL TESTS, AND DELTA LIMITS*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Max.	Max.Δ	
Input Bias Current	I_1		-	80	± 8	μA
Input Offset Voltage	V_{IO}		-	5	± 2	mV
Quiescent Oper. Current	I_6 or I_8		2.5	4	± 0.4	mA
Input Current (term. 7)	I_7		1.0	2.1	± 0.2	mA
Device Dissipation	P_T		120	220	± 24	mW

*Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits.
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 7.

Table 4. FINAL ELECTRICAL TESTS

CHARACTERISTICS	SYM-BOLS	TEST CONDITIONS		LIMITS FOR INDICATED TEMPERATURE (°C)						UNITS
				Minimum			Maximum			
		V^+	V^-	-55	+25	+125	-55	+25	+125	
STATIC										
Input Offset Voltage	V_{IO}	+6 +12	-6 -12	- -	- -	- -	- 5	5 5	- 6	mV
Input Offset Current	I_{IO}	+6 +12	-6 -12	- -	- -	- -	- 12	5 6	- 9	μA
Input Bias Current	I_I	+6 +12	-6 -12	- -	- -	- -	- 130	40 80	- 55	μA
Quiescent Oper. Current	I_6 or I_8	+6 +12	-6 -12	- 2.0	1 2.5	- 1.5	- 4.5	1.5 4.0	- 4.0	mA
Input Current (terminal 7)	I_7	+6 +12	-6 -12	- 1.0	0.5 1.0	- 0.75	- 2.5	1.0 2.1	- 2.0	mA
Device Dissipation	P_T	+6 +12	-6 -12	- 120	24 120	- 105	- 230	42 220	- 210	mW
DYNAMIC										
Power Gain	G_P	V_{CC} = +9V, f = 10.7 MHz Diff.-Ampl. Config.		-	28	-	-	-	-	dB
		V_{CC} = +9V, f = 100 MHz Cascode Ampl. Config.		-	16	-	-	-	-	dB
Noise Figure	NF	V_{CC} = +9V, f = 100 MHz Cascode Ampl. Config.		-	-	-	-	9	-	dB
Voltage Gain (Diff.)	A	V_{CC} = +12V, f = 1 kHz R_L = 1.6 kΩ		-	40	-	-	45	-	dB

Table 5. GROUP C ELECTRICAL CHARACTERISTICS SAMPLING TESTS (T_A = 25°C, V^+ = + 12V, V^- = -12V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			Min.	Max.	
Input Offset Voltage	V_{IO}		-	5	mV
Input Bias Current	I_I		-	80	μA
Quiescent Oper. Current	I_6 or I_8		2.5	4.0	mA
Input Current (term. 7)	I_7		1.0	2.1	mA
Device Dissipation	P_T		120	220	mW
Power Gain	G_P	V_{CC} = +9V, f = 10.7 MHz Diff.-Ampl. Config.	28	-	dB

TYPICAL CHARACTERISTICS

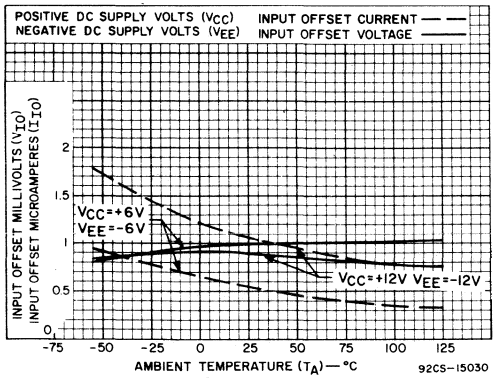


Fig. 2 — Input offset voltage and input offset current for CA3028B.

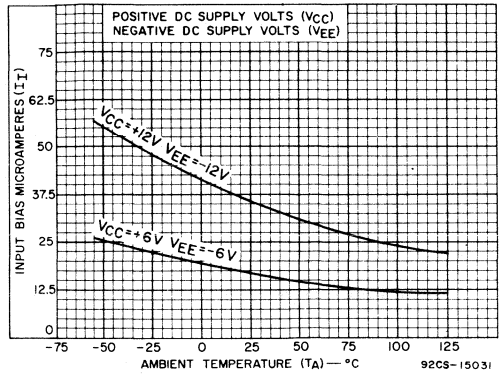


Fig. 3 — Input bias current vs. ambient temperature for CA3028B.

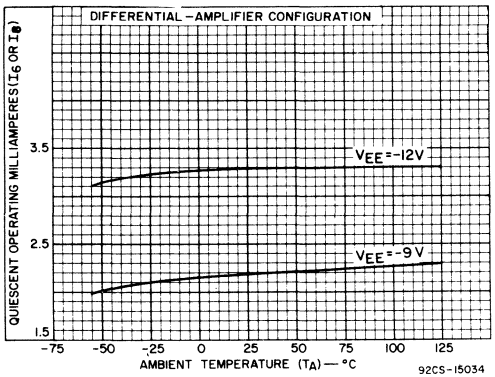


Fig. 4 — Quiescent operating current vs. ambient temperature for CA3028B.

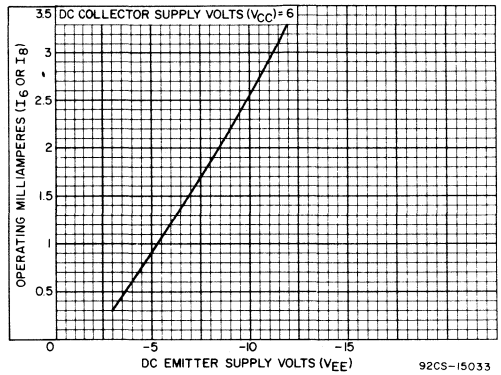


Fig. 5 — Operating current vs. V_{EE} voltage for CA3028B.

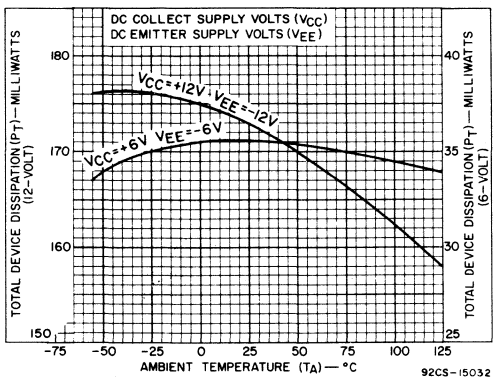


Fig. 6 — Device dissipation vs. temperature for CA3028B.

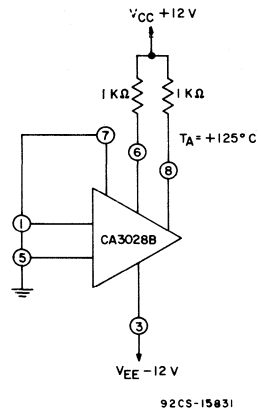


Fig. 7 — Burn-in and operating life test circuit.

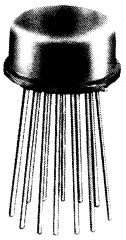
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3039/. . .



H-1463

12-Lead TO-5 Style Package

High-Reliability Diode Array

Six Ultra - Fast Low - Capacitance Matched Diodes

For Applications in Communications and Switching Systems of Aerospace, Military and Critical Industrial Equipment

RCA-CA3039 "Slash" (/) Series type is a high-reliability linear integrated circuit Diode Array intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3039 described in Data Bulletin File No. 343 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3039 can be supplied to six screening levels -- /1N, /1R, /1, /2, /3, and /4 -- which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels -- /N, /R, and standard chip. These screening levels and detailed information on tests, methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883", and in High-Reliability Devices DATABOOK SSD-207.

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on page 3.

The CA3039 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Features:

- **Excellent reverse recovery time — 1 ns typ.**
- **Matched monolithic construction — V_F matched within 5 m V**
- **Low diode capacitance — C_D = 0.65 pF typical at V_R = — 2 V**

Applications:

- **Balanced modulators or demodulators**
- **Ring modulators**
- **High speed diode gates**
- **Analog switches**

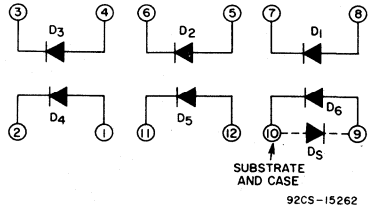


Fig. 1 - Schematic Diagram

ABSOLUTE MAXIMUM RATINGS at T_A = 25 °C

DISSIPATION:
- Any one diode unit . . . . . 100 mW
- Total for device . . . . . 600 mW
- For $T_A > 55$ °C . . . . . derate linearly 5.7 mW/°C

TEMPERATURE RANGE
- Operating . . . . . -55 to + 125 °C
- Storage . . . . . -65 to + 150 °C

LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max . . . . . 265°C

Peak Inverse Voltage, PIV for: D_1-D_5 . . . . . 5 V
D_6 . . . . . 0.5 V
Peak Diode-to-Substrate Voltage, V_{DI} for D_1-D_5 (term. 1,4,5,8 or 12 to term. 10) +20, - 1 V
DC Forward Current, I_F . . . . . 25 mA
Peak Recurrent Forward Current, I_f . . . . . 100 mA
Peak Forward Surge Current, I_f (surge) . . . . . 100 mA

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS TYP.	UNITS	CHARACTERISTIC CURVES FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	0.65	V	2
		1 mA	0.73	V	
		3 mA	0.76	V	
		10 mA	0.81	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 40μA	7	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = −10 μA	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = −4 V	0.016	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = −10 V	0.022	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	0.5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	1	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	−1.9	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	0.65	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	1	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	30	Ω	7
Diode Capacitance	C_D	V_R = −2 V, I_F = 0	0.65	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	3.2	pF	9

Table 1 – Available Screening Level Options (Indicated by Check [√] Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 8-LEAD TO-5 STYLE WITH STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3039	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes A, B, &C	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3039	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2 – Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA3039 H/N

CA3039 H N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	H= Chip Version	/N For /R Description, See R1C-202

Packaged Device, CA3039 T/1N

CA3039 T 1N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	T =TO-5 Style with straight leads	/1N /1R /1 /2 /3 /4 For Description, See R1C-202

*Table 3 – Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25° C	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Each Diode DC Forward Voltage Drop	V_F	I_F = 3 mA	0.69	0.81	±0.010	V

* Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 10.

Table 4 – Final Electrical Tests and Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			−55	+25	+125	−55	+25	+125	
Each Diode: DC Forward Voltage Drop	V_F	I_F = 3 mA	0.82	0.69	0.47	1.0	0.86	0.63	V
DC Reverse Leakage Current	I_R	V_R = −4 V	–	–	–	–	100	–	nA
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 40 μA	–	5	–	–	–	–	V
Between Any Two Diodes: Diode Offset Voltage	$\lvert V_{F1} - V_{F2} \rvert$	I_F = 1 mA	–	–	–	–	8	–	mV
Breakdown Voltage Isolation-to-Substrate		−50 V through a 25 kΩ resistor to terminal 10. Ground terminals 1 through 9, 11 and 12. Measure voltage at terminal 10.	–	–	–	−25	−25	−25	V

Table 5 – Group C Electrical Characteristics Sampling Tests (T_A = 25° C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Each Diode:					
DC Forward Voltage Drop	V_F	I_F = 3 mA	0.69	0.81	V
DC Reverse Leakage Current	I_R	V_R = −4 V	–	100	nA
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 40 μA	5	–	V
Between Any Two Diodes:					
Diode Offset Voltage	$\|V_{F1} - V_{F2}\|$	I_F = 1 mA	–	8	mV

TYPICAL CHARACTERISTICS

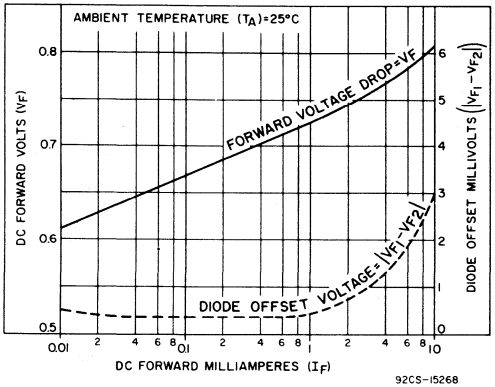


Fig. 2 – DC forward voltage drop (any diode) and diode offset voltage vs DC forward current.

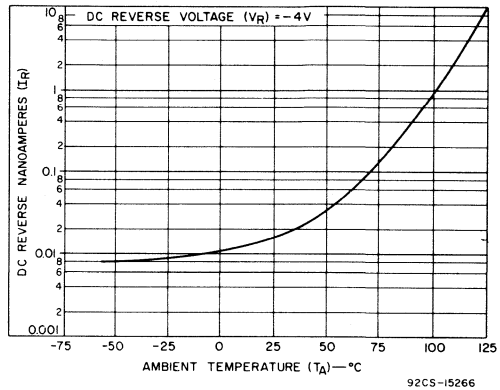


Fig. 3 – DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature.

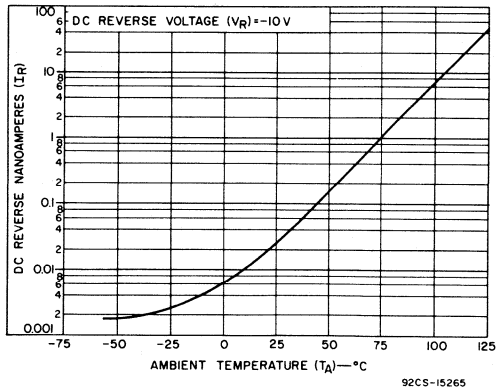


Fig. 4 – DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature.

TYPICAL CHARACTERISTICS – Cont'd.

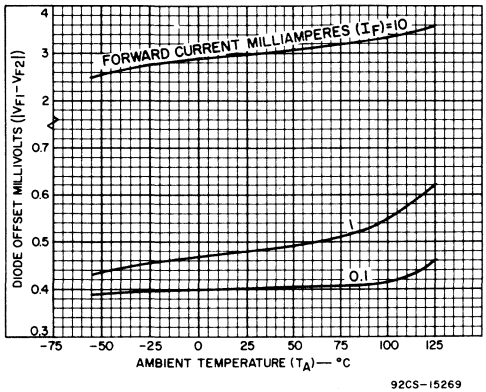


Fig. 5 – Diode offset voltage (any diode) vs temperature.

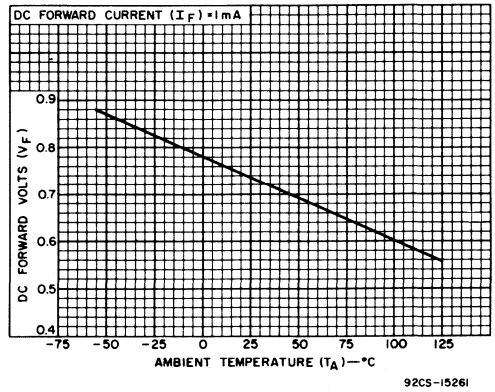


Fig. 6 – DC forward voltage drop (any diode) vs temperature.

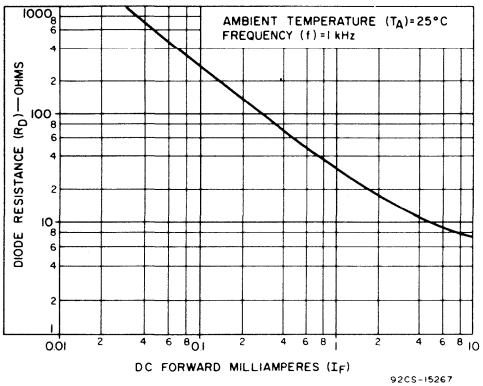


Fig. 7 – Diode resistance (any diode) vs DC forward current.

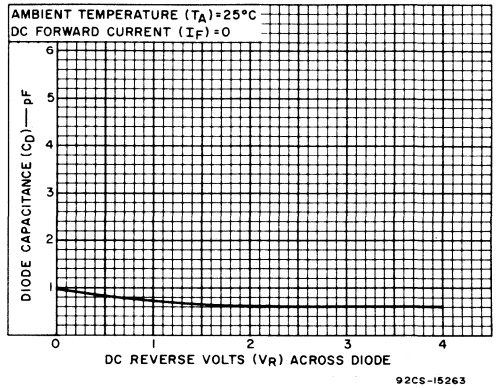


Fig. 8 – Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage.

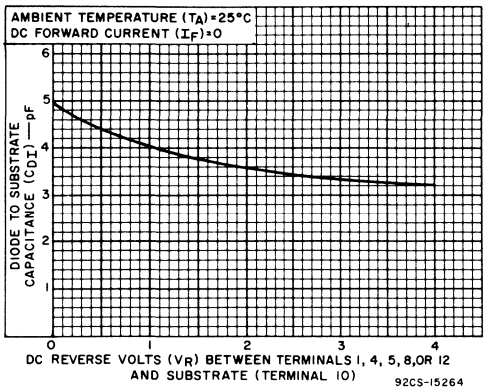


Fig. 9 – Diode-to-substrate capacitance vs reverse voltage.

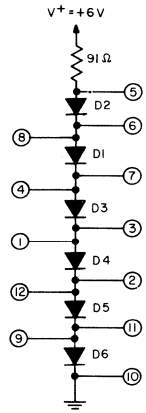


Fig. 10 – Burn-in and operating life test circuit.

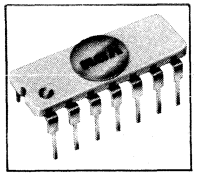
RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3045/. . .



14-Lead Dual In-Line
Ceramic Package

High-Reliability General-Purpose Transistor Array

Three Isolated Transistors and One Differentially-Connected Transistor Pair

For Low-Power Applications at Frequencies Through the VHF Range In Aerospace, Military, and Critical Industrial Equipment

Features:

- **Two matched pairs of transistors**
  V_{BE} matched ±5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- **5 general purpose monolithic transistors**
- **Operation from DC to 120 MHz**
- **Wide operating current range**
- **Low noise figure — 3.2 dB typ. at 1 kHz**
- **Full military temperature range for CA3045 -55 to +125°C**

RCA-CA-3045 "Slash" (/) Series type is a high-reliability linear integrated circuit general-purpose transistor array intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3045 described in Data Bulletin File No. 341 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3045 can be supplied to six screening levels — /1N, /1R, /1, /2, /3, and /4 — which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels — /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883".

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3045 Slash (/) Series type is supplied in the 14-lead dual-in-line ceramic package ("D" suffix) or in chip form ("H" suffix).

Applications:

- **General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF**
- **Custom designed differential amplifiers**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

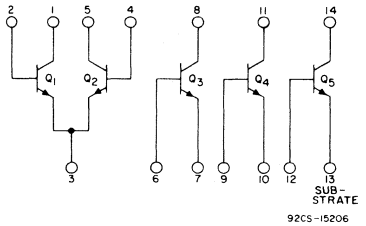


Fig. 1 — Schematic diagram.

Table 1 – Available Screening Level Options (Indicated by Check (√) Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE: 14-LEAD DUAL-IN LINE CERAMIC (D) SUFFIX	PACKAGE: WITH DUAL-IN-LINE FORMED LEADS "DIL-CAN" (S) SUFFIX
PACKAGED DEVICE				
CA3045	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883 Classes "A", "B", & "C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
CHIP			*(H) Suffix*	
CA3045	Custom	/N	√	√
		/R	√	√
	Standard Chip		√	√

Table 2 – Description of RCA Linear IC High-Reliability Part Number

Packaged Device, CA3045D/1N

CA3045 D /1N/

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	D = Dual-In-Line Ceramic	/IN, /IR, /1, /2, /3, /4 — For Description, See R1C-202

Chip Version, CA3045 H/N

CA3045 H /N/

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	H= Chip Version	/N, /R — For Description, R1C-202

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C:

	EACH TRANSISTOR	TOTAL PACKAGE	
POWER DISSIPATION:			
At T_A up to 75°C	300	750	mW
At T_A > 75°C		Derate at 8 mW/°C	
Collector-to-Emitter Voltage, V_{CEO}	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	V
Collector Current, I_C	50	–	mA
TEMPERATURE RANGE:			
Operating		-55 to +125	°C
Storage		-65 to +150	°C
LEAD TEMPERATURE (During Soldering):			
At distance 1/16" ± 1/32" (1.59 mm ±0.79 mm) from case for 10 s max.	265°C		

*The collector of each transistor of the CA3045 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 MIN.	LIMITS Type CA3045 TYP.	LIMITS Type CA3045 MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V	-
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V	-
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA	3
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-	4
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-	
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-	
Input Offset Current for Matched Pair Q_1 and Q_2. $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA	5
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V	6
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	−1.9	-	mV/°C	7
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V	-
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	1.1	-	μV/°C	8

DYNAMIC CHARACTERISTICS							
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB	10(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:							
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ	
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho	
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-	
Admittance Characteristics:							
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-	
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-	
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-	
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-	
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-	9
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF	-
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF	-
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF	-

*Table 3 — Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits**

Electrical Characteristics, at $T_A = 25^oC$ For Each Transistor (Except where otherwise indicated)						
Characteristics	Symbol	Test Conditions	Limits			Units
			Min.	Max.	Max.Δ	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$ (Except Q_5)	5	-	±0.5	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	0.5	±0.15	μA
Input Current	I_I	$I_C = 1mA$, $V_{CE} = 3V$	5	25	±3	μA
Base-to-Emitter Voltage	V_{BE}	$I_C = 1mA$, $V_{CE} = 3V$	0.6	0.8	±0.10	V

*Levels /1 and /2 require pre burn-in electrical and post burn-in electrical tests, and delta limits. Level 3 requires pre burn-in test only. The burn-in and operating life test circuit is shown in Fig. 12.

Table 4 — Final Electrical Tests (For each transistor unless otherwise indicated)

Characteristics	Symbol	Test Conditions	Limits For Indicated Temperature (^oC)						Units
			Minimum			Maximum			
			-55	+25	+125	-55	+25	+125	
STATIC									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	-	20	-	-	-	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	-	15	-	-	-	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$	-	20	-	-	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$ (Except Q5)	-	5	-	-	-	-	V
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	-	-	-	40	-	nA
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	-	-	-	0.5	100	μA
Static Forward Current-Transfer Ratio	h_{FE}	$V_{CE} = 3V$, $I_C = 10mA$	-	30	-	-	-	-	-
		$V_{CE} = 3V$, $I_C = 1mA$	18	40	45	-	-	-	
		$V_{CE} = 3V$, $I_C = 10\mu A$	-	15	-	-	-	-	
Input Offset Current for Differential Pair	$\lvert I_{IO_1} - I_{IO_2} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	2	-	μA
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 10mA$					1.0		V
		$V_{CE} = 3V$, $I_C = 1mA$	0.7	0.6	0.4	1.0	0.8	0.7	
Input Offset Voltage for Differential Pair	$\lvert V_{BE_1} - V_{BE_2} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Input Offset Voltage for Isolated Transistors	V_{IO}	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1mA$, $I_C = 10mA$	-	-	-	-	0.5	-	V

Table 5 – Group A Electrical Sampling Inspection

Characteristics	Symbol	Test Conditions	Limits for Indicated Temperature (°C)						Units
			Minimum			Maximum			
			-55	+25	+125	-55	+25	+125	
STATIC									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	-	20	-	-	-	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	-	15	-	-	-	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$	-	20	-	-	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$ (Except Q_5)	-	5	-	-	-	-	V
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	-	-	-	40	-	nA
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	-	-	-	0.5	100	μA
Static Forward Current-Transfer Ratio	h_{FE}	$V_{CE} = 3V$, $I_C = 10mA$	-	30	-	-	-	-	–
		$V_{CE} = 3V$, $I_C = 1mA$	18	40	45	-	-	200	–
		$V_{CE} = 3V$, $I_C = 10\mu A$	-	15	-	-	-	-	–
Input Offset Current for Differential Pair, (Q_1, Q_2)	$\lvert I_{IO_1} - I_{IO_2} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	-	2	μA
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 1mA$	0.7	0.6	0.4	1.0	0.8	0.70	V
		$V_{CE} = 3V$, $I_C = 10mA$	-	-	-	-	1.0	-	V
Input Offset Voltage for Differential Pair, (Q_1, Q_2)	$\lvert V_{BE_1} - V_{BE_2} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Input Offset Voltage for Isolated Transistors $\lvert Q_3 - Q_4 \rvert$, $\lvert Q_4 - Q_5 \rvert$, $\lvert Q_5 - Q_3 \rvert$	V_{IO}	$V_{CE} = 3V$, $I_C = 1mA$	-	-	-	-	5	-	mV
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1mA$, $I_C = 10mA$	-	-	-	-	0.5	-	V
DYNAMIC									
Gain-Bandwidth Product (Q_3)	f_T	$V_{CE} = 3V$, $I_C = 3mA$, f = 100 MHz	-	300	-	-	-	-	MHz

Table 6 – Group C Electrical Characteristics Sampling Tests
($T_A = 25°C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V)

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$ (Except Q5)	5	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	15	-	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	-	0.5	μA
Input Current	I_I	$V_{CE} = 3$ V, $I_C = 1$ mA	5	25	μA
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3$ V, $I_C = 1$ mA	0.6	0.8	V

STATIC CHARACTERISTICS

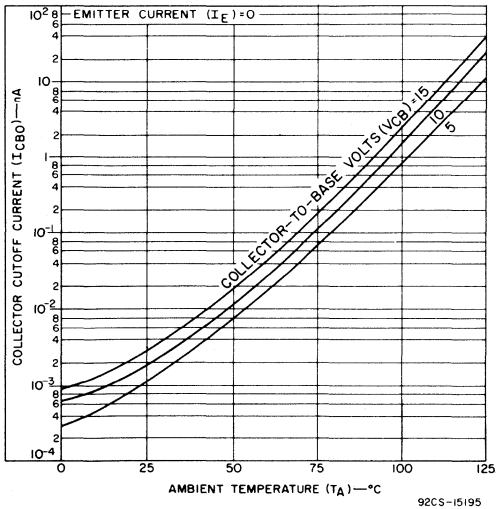


Fig. 2 — Typical collector-to-base cutoff current vs ambient temperature for each transistor.

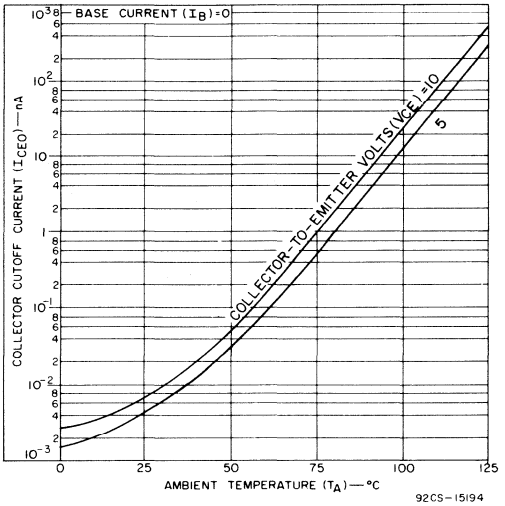


Fig. 3 — Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

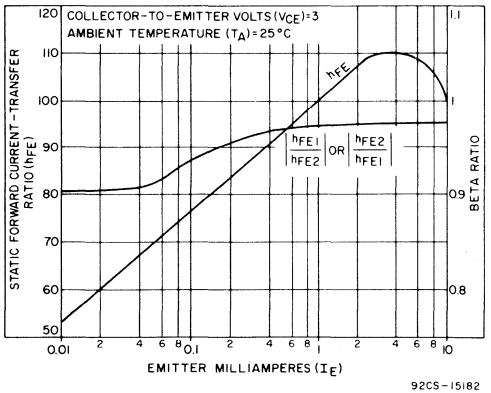


Fig. 4 — Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

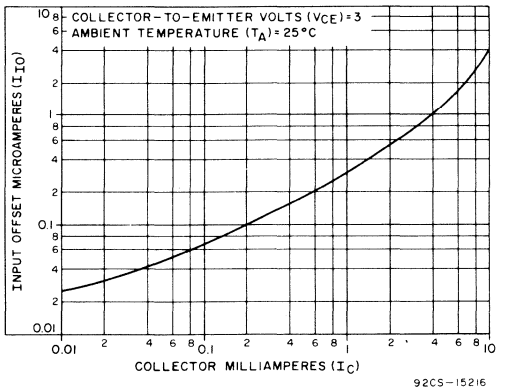


Fig. 5 — Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

STATIC CHARACTERISTICS

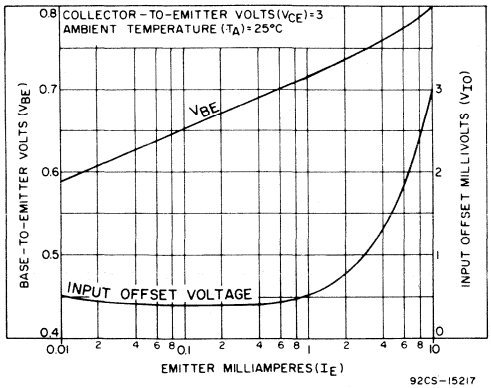


Fig. 6 — Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

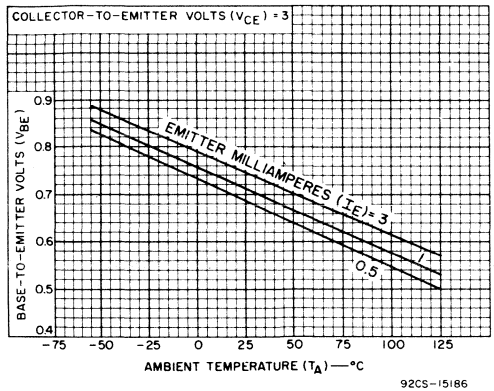


Fig. 7 — Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

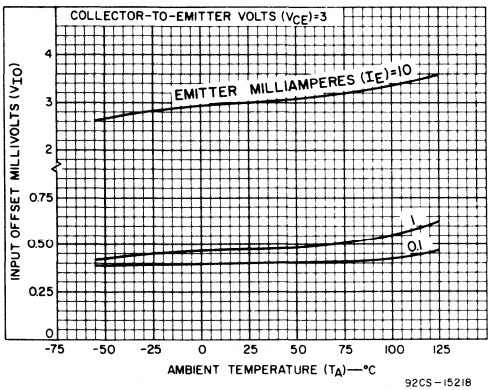


Fig. 8 — Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

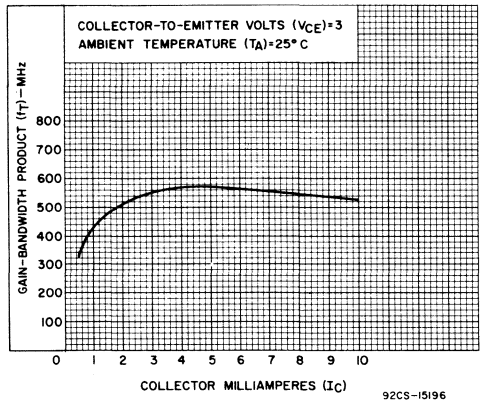


Fig. 9 — Typical gain-bandwidth product vs collector current.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

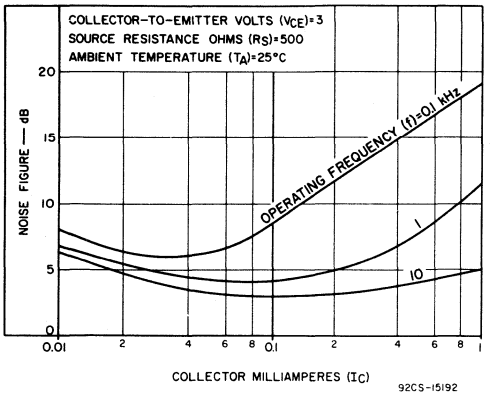


Fig. 10(a) — Typical noise figure vs collector current.

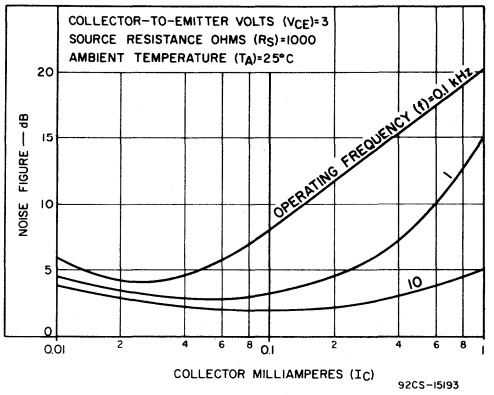


Fig. 10(b) — Typical noise figure vs collector current.

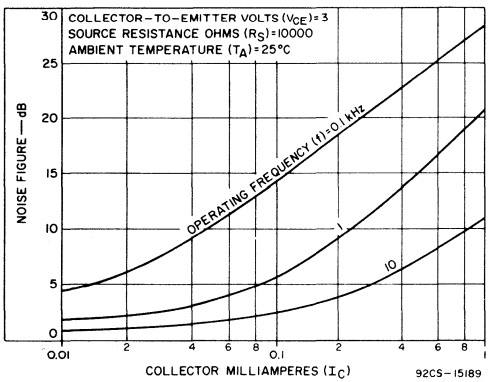


Fig. 10(c) — Typical noise figure vs collector current.

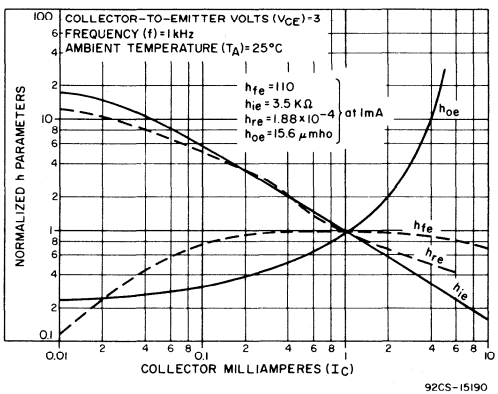


Fig. 11 — Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

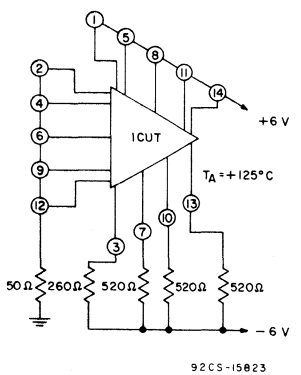


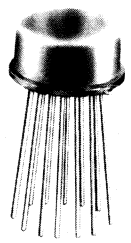
Fig. 12 — Burn-in and operating life test circuit.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CA3049/. . .



12-Lead TO-5 Style Package

High-Reliability Dual High-Frequency Differential Amplifier

For Low-Power Applications at Frequencies up to 500 MHz in Aerospace, Military and Critical Industrial Equipment

Features:

- **Power Gain 23 dB (typ.) at 200 MHz**
- **Noise Figure 4.6 dB (typ.) at 200 MHz**
- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**

RCA-CA3049 "Slash" (/) Series type is a high-reliability linear integrated circuit dual high-frequency differential amplifier intended for low-power applications at frequencies up to 500 MHz in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3049 described in Data Bulletin File No. 611 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3049 can be supplied to six screening levels -- /1N, /1R, /1, /2, /3, and /4 -- which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels -- /N, /R, and standard chip. These screening levels and detailed information on test methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883", and in High-Reliability Devices DATABOOK SSD-207.

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3049 Slash (/) Series type is supplied in the 12-lead TO-5 style package ("T" suffix) or in chip form ("H" suffix).

Applications

- **VHF amplifers**
- **VHF mixers**
- **Multifunction combinations — RF/Mixer/Oscillator; Converter/IF**
- **IF amplifiers (differential and/or cascode)**
- **Product detectors**
- **Doubly balanced modulators and demodulators**
- **Balanced quadrature detectors**
- **Cascade limiters**
- **Synchronous detectors**
- **Balanced mixers**
- **Synthesizers**
- **Balanced (push-pull) cascode amplifiers**
- **Sense amplifiers**

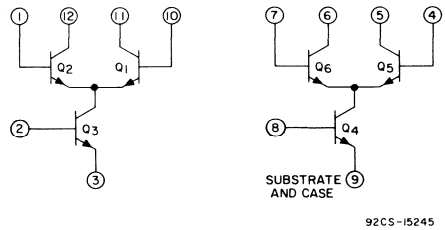


Fig. 1 - Schematic Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

POWER DISSIPATION, P:

Any one transistor	300
Total package	600
For $T_A > 55^oC$ Derate at:	5 mW/^oC

TEMPERATURE RANGE:

Operating	−55 to +125^oC
Storage	−65 to +150^oC

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ±1/32" (1.59 mm ±0.79 mm) from case for 10 s max. . . . . 265^oC

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Table 1 – Available Screening Level Options (Indicated by Check [√] Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 12-Lead TO-5 STYLE WITH STRAIGHT LEADS (T) SUFFIX
PACKAGED DEVICE			
CA3028B	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes A, B, &C	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3028BH	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2 – Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA3049 H/N

CA3049 H /N/

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	H= Chip Version	/N, /R — For Description, See R1C-202 and DATABOOK SSD-207

Packaged Device CA3049/1N

CA3049 T /1N/

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	T =TO-5 Style with straight leads	/1N, /1R, /1, /2, /3, /4 — For Description, See R1C-202 and DATABOOK SSD-207

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		CA3049T LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}			---	0.25	---	mV	4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		---	0.3	---	μA	---
Input Bias Current	I_{IB}				13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\lvert\frac{\Delta V_{IO}}{\Delta T}\rvert$			---	1.1	---	μV/°C	4
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		5	7	---	V	---
DYNAMIC CHARACTERISTICS								
1/f Noise Figure (For Single Transistor)	NF	f = 100 KHz, R_S = 500 Ω, I_C = 1 mA		---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		---	1.35	---	GH_z	11
Collector-Base Capacitance	C_{CB}	I_C = 0	V_{CB} = 5V	--- ---	0.28 0.28	--- ---	pF pF	8
Collector-Substrate Capacitance	C_{CI}	I_C = 0	V_{CI} = 5V	---	1.65	---	pF	8
For Each Differential Amplifier								
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	---	23	---	dB	---
Noise Figure	NF	V_{CC} = 12V	Cascode	---	4.6		dB	---
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9$ = 2 mA	Cascode	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	0.071 + j 0.62	---		21, 23, 25

*Table 3 — Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS at T_A = 25°C	LIMITS MIN.	MAX.	MAX. Δ	UNITS
Input Bias Current Q1, Q2, Q5, Q6	I_I	$I_3 = I_9$ = 2mA V^+ = +6 V	–	25.2	±6	μA
Input Bias Current Q3, Q4	I_I	$I_3 = I_9$ = 2mA V^+ = +6 V	–	50.4	±12	μA
Emitter-to Base Breakdown Voltage Q3, Q4	V_{EBO}	I_E = 10μA I_C = 0	-5.3	–	±1.0	V
Collector Cutoff Current Q1 to Q6	I_{CBO}	V_{CB} = 10 V I_E = 0	–	95	±50	nA

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 12.

Table 4 – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
STATIC (Each Differential Amplifer)									
Input Offset Voltage	V_{IO}		–	–	–	7	5	7.5	mV
Input Offset Current	I_{IO}	$I_3 = I_9 = 2mA$ $V^+ = +6$ V	–	–	–	9	3	3	μA
Input Bias Current	I_I	$I_3 = I_9 = 2mA$ $V^+ = +6$ V	–	–	–	41	33	18	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	–	–	–	100	–	nA
Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$V, $I_C = 1mA$	–	–	–	–	874	–	mV
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	–	15	–	–	–	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	–	20	–	–	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_B = I_E = 0$	–	20	–	–	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	–	5	–	–	–	–	V

Table 5 – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
These tests are the same as the Final Electrical Tests except for the addition of the Dynamic test shown below									
Dynamic Voltage gain (Single-Ended Output)	A	Bias Voltage = 4.2V, f = 10 MHz	–	18	–	–	–	–	dB

Table 6 – Group C Electrical Characteristics Sampling Tests ($T_A = 25^oC$)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Input Offset Voltage	V_{IO}		–	5	mV
Input Bias Current Q_1, Q_2, Q_5, Q_6	I_I	$I_3 = I_9 = 2$ mA, $V+ = +6$ V	–	25.2	μA
Input Bias Current Q_3, Q_4	I_I	$I_3 = I_9 = 2$ mA, $V+ = +6$ V	–	50.4	μA
Power Gain	P_G		19	26	dB

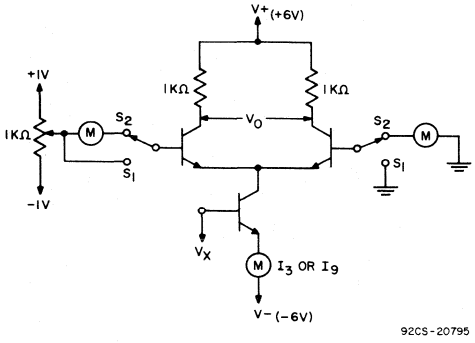
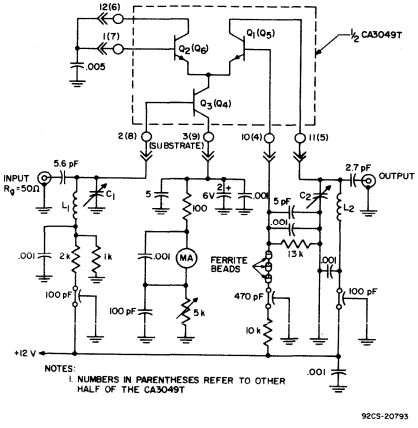


Fig. 2 – Static characteristics test circuit



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.
C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)
All Capacitors in μF Unless Otherwise Indicated
All Resistors in Ohms Unless Otherwise Indicated

Fig. 3 – 200 MHz cascode power gain and noise figure test circuit.

TYPICAL CHARACTERISTICS

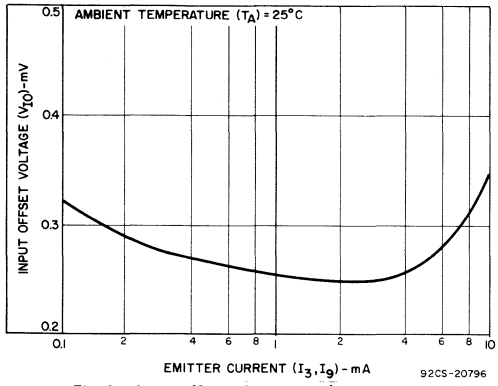


Fig. 4 – Input offset voltage vs. emitter current.

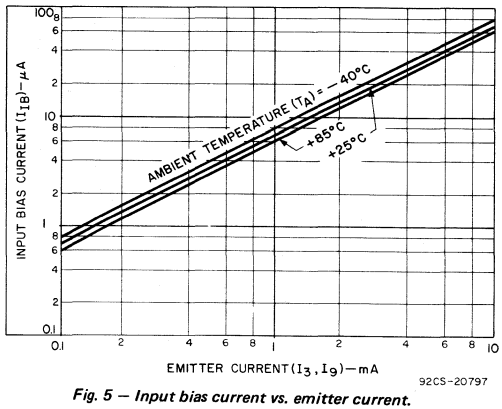


Fig. 5 – Input bias current vs. emitter current.

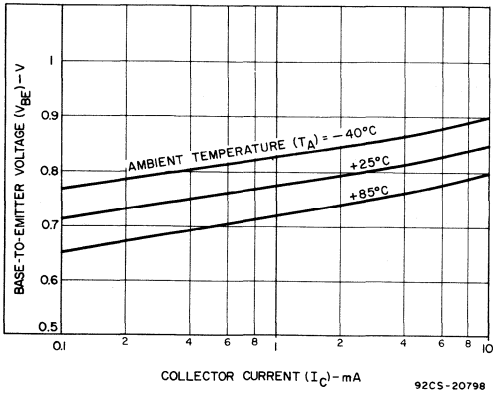


Fig. 6 – Base-to-emitter voltage vs. collector current.

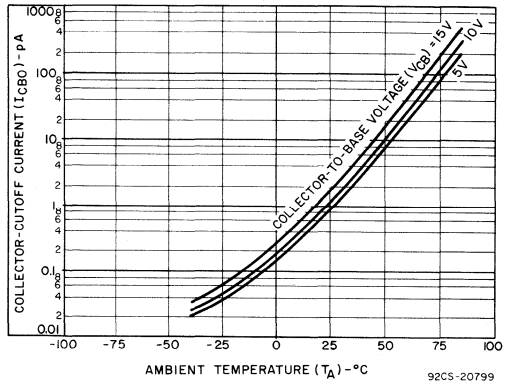


Fig. 7 – Collector-cutoff current vs. temperature.

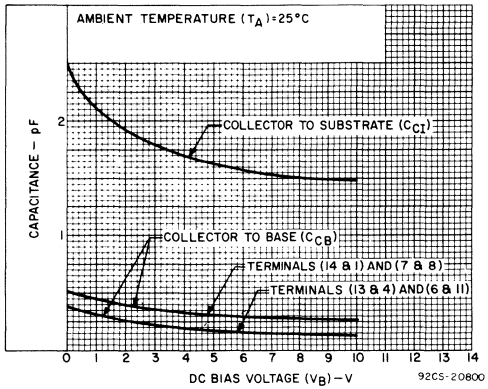


Fig. 8 — Capacitance vs. dc bias voltage.

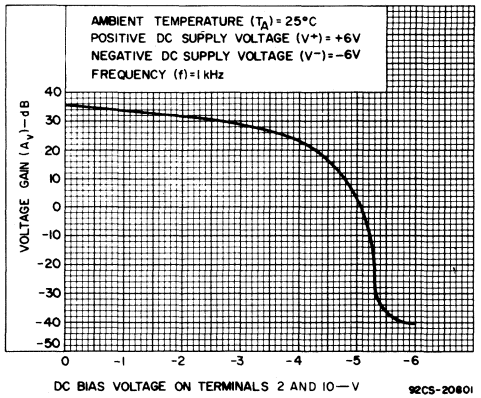


Fig. 9 — Voltage gain vs. dc bias voltage.

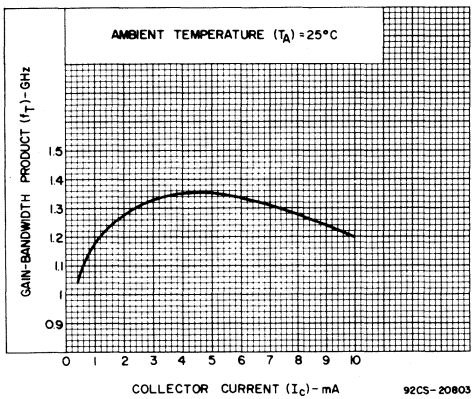


Fig. 10 — Voltage gain vs. frequency.

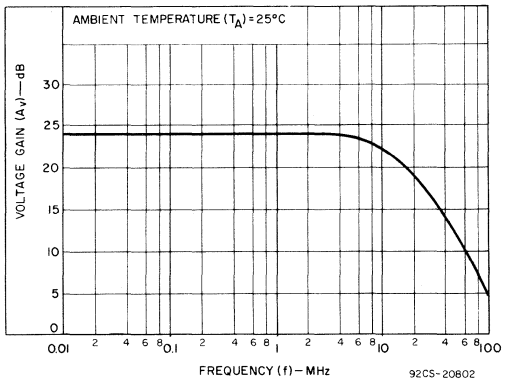


Fig. 11 — Gain-bandwidth product vs. collector current.

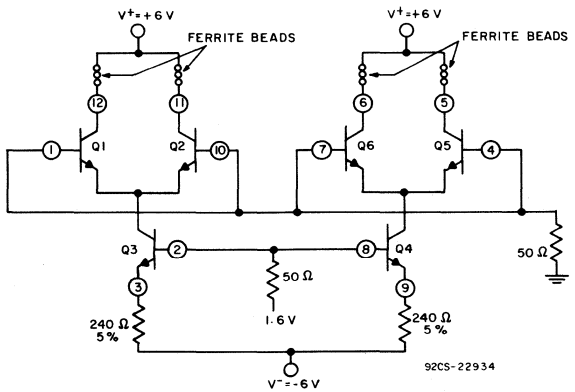


Fig. 12 — Burn-in and operating life test circuit.

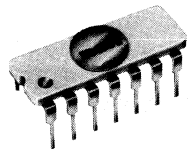
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3058/. . .



14-Lead Dual-In-Line
Ceramic Package

High-Reliability Zero - Voltage Switch

For 50/60 and 400-Hz Thyristor Control Applications
In Aerospace, Military and Critical Industrial Equipment

Features:

- **24 V, 120 V, 208/230 V, 277 V at 50 60, or 400 Hz operation**
- **Differential input**
- **Low balance input current (max.)1μA**
- **Built-in protection circuit for opened or shorted sensor (term. 14)**
- **Sensor range (R_X) - 2 to 100 kΩ**
- **DC mode (term 12)**
- **External trigger (term. 6)**
- **External inhibit (term. 1)**
- **DC supply volts (max.) 14**

RCA-CA3058 "Slash" (/) Series type is a high-reliability linear integrated circuit Zero-Voltage Switch designed to control a thyristor in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. It is intended for applications in aerospace, military, and industrial equipment. It is electrically and mechanically identical with the standard type CA3058 described in Data Bulletin File No. 490 but is specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package type CA3058 can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883", and in High-Reliability Devices DATABOOK SSD-207.

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3058 Slash (/) Series type is supplied in the 14-Lead dual-in-line ceramic package ("D" suffix), or in chip form ("H" Suffix).

Applications

- **Relay control ■ Heater control ■ Photosensitive control**
- **Valve control ■ Lamp control ■ Power one-shot control**
- **Synchronous switching of flashing lights**
- **On-off motor switching**
- **Differential comparator with self-contained power supply for industrial applications**
- **For detailed application information, see application note 1CAN-6182 "Applications of RCA Integrated Circuit Zero-Votlage Switches (CA3058, CA3059, CA3079)"**

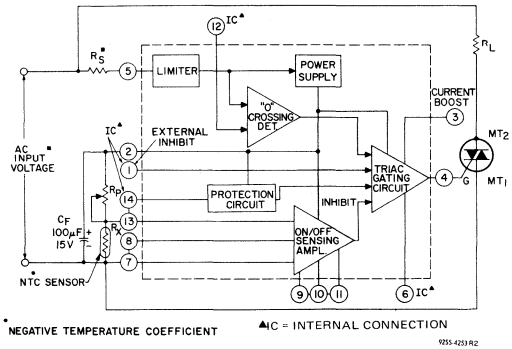


Fig. 1—Functional block diagram.

AC Input Voltage (50/60 to 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

Table 1 — Available Screening Level Options (Indicated by Check (√) Mark)

PART NUMBER	SCREENING LEVEL		PACKAGE 14-LEAD DUAL-IN-LINE CERAMIC (D) SUFFIX
PACKAGED DEVICE			
CA3058	Custom	/1N	√
		/1R	√
	Standard Equivalent to MIL-STD-883 Classes A, B, & C	/1	√
		/2	√
		/3	√
		/4	√
CHIP			*(H) Suffix*
CA3058	Custom	/N	√
		/R	√
	Standard Chip		√

Table 2 — Description of RCA Linear IC High-Reliability Part Number

Chip Version, CA3058D H/N

CA3058D — H — N

	PACKAGE SUFFIX LETTER	SCREENING LEVEL
Part Number (Type Designation)	H= Chip Version	/N, /R — For Description, See R1C-202 and DATABOOK SSD-207

Packaged Device, CA3058 D/IN

CA3058 — D — 1N

	PACKAGE SUFFIX LETTER	SCREENING LEVEL
Part Number (Type Designation)	D = Dual-In-Line Ceramic Package	/1N, /1R, /1, /2, /3, /4 — For Description, See R1C-202 and DATABOOK SSD-207

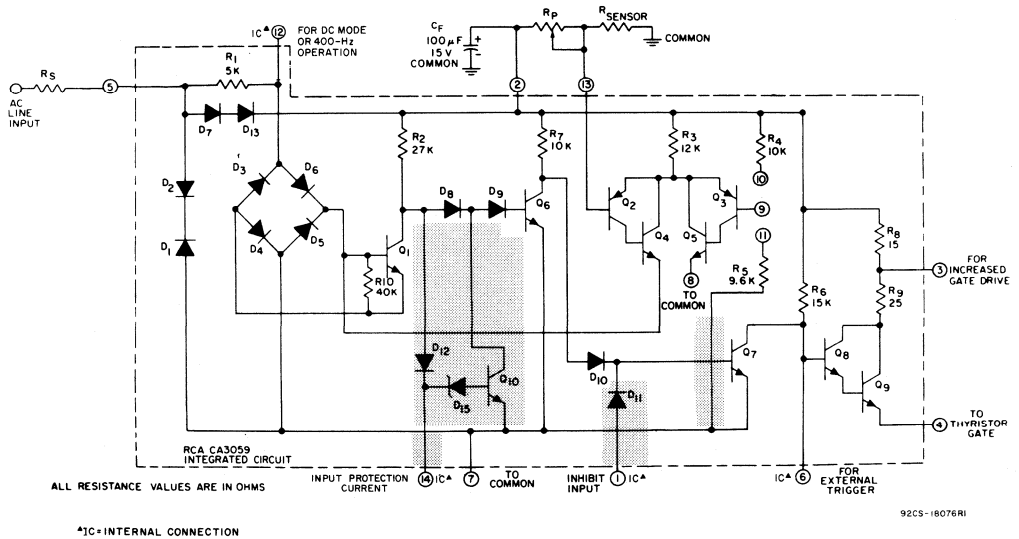


Fig. 2—Schematic diagram of CA3058 zero-voltage switch. For functional block diagram see Fig. 1.

MAXIMUM RATINGS, *Absolute Maximum Values, at* $T_A = 25°C$

DC Supply Voltage (between Terms. 2 and 7)	14	V
DC Supply Voltage (between Terms. 2 and 8)	14	V
Peak Supply Current (Terms. 5 and 7)	±50	mA
Output Pulse Current (Term. 4)	150	mA
Power Dissipation:		
Up to $T_A = 75°C$	700	mW
Above $T_A = 75°C$	Derate Linearly 8	mW/°C
Ambient Temperature Range:		
Operating	-55 to +125°C	
Storage	-65 to +150°C	
Lead Temperature (During soldering)		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	265	°C

MAXIMUM VOLTAGE RATINGS at $T_A = 25°C$

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*
2			0 -15	0 -15	2 -14	0 -14	0 -14	0 -14	0 -14	0 -14	0 -14	*	0 -14	0 -14
3				0 -15	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*
5 Note 1						*	7 -7	*	*	*	*	*	*	*
6 Note 3							14 0	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6
8									10 0	*	*	*	*	*
9										*	*	*	*	*
10											*	*	*	*
11												*	*	*
12 Note 3													*	*
13														*
14 Note 3														

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to -10 volts.

Note 1 – Resistance should be inserted between Term. 5 and external supply or line voltage for limiting current into Term. 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Term. 14 and external supply for limiting current into Term. 14 to less than 2 mA.

NOTE 3: For the CA3079 indicated terminal is internally connected and therefore, should not be used.

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

I_{IN} mA	I_{OUT} mA
10	0.1
150	10
*	*
0.1	150
50	10
*	*
*	*
0.1	2
*	*
*	*
*	*
50	50
*	*
2	2

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	Typical Characteristics Curves Fig. No.	LIMITS Typ.	UNITS
For Operating at 120V rms, 50-60 Hz (AC Line Voltage)•					
DC Supply Voltage: Inhibit Mode At 50/60 Hz	V_S	R_S = 10 k Ω, I_L = 0	3b	6.5	V
At 400 Hz		R_S = 10 k Ω, I_L = 0	–	6.8	V
At 50/60 Hz		R_S = 5 k Ω, I_L = 2 mA	3c	6.4	V
Pulse Mode At 50/60 Hz		R_S = 10 k Ω, I_L = 0	3b	6.4	V
At 400 Hz		R_S = 10 k Ω, I_L = 0	–	6.7	V
At 50/60 Hz		R_S = 5 k Ω, I_L = 2 mA	3c	6.3	V
At 50/60 Hz		R_S = 10 k Ω, I_L = 0 T_A = -55 to 125°C	–	–	V
Gate Trigger Current	I_{GT}(4)	Terms 3 and 2 connected, V_{GT}=1V	4	105	mA
Peak Output Current (Pulsed): With Internal Power Supply	I_{OM}(4)	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	5b	84	mA
		Terms.3 and 2 connected, Gate Trigger Voltage (V_{GT}) = 0	5b	124	mA
With External Power Supply	I_{OM}(4)	Term. 3 open, V^+ = 12V, V_{GT} = 0	6b, c	170	mA
		Terms 3 and 2 connected V^+ = 12V, V_{GT} = 0	6b, c	240	mA
Inhibit Input Ratio:	V_9/V_2	Voltage Ratio of Term. 9 to 2 T_A = -55 to 125°C	7b	0.485 –	–
Total Gate Pulse Duration:* For positive dv/dt 50-60 Hz	t_P	C_{EXT} = 0		100	μs
400 Hz	t_P	C_{EXT} = 0, R_{EXT} = ∞		12	μs
For negative dv/dt 50-60 Hz	t_N	C_{EXT} = 0		100	μs
400 Hz	t_N	C_{EXT} = 0, R_{EXT} = ∞		10	μs
Pulse Duration After Zero Crossing (50-60Hz): For positive dv/dt	t_{P1}	C_{EXT} = 0 R_{EXT} = ∞		50	μs
For negative dv/dt	t_{N1}			60	μs
Output Leakage Current Inhibit Mode:	I_4	T_A = -55 to 125°C	8	0.001	μA
Input Bias Current:	I_I			220	nA
Common-Mode Input Voltage Range	V_{CMR}	Terms. 9 and 13 connected		1.5 to 5	V
Sensitivity ≠ (Pulse Mode)	ΔV_{13}	Term. 12 open	9	6	mV

≠Required voltage change at Term.13 to either turn OFF the triac when ON or turn ON the triac when OFF.

•The values given in the Electrical Characteristics Chart at 120V also apply for operation at input voltages of 24V, 208/230V, and 277V., except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in Fig. 2, for the specified input voltage.

*Table 3 — Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS at T_A = 25°C	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
DC Supply Voltage	V_s	R_s = 10 kΩ, I_L = 0	6.0	7.0	±0.2	V
Output Leakage Current (Inhibit Mode)	I_4		–	10	±0.5	μA
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM}(4)	Terminal 3 Open, V_{GT}=0	50	–	±10	mA
Input Bias Current	I_I		–	1.0	±0.2	μA

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 11.

Table 4 — Final Electrical Tests and Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS f = 50/60 Hz	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
DC Supply Voltage	V_s	R_s = 10 kΩ, I_L = 0	5.5	6.0	5.5	7.5	7.0	7.5	V
Output Leakage Current (Inhibit Mode)	I_4		–	–	–	20	10	20	μA
Input Bias Current	I_I		–	–	–	1.0	1.0	1.0	μA
Inhibit Input Ratio	V_G/V_Z	Voltage ratio of terminal 9 to terminal 2.	0.450	0.465	0.450	0.520	0.520	0.520	
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM} (4)	Terminal 3 open, V_{GT} = 0	–	50	–	–	–	–	mA
		Terminals 2 and 3 shorted, V_{GT} = 0	–	90	–	–	–	–	mA
Pulse Duration After Zero Crossing:									
For Positive dv/dt		C external = 0	–	70	–	–	140	–	μS
For Negative dv/dt		R external = 0	–	70	–	–	140	–	μS

Table 5 — Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS f = 50/60 Hz	LIMITS		UNITS
			MIN.	MAX.	
DC Supply Voltage	V_S	R_S = 10 kΩ, I_L = 0	5.9	7.1	V
Output Leakage Current (Inhibit Mode)	I_4		–	11	μA
Peak Output Current (Pulsed) With Internal Power Supply	I_{OM} (4)	Terminal 3 Open, V_{GT} = 0	45	–	mA
Input Bias Current	I_I		–	1.2	μA

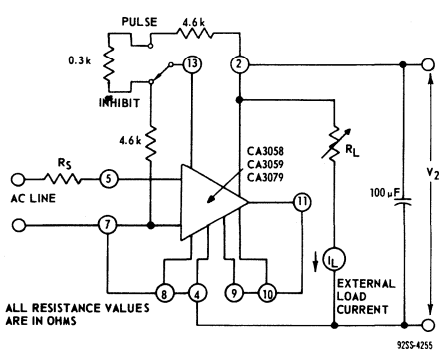


Fig. 3a—DC supply voltage test circuit

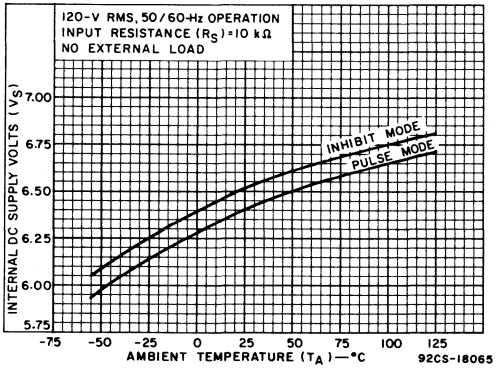


Fig. 3b—DC supply voltage vs. T_A

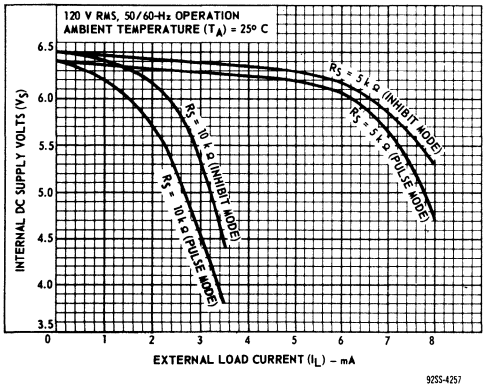


Fig. 3c—DC supply voltage vs. external load current

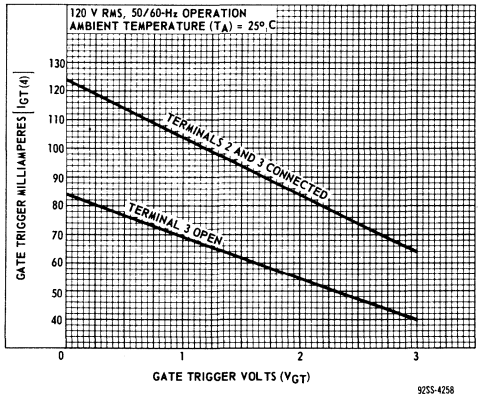


Fig. 4—Gate trigger current vs. gate trigger voltage

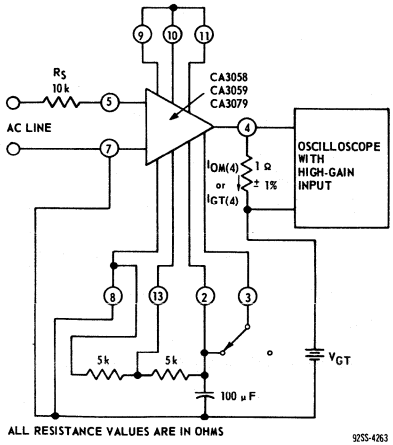


Fig. 5a—Peak output (pulsed) and gate trigger current with internal power supply test circuit

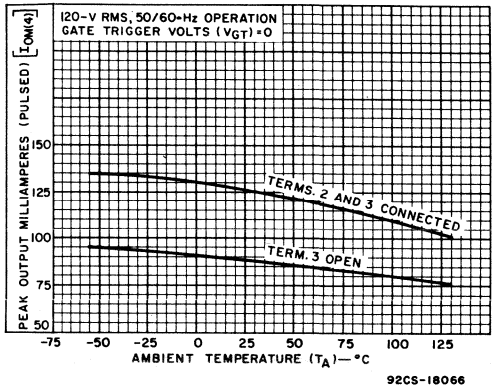


Fig. 5b—I_{OM} vs. T_A

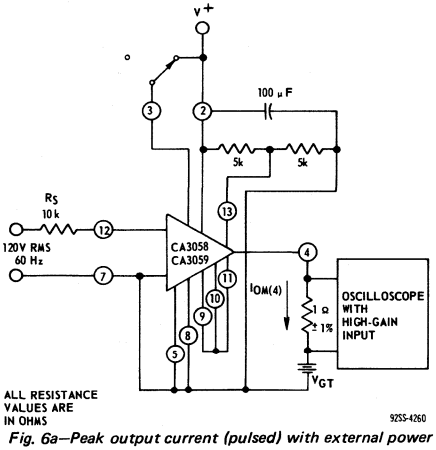


Fig. 6a—Peak output current (pulsed) with external power supply test circuit

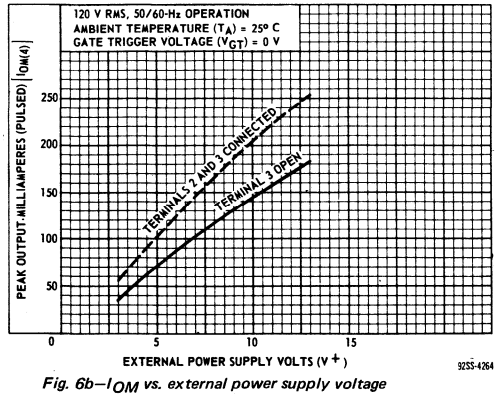


Fig. 6b—I_{OM} vs. external power supply voltage

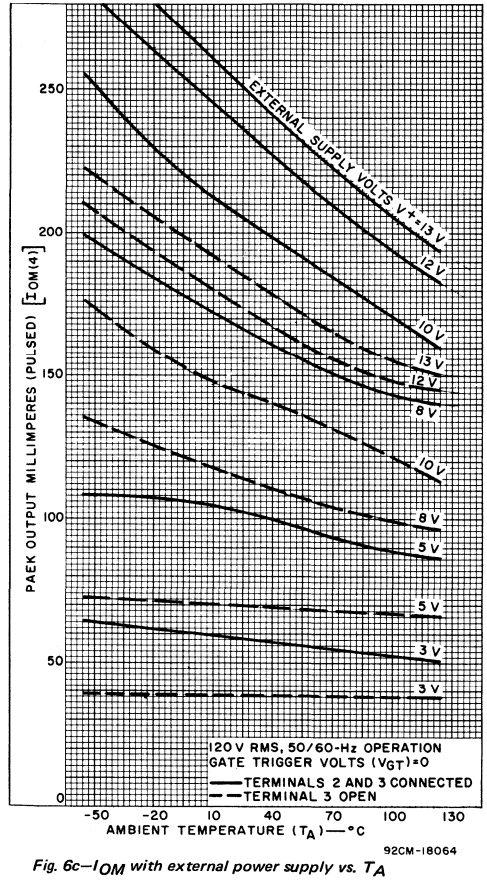


Fig. 6c—I_{OM} with external power supply vs. T_A

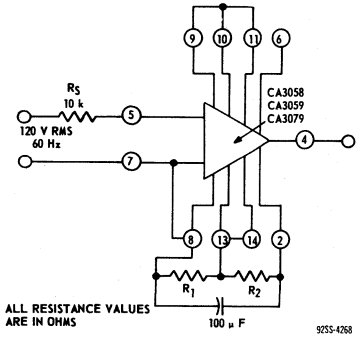


Fig. 7a—Input inhibit ratio test circuit.

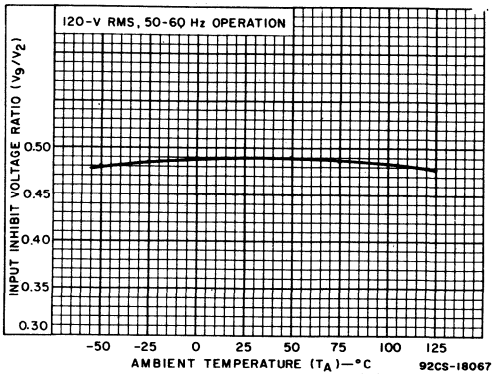


Fig. 7b—Input inhibit voltage ratio vs. T_A

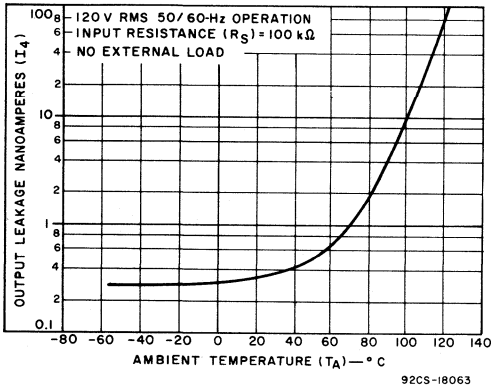


Fig. 8—Output leakage current (inhibit mode) vs. T_A

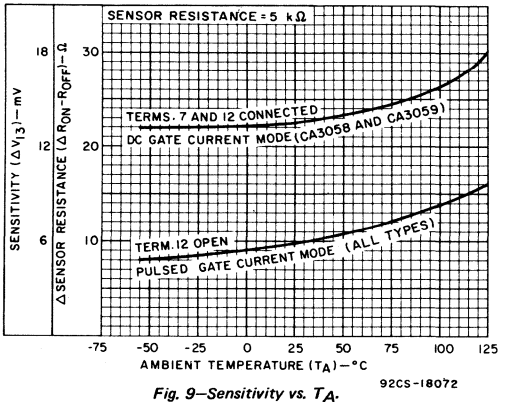


Fig. 9—Sensitivity vs. T_A.

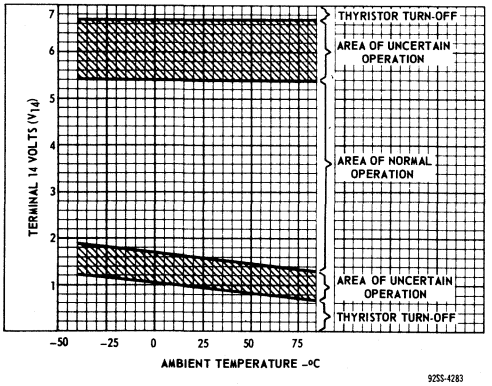


Fig. 10—Operating regions for built-in protection circuit

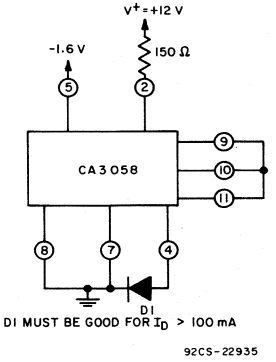


Fig. 11—Burn-in and operating life test circuit.

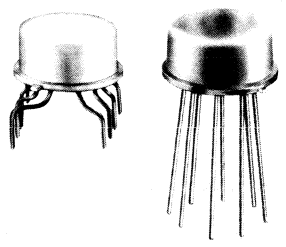
RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CA3080/. . ., CA3080A/. . .



H-1787
8-LEAD TO-5 Style Package with Dual-In-Line Formed Leads

H-1528
8-LEAD TO-5 Style Package

High-Reliability Operational Transconductance Amplifiers Gateable-Gain Blocks

For Applications in Aerospace, Military and Critical Industrial Equipment

Features:

- **Slew rate (unity gain, compensated): 50 V/μs**
- **Adjustable power consumption: 10 μW to 30 mW**
- **Flexible supply voltage range: ±2 V to ±15 V**
- **Fully adjustable gain: 0 to $g_m R_L$ limit**
- **Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)**
- **Extended g_m linearity: 3 decades**
- **Hermetic package: 8-lead TO-5 style**

RCA-CA3080 and CA3080A "Slash" (/) Series types are high-reliability linear integrated circuit Operational Transconductance Amplifiers. These gateable-gain blocks, which utilize the same unique OTA (Operational Transconductance Amplifier) concept first introduced in the RCA-CA3060, are intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard types CA3080 and CA3080A described in Data Bulletin File No. 475 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package types CA3080 and CA3080A can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /N, /R, and standard chip. These screening levels and detailed information on tests methods, procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883",

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3080 and CA3080A Slash (/) Series types are supplied in the 8-lead TO-5 style package ("T" suffix), in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

Applications:

- **Sample and hold**
- **Multiplex**
- **Voltage follower**
- **Multiplier**
- **Comparator**

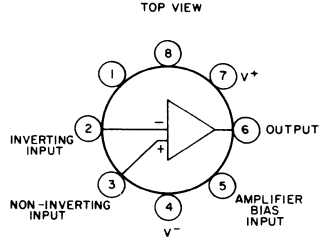


Fig. 1 – Functional diagram of CA3080 and CA3080A.

Table 1 – Available Screening Level Options (Indicated by Check [√] Mark)

PART NUMBER	SCREENING LEVEL		Package 8-Lead TO-5 Style: With Straight Leads (T) Suffix	Package 8-Lead TO-5 Style: With Dual-In-Line Formed Leads DIL-CAN (S) Suffix
PACKAGED DEVICE				
CA3080 CA3080A	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883 Classes A, B, &C	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
CHIP				*(H) Suffix*
CA3080 CA3080A	Custom	/N		√
		/R		√
	Standard Chip			√

Table 2 – Description of RCA Linear IC High-Reliability Part Numbers

Chip Version, CA3080AH/N

CA3080A / H / N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	H= Chip Version	/N, /R: For Description, See R1C-202 and DATABOOK SSD-207

Packaged Device, CA3080A T/IN

CA3080A / T / 1N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	T = TO-5 Style with straight leads S = TO-5 Style with Dual-In-Line Formed Leads (DILCAN)	/1N, /1R, /1, /2, /3, /4: For Description, See R1C-202 and DATABOOK SSD-207

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC Supply Voltage (between V^+ and V^- terminals)	36 V
Differential Input Voltage	±5 V
DC Input Voltage	V^+ to V^-
Input Signal Current	1 mA
Amplifier Bias Current	2 mA
Output Short-Circuit Duration	Indefinite
Device Dissipation	125 mW
Temperature Range:	
Operating	
CA3080	0 to 70 °C
CA3080A	–55 to + 125 °C
Storage	65 to +150 °C
Lead Temperature (During Soldering):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+ 300 °C

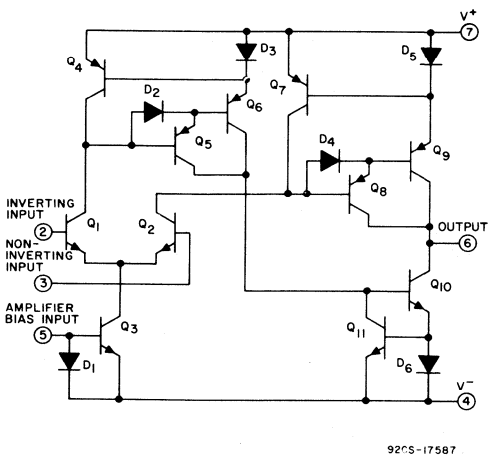


Fig. 2 – Schematic diagram for CA3080 and CA3080A.

ELECTRICAL CHARACTERISTICS
For Equipment Design — CA3080

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS			UNITS
		Circuit Fig.	$V^+ = 15V$, $V^- = -15V$, $I_{ABC} = 500\,\mu A$, $T_A = 25^oC$ (unless indicated otherwise)	Typical Characteristics Curves Fig.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{IO}	–		3	–	0.4	5	mV
Input Offset Current	I_{IO}	–		4	–	0.12	0.6	μA
Input Bias Current	I_I	–		5	–	2	5	μA
Forward Transconductance (large signal)	g_m	–		12	6700	9600	13000	μmho
Peak Output Current	$\lvert I_{OM} \rvert$	–	$R_L = 0$	6	350	500	650	μA
Peak Output Voltage: Positive	V_{OM}^+	–	$R_L = \infty$	7	12	13.5	–	V
Negative	V_{OM}^-				−12	−14.4	–	
Amplifier Supply Current	I_A	–		8	0.8	1	1.2	mA
Device Dissipation	P_D	–		9	24	30	36	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	–		–	–	–	150	$\mu V/V$
Negative	$\Delta V_{IO}/\Delta V^-$				–	–	150	
Common-Mode Rejection Ratio	CMRR	–		–	80	110	–	dB
Common-Mode Input-Voltage Range	V_{CMR}	–		7	12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I	–			10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only For Design Guidance — CA3080

Input Offset Voltage	V_{IO}	$I_{ABC} = 5\,\mu A$	3	0.3	mV
Input Offset Voltage Change	$\lvert \Delta V_{IO} \rvert$	Change in V_{IO} between $I_{ABC} = 500\,\mu A$ and $I_{ABC} = 5\,\mu A$	–	0.2	mV
Peak Output Current	I_{OM}	$I_{ABC} = 5\,\mu A$	6	5	μA
Peak Output Voltage: Positive	V_{OM}^+	$I_{ABC} = 5\,\mu A$	7	13.8	V
Negative	V_{OM}^-			−14.5	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	10	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36V$		0.3	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4V$	11	0.008	nA
Amplifier Bias Voltage	V_{ABC}			0.71	V
Slew Rate: Maximum (uncompensated)	SR		–	75	V/μs
Unity Gain (compensated)				50	
Open-Loop Bandwidth	BW_{OL}	–	–	2	MHz
Input Capacitance	C_I	f = 1 MHz		3.6	pF
Output Capacitance	C_O	f = 1 MHz		5.6	pF
Output Resistance	R_O			15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz		0.024	pF

ELECTRICAL CHARACTERISTICS
For Equipment Design

CA3080A

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS: $V^+ = 15\,V, V^- = -15\,V$, $I_{ABC} = 500\,\mu A$, $T_A = 25^oC$ (unless indicated otherwise)	Typical Characteristics Curves Fig.	LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\,\mu A$	3	–	0.3	2	mV
				–	0.4	2	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	Change in V_{IO} between $I_{ABC} = 500\,\mu A$ and $I_{ABC} = 5\,\mu A$	3	–	0.1	3	mV
Input Offset Current	I_{IO}		4	–	0.12	0.6	μA
Input Bias Current	I_I		5	–	2	5	μA
Forward Transconductance (large signal)	g_m		12	7700	9600	12000	μmho
Peak Output Current	$\lvert I_{OM}\rvert$	$I_{ABC} = 5\,\mu A, R_L = 0$	6	3	5	7	μA
		$R_L = 0$		350	500	650	
		$R_L = 0, T_A = -55$ to $+125^oC$		300	–	–	
Peak Output Voltage:			7				V
Positive	V^+_{OM}	$I_{ABC} = 5\,\mu A$		12	13.8	–	
Negative	V^-_{OM}	$R_L = \infty$		−12	−14.5	–	
Positive	V^+_{OM}	$R_L = \infty$		12	13.5	–	
Negative	V^-_{OM}			−12	−14.4	–	
Amplifier Supply Current	I_A		8	0.8	1	1.2	mA
Device Dissipation	P_D		9	24	30	36	mW
Input Offset Voltage Sensitivity:			–				μV/V
Positive	$\Delta V_{IO}/\Delta V^+$			–	–	150	
Negative	$\Delta V_{IO}/\Delta V^-$			–	–	150	
Magnitude of Leakage Current		$I_{ABC} = 0, V_{TP} = 0$	10	–	0.08	5	nA
		$I_{ABC} = 0, V_{TP} = 36\,V$		–	0.3	5	
Differential Input Current		$I_{ABC} = 0, V_{DIFF} = 4\,V$	11	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR		–	80	110	–	dB
Common-Mode Input-Voltage Range	V_{CMR}		7	12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I			10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only For Design Guidance

CA3080A

Amplifier Bias Voltage	V_{ABC}			0.71	V
Slew Rate:	SR		–		V/μs
Maximum (uncompensated)				75	
Unity Gain (compensated)				50	
Open-Loop Bandwidth	BW_{OL}	–	–	2	MHz
Input Capacitance	C_I	f = 1 MHz		3.6	pF
Output Capacitance	C_O	f = 1 MHz		5.6	pF
Output Resistance	R_O			15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz		0.024	pF

Table 3 – Final Electrical Tests

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = +15$ V, $I_{ABC} = 0.5$ mA, $V^- = -15$ V		LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM −55	MINIMUM +25	MINIMUM +125	MAXIMUM −55	MAXIMUM +25	MAXIMUM +125	UNITS
Input Offset Voltage	V_{IO}		CA3080	–	–	–	6	5	6	mV
			CA3080A	–	–	–	5	2	5	
Input Offset Current	I_{IO}		CA3080	–	–	–	1.2	0.6	0.7	μA
			CA3080A	–	–	–	1.2	0.6	0.7	
Input Bias Current	I_I		CA3080	–	–	–	8	5	8	μA
			CA3080A	–	–	–	8	5	8	
Forward Transconductance	g_m		CA3080	5400	6700	5400	13000	13000	20000	umho
			CA3080A	4000	4000	4000	9000	12000	18000	
Peak Output Voltage Positive	$+V_{OM}$	$R_L = \infty$	CA3080 CA3080A	11.6	12	12	–	–	–	V
Peak Output Voltage Negative	$-V_{OM}$	$R_L = \infty$	CA3080 CA3080A	11.8	12	12	–	–	–	V
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	CA3080	350	350	320	750	650	750	μA
		$R_L = 0$	CA3080A	350	350	320	750	650	750	
Amplifier Supply Current	I_A		CA3080	0.7	0.8	0.7	1.4	1.2	1.4	mA
			CA3080A	0.7	0.8	0.7	1.4	1.2	1.4	
Common-Mode Rejection Ratio	C_{MRR}		CA3080	80	80	80	–	–	–	dB
			CA3080A	80	80	80	–	–	–	
Supply Voltage Rejection Ratio	V_{RR}		CA3080	–	–	–	150	150	150	μV/V
			CA3080A	–	–	–	150	150	150	

Table 4 – Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^- = -15$ V, $V^+ = +15$ V, $I_{ABC} = 0.5$ mA		LIMITS FOR INDICATED TEMPERATURES (°C) MINIMUM −55	MINIMUM +25	MINIMUM +125	MAXIMUM −55	MAXIMUM +25	MAXIMUM +125	UNITS
Input Offset Voltage	V_{IO}		CA3080	–	–	–	6	5	6	mV
			CA3080A	–	–	–	5	2	5	
Input Offset Current	I_{IO}		CA3080	–	–	–	1.2	0.6	0.7	μA
			CA3080A	–	–	–	1.2	0.6	0.7	
Input Bias Current	I_I		CA3080	–	–	–	8	5	8	μA
			CA3080A	–	–	–	8	5	8	
Forward Transconductance	g_m		CA3080	5400	6700	5400	13000	13000	20000	umho
			CA3080A	4000	4000	4000	9000	12000	18000	
Peak Output Voltage Positive	$+V_{OM}$	$R_L = \infty$	CA3080 CA3080A	11.6	12	12	–	–	–	V
Peak Output Voltage Negative	$-V_{OM}$	$R_L = \infty$	CA3080 CA3080A	11.8	12	12	–	–	–	V
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	CA3080	350	350	320	750	650	750	μA
		$R_L = 0$	CA3080A	350	350	320	750	650	750	
Amplifier Supply Current	I_A		CA3080	0.7	0.8	0.7	1.4	1.2	1.4	mA
			CA3080A	0.7	0.8	0.7	1.4	1.2	1.4	
Common-Mode Rejection Ratio	C_{MRR}		CA3080	80	80	80	–	–	–	dB
			CA3080A	80	80	80	–	–	–	
Supply Voltage Rejection Ratio	V_{RR}		CA3080	–	–	–	150	150	150	μV/V
			CA3080A	–	–	–	150	150	150	
Differential Input Current		$I_{ABC} = 10$ mA, $V_{DIFF} = 4$ V	CA3080	–	–	–	–	7	–	nA
		$I_{ABC} = 10$ mA, $V_{DIFF} = 4$ V	CA3080A	–	–	–	–	5	–	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	CA3080	–	–	–	–	7	–	nA
		$I_{ABC} = 0$, $V_{TP} = 0$	CA3080A	–	–	–	–	5	–	
		$I_{ABC} = 0$, $V_{TP} = 36$	CA3080	–	–	–	–	7	–	nA
		$I_{ABC} = 0$, $V_{TP} = 36$	CA3080A	–	–	–	–	5	–	

*Table 5 — Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS AT T_A = 25° C V^+ = +15 V, V^- = −15 V	LIMITS MIN.	LIMITS MAX.	LIMITS MAX. Δ	UNITS
Input Offset Voltage	V_{IO}	CA3080	–	5	±0.2	mV
		CA3080A	–	2	±0.15	
Input Offset Current	I_{IO}	CA3080	–	0.6	±0.05	μA
		CA3080A	–	0.6	±0.05	
Input Bias Current	I_I	CA3080	–	5	±0.25	μA
		CA3080A	–	5	±0.25	
Forward Transconductance	g_m	CA3080	6700	13000	±3000	umho
		CA3080A	7700	12000	±3000	

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in and operating life test circuit is shown in Fig. 13.

Table 6 — Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = +15 V, V^- = −15 V	LIMITS MIN.	LIMITS MAX.	UNITS
Input Offset Voltage	V_{IO}	CA3080	–	6.5	mV
		CA3080A	–	5.5	
Input Offset Current	I_{IO}	CA3080	–	1.2	μA
		CA3080A	–	1.2	
Input Bias Current	I_I	CA3080	–	10	μA
		CA3080A	–	10	
Forward Transconductance to Terminal No. 1	g_m	CA3080	6500	14000	umho
		CA3080A	7000	13000	
Peak Output Current	$\lvert I_{OM} \rvert$	CA3080	300	700	μA
		CA3080A	300	700	
Peak Output Voltage	$+V_{OM}$	CA3080	11	–	V
		CA3080A	11	–	
	$-V_{OM}$	CA3080	−11	–	
		CA3080A	−11	–	

Typical Characteristics Curves for the CA3080 and CA3080A

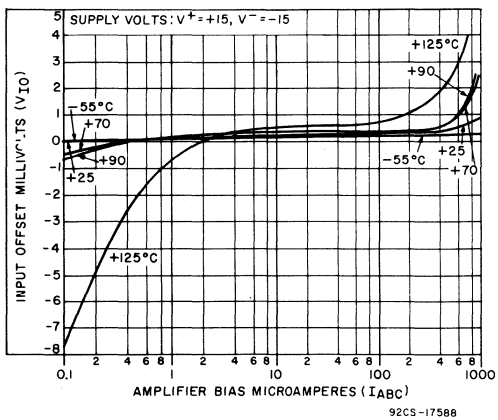


Fig. 3 — Input offset voltage vs. amplifier bias current.

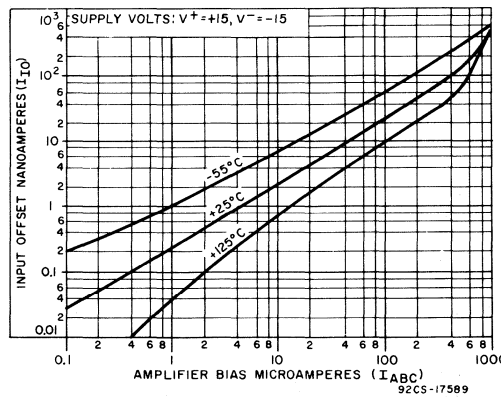


Fig. 4 — Input offset current vs. amplifier bias current.

Typical Characteristics Curves for the CA3080 and CA3080A (Cont'd.)

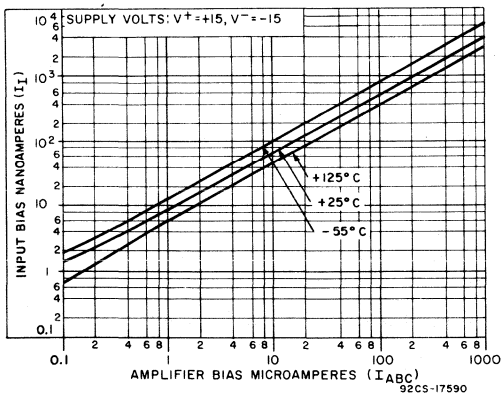


Fig. 5 – Input bias current vs. amplifier bias current.

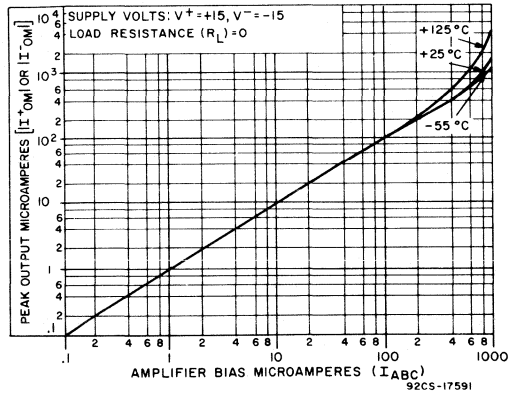


Fig. 6 – Peak output current vs. amplifier bias current.

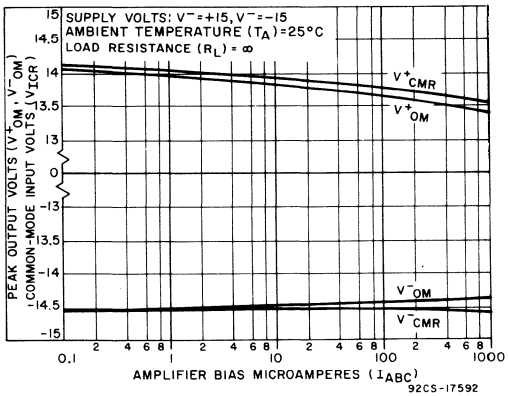


Fig. 7 – Peak output voltage vs. amplifier bias current.

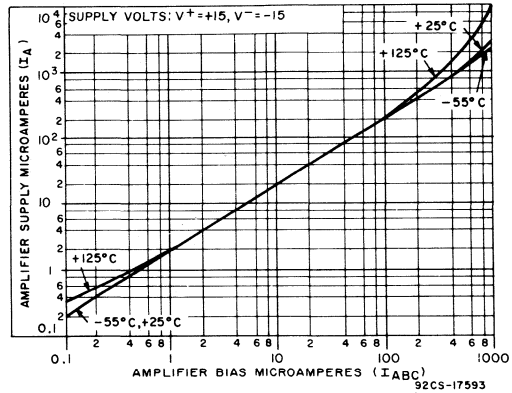


Fig. 8 – Amplifier supply current vs. amplifier bias current.

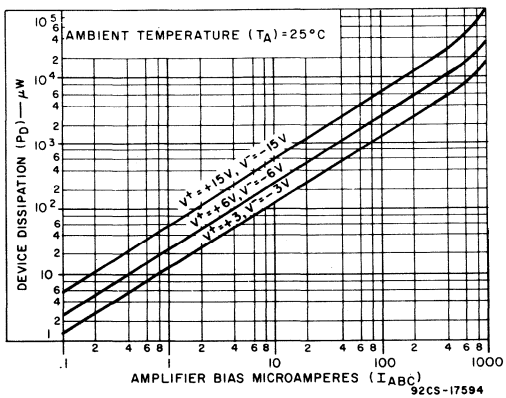


Fig. 9 – Total power dissipation vs. amplifier bias current.

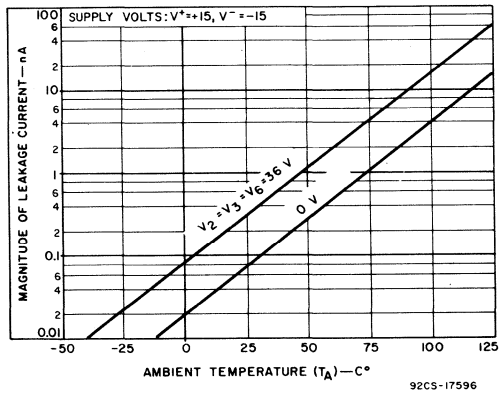


Fig. 10 – Leakage current vs. temperature.

Typical Characteristics Curves for CA3080 and CA3080A – Cont'd.

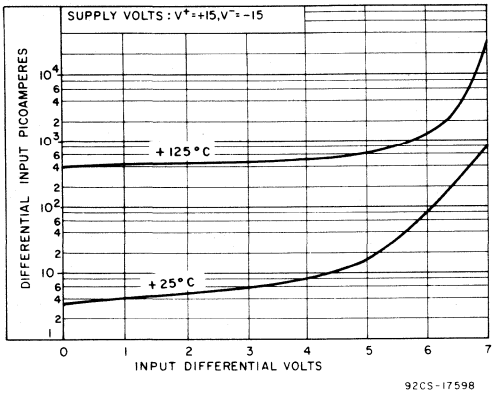


Fig. 11 – Input current vs. input differential voltage.

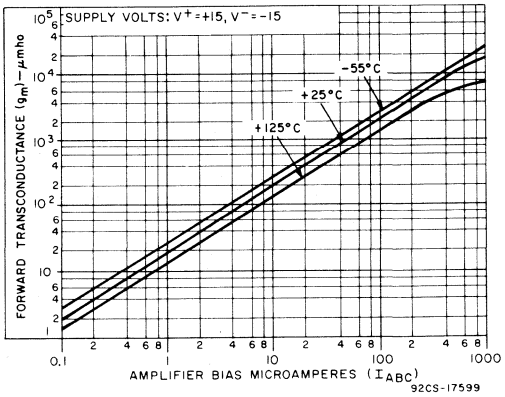


Fig. 12 – Transconductance vs. amplifier bias current.

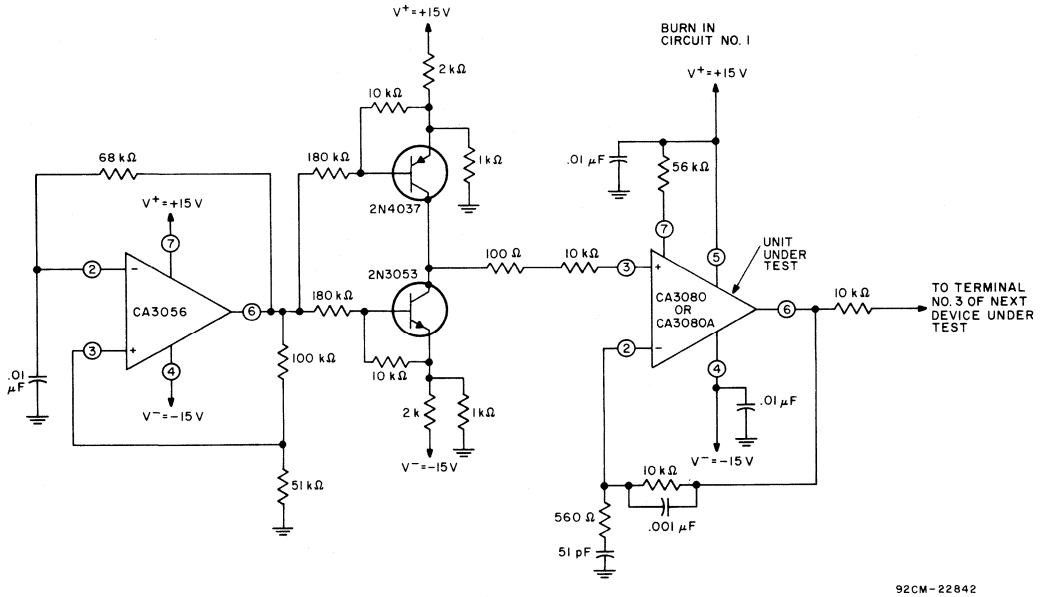


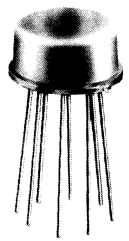
Fig. 13 – Burn-in and operating life test circuit.

RCA
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CA3085/..., CA3085A/..., CA3085B/...



H 1528

8-Lead TO-5 Style Package

High-Reliability

Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V
at Currents up to 100mA
For Application in Aerospace, Military and Critical Industrial Equipment

Features

- **Up to 100 mA output current**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.025%**
- **Pin compatible with LM100 Series**
- **Adjustable output voltage**

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

RCA-CA3085, CA3085A, and CA3085B "Slash" (/) Series types are high-reliability linear integrated circuits designed specifically for voltage service as voltage regulators at output voltages ranging from 17 to 46 volts at currents up to 100 milliamperes. They are intended for applications in aerospace, military, and industrial equipment. They are electrically and mechanically identical with the standard types CA3085, CA3085A and CA3085B described in Data Bulletin File No. 491 but are specially processed and tested to meet the electrical, mechanical and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The package types CA3085, CA3085A, and CA3085B can be supplied to six screening levels – /1N, /1R, /1, /2, /3, and /4 – which correspond to MIL-STD-883 Classes A, B, and C. The chip version can be supplied to three screening levels – /N, /R, and standard chip. These screening levels and detailed information on tests methods,procedures and test sequence are given in Reliability Report RIC-202 "High-Reliability CA3000 Slash (/) Series Types Screened to MIL-STD-883", and in High-Reliability Devices DATABOOK SSD-207.

A list of the available Screening Level Options and a Description of the High-Reliability Type Part Number are given on the following page.

The CA3085, CA3085A, and CA3085B Slash (/) Series type are supplied in the 8-lead TO-5 style package ("T" suffix) in the 8-lead TO-5 style package with dual-in-line formed leads, DIL-CAN, ("S" suffix), or in chip form ("H" suffix).

Applications

- **Shunt voltage regulator**
- **Current regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Combination positive and negative voltage regulator**
- **Dual tracking regulator**

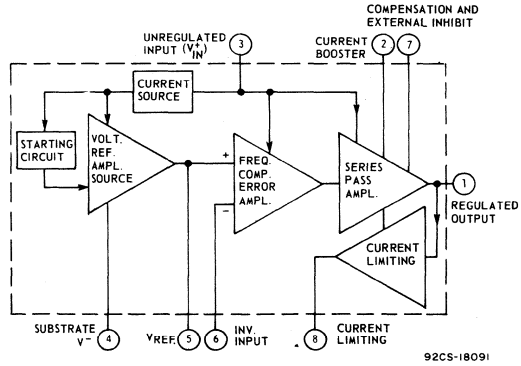


Fig.1–Block diagram of CA3085 Series. For schematic diagram see Fig.2.

Table 1 – Available Screening Level Options (Indicated by Check (√) Mark

PART NUMBER	SCREENING LEVEL		PACKAGE 8-LEAD TO-5 STYLE: WITH STRAIGHT LEADS (T) SUFFIX	PACKAGE 8-LEAD TO-5 STYLE: WITH DUAL-IN-LINE FORMED LEADS DIL-CAN (S) SUFFIX
PACKAGED DEVICE				
CA3085, CA3085A, CA3085B	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883 Classes A, B, &C	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
CHIP			*(H) Suffix*	
CA3085, CA3085A, CA3085B	Custom	/N		√
		/R		√
	Standard Chip			√

Table 2 – Description of RCA Linear IC High-Reliability Part Numbers

Chip Version, CA3085B H/N

CA3085B / H / N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	H= Chip Version	/N, /R — For Description, See RIC-202 and DATABOOK SSD-207

Packaged Device, CA3085B T/IN

CA3085B / T / 1N

Part Number (Type Designation)	PACKAGE SUFFIX LETTER	SCREENING LEVEL
	T = TO-5 Style with Straight Leads	/1N, /1R, /1, /2, /3, /4 — For Description, See RIC-202 and DATABOOK SSD-207
	S = TO-5 Style with with Dual-In-Line Formed Leads (DILCAN)	

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

Power Dissipation:

Without Heat Sink:
- up to T_A = 55°C . . . . . 630 mW
- above T_A = 55°C derate linearly @6.67 mW/°C

With Heat Sink:
- up to T_C = 55°C . . . . 1.6 W
- above T_C = 55°C. . . . derate linearly at 16.7 mW/°C

Unregulated Input Voltage:
- CA3085 . . . . . 30 V
- CA3085A. . . . . 40 V
- CA3085B . . . . . 50 V

TEMPERATURE RANGE
- Operating . . . . . −55 to +125°C
- Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max. . . . .265°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	*	*	*	*	*	+10 0
6	–	–	*	*	*	*	*	*
7	–	–	–	+3 −10	+3 −10	*	*	+‡ 0
8	–	–	–	–	+5 −1	*	*	*
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$ [Unless indicated otherwise]	Typ. Char. Curve Fig. No.	LIMITS CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNITS
Reference Voltage	V_{REF}	V^+_{IN} = 15V	–	1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	V^+_{IN} = 30V	3	–	3.3	4.5	—	–	–	–	–	–	mA
		V^+_{IN} = 40V	–	–	–	–	–	3.65	5	–	–	–	
		V^+_{IN} = 50V	–	–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–	7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	V^+_{IN} = 30, 40, 50V#; R_L = 365 Ω; Term. No. 6 to Gnd.	–	26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	V^+_{IN} = 30V	–	–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–	4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	V^+_{IN} = 16V, V^+_{OUT} = 10V R_{SCP}* = 6 Ω	4	–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	I_L = 1 to 100mA, R_{SCP} = 0	6	–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		I_L = 1 to 100mA, R_{SCP} = 0 T_A = 0°C to +70°C	–	–	–	–	–	0.035	0.6	–	0.035	0.6	
		I_L = 1 to 12mA, R_{SCP} = 0	–	–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	I_L = 1 mA, R_{SCP} = 0	7	–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		I_L = 1mA, R_{SCP} = 0 T_A = 0°C to +70°C	–	–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage	V_{NOISE}	V^+_{IN} = 25V, C_{REF} = 0	–	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
		C_{REF} = 0.22μF		–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	V^+_{IN} = 25V, C_{REF} = 0	–	–	50	–	–	50	–	45	50	–	dB
		f = 1kHz, C_{REF} = 2μF		–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	V^+_{IN} = 25V, f = 1kHz		–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	ΔV_{REF}, ΔV_o	I_L = 0, V_{REF} = 1.6V	10	–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	V^+_{IN} = 25V, +50mA Step	–	–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}	V^+_{IN} = 25V, −50mA Step	–	–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	V^+_{IN} = 25V, f = 1kHz, 2V Step	–	–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}		–	–	0.4	–	–	0.4	–	–	0.4	–	μs

30 (CA3085), 40V(CA3085A), 50V(CA3085B)

• R_{SCP}: Short-circuit protection resistance

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{[V_{OUT(initial)}]\ (\Delta V_{IN})} \times 100\%$

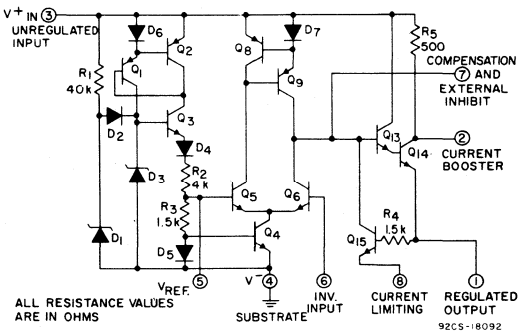


Fig.2—Schematic diagram of CA3085 Series.

*Table 3 – Pre Burn-In and Post Burn-In Electrical Tests and Delta Limits**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $T_A = 25°C$	LIMITS			UNITS
			MIN.	MAX.	MAX. Δ	
Reference Voltage	V_{REF}		1.4	1.8	±0.05	V
Output Voltage Minimum Value	$V_{O(min)}$	V^+_{IN} = 7.5 V or 30 V	–	1.8	±0.1	V
Output Voltage Maximum Value	$V_{O(max)}$	V^+_{IN} = 30 V	26	–	±0.5	V
Limiting Current	I_{LIM}	V^+_{IN} = 7.5 V, R_{SCP} = 7Ω, R_L = 10Ω	–	115	±10	mA
Output Drift Voltage			16	22	±0.5	V

*Levels /1N, /1R, /1, and /2 require pre and post burn-in electrical tests and delta limits
Level /3 requires pre burn-in electrical test only. The burn-in circuit is shown in Fig. 12.

Table 4 – Final Electrical Tests and Group A Electrical Sampling Inspection

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS
			MINIMUM			MAXIMUM			
			–55	+25	+125	–55	+25	+125	
Reference Voltage	V_{REF}		1.4	1.4	1.3	1.9	1.8	1.8	V
Output Voltage Minimum Value	$V_{O(min)}$	V^+_{IN} = 7.5 V, or 30 V	1.9	1.7	1.7	–	–	–	V
Maximum Value	$V_{O(max)}$	V^+_{IN} = 30 V, CA3085	25	26	26	–	–	–	
		V^+_{IN} = 40 V, CA3085A	35	36	36	–	–	–	V
		V^+_{IN} = 50 V, CA3085B	45	46	46	–	–	–	
Load Regulation		I_L = 1 to 100 mA, R_{SCP} = 0, CA3085A	–	–	–	0.75	0.15	0.75	$\%/V_{OUT}$
		I_L = 1 to 100 mA, R_{SCP} = 0, CA3085B	–	–	–	0.75	0.15	0.75	$\%/V_{OUT}$
		I_L = 1 to 12 mA, CA3085	–	–	–	0.15	0.10	|0.15|	$\%/V_{OUT}$
Line Regulation		I_L = 1 mA, R_{SCP} = 0, CA3085	–	–	–	0.2	0.1	0.2	%/V
		I_L = 1 mA, R_{SCP} = 0, CA3085A	–	–	–	0.15	0.075	0.15	%/V
		I_L = 1 mA, R_{SCP} = 0, CA3085B	–	–	–	0.12	0.04	0.12	%/V

Table 5 – Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Reference Voltage	V_{REF}		1.4	1.8	V
Minimum Output Voltage	$V_{O(min)}$	V^+_{IN} = 30 V, CA3085	–	1.9	V
		V^+_{IN} = 40 V, CA3085A	–	1.9	V
		V^+_{IN} = 50 V, CA3085B	–	2.0	V
Load Regulation		I_L = 1 to 100 mA, R_{SCP} = 0, CA3085A	–	0.3	%/V_{OUT}
		I_L = 1 to 12 mA, R_{SCP} = 0, CA3085B	–	0.75	%/V_{OUT}
		I_L = 1 to 12 mA, R_{SCP} = 0, CA3085	–	0.15	%/V_{OUT}
Line Regulation		I_L = 1 mA, R_{SCP} = 0, CA3085	–	0.25	%/V
		I_L = 1 mA, R_{SCP} = 0, CA3085A	–	0.1	%/V
		I_L = 1 mA, R_{SCP} = 0, CA3085B	–	0.05	%/V

TYPICAL CHARACTERISTICS CURVES

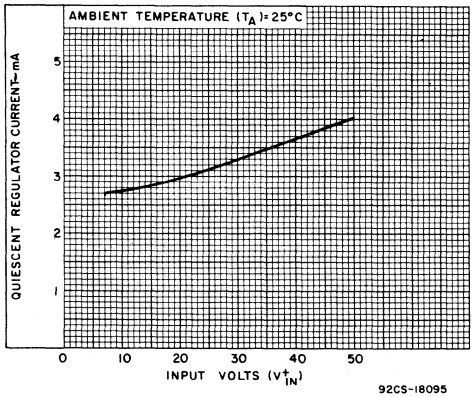


Fig. 3 – $I_{quiescent}$ vs. V^+_{IN}.

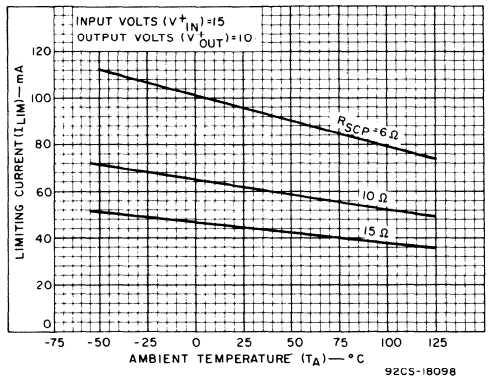


Fig. 4 – I_{LIM} vs. T_A.

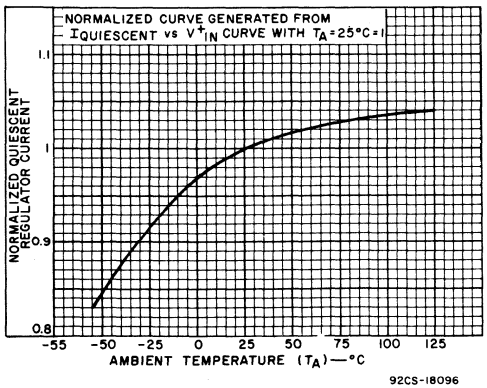


Fig. 5 – Normalized $I_{quiescent}$ vs. T_A.

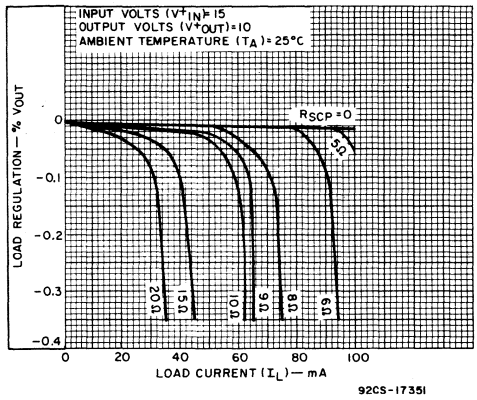


Fig. 6 – Load regulation characteristics.

TYPICAL CHARACTERISTICS CURVES – Cont'd

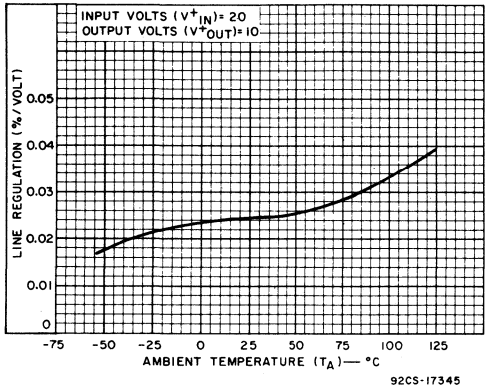


Fig. 7 – Line regulation temperature characteristics.

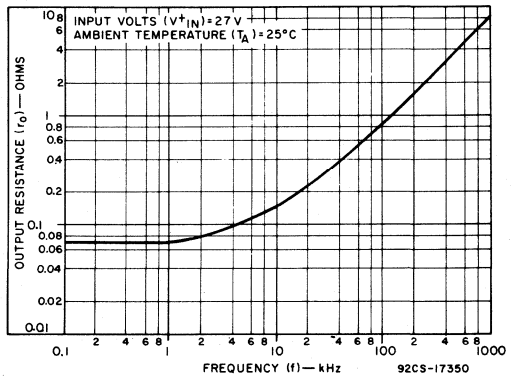


Fig. 8 – r_o vs. f.

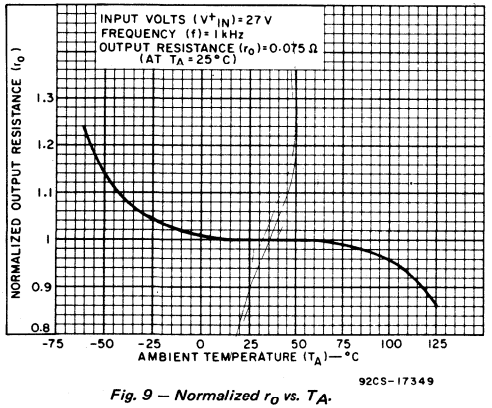


Fig. 9 – Normalized r_o vs. T_A.

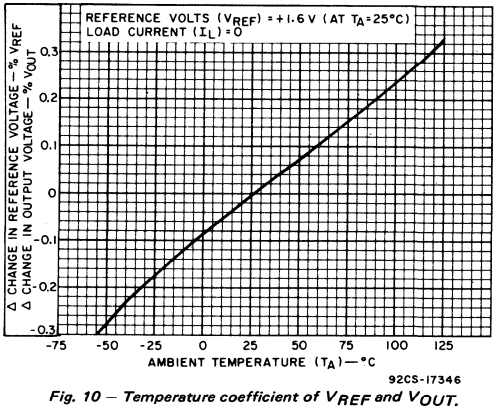


Fig. 10 – Temperature coefficient of V_{REF} and V_{OUT}.

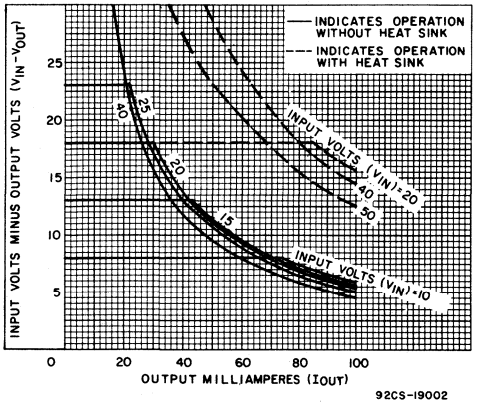


Fig. 11 – Dissipation limitation (V_{IN} – V_{OUT} vs. I_{OUT}).

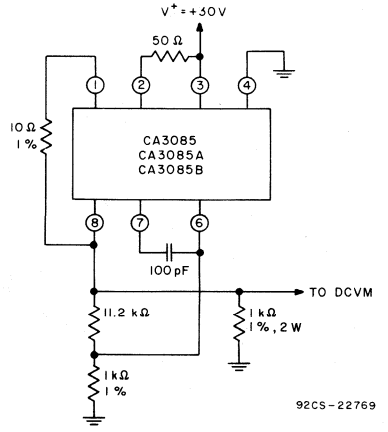


Fig. 12 – Burn-in and operating life test circuit.

For Dimensional Outline, see Appendix

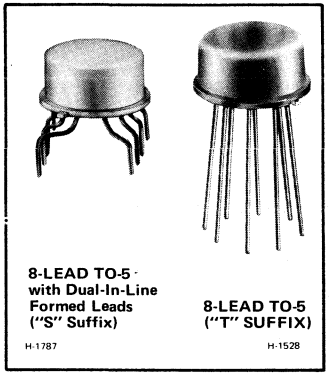
RCA
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

High-Reliability Slash (/) Series

CA3094/... CA3094A/... CA3094B/...



8-LEAD TO-5 with Dual-In-Line Formed Leads ("S" Suffix)
H-1787

8-LEAD TO-5 ("T" SUFFIX)
H-1528

High-Reliability Programmable Power Switch/Amplifiers

For Control & General-Purpose Applications

In Aerospace, Military, and Critical Industrial Equipment

Features:

- **Designed for *single* or dual power supply**
- **Programmable: strobing, gating, squelching, AGC capabilities**
- **Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)**
- **High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)**
- **Total harmonic distortion (THD) @ 0.6 W in class A operation – 1.4% typ.**
- **High current-handling capability – 100 mA (avg.), 300 mA (peak)**
- **Sensitivity controlled by varying bias current**
- **Output: "sink" or "drive" capability**

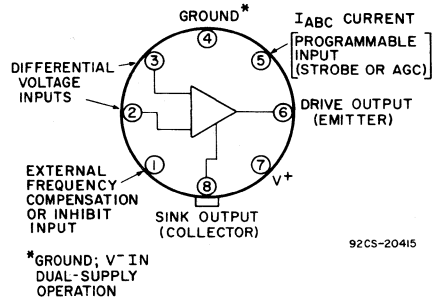
RCA-CA3094, CA3094A, and CA3094B "Slash" (/) Series are high-reliability linear integrated circuit differential-input power-control switch amplifiers with auxiliary circuit features for ease of programmability. They are intended for use in a variety of control and general-purpose applications for aerospace, military and industrial equipment. These devices are electrically and mechanically identical with standard types CA3094, CA3094A and CA3094B described in Data Bulletin File No. 598, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. The CA3094 is intended for operation up to 24 volts. The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

The packaged types in the CA3094, CA3094A, and CA3094B "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883, Classes "A", "B", and "C". The chip versions of the CA3094, CA3094A, and CA3094B can be supplied to three screening levels – /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed in the high-reliability Linear devices, refer to High-Reliability Report RIC-202 "High-Reliability" LINEAR Integrated Circuit CA-3000-Series Types.*

The CA3094, CA3094A, and CA3094B "Slash" (/) Series types are supplied in the 8-lead TO-5 style ceramic package ("T" Suffix), in 8-lead TO-5 style ceramic package with dual-in-line formed leads – ("S" Suffix DIL-CAN) – or in chip form ("H" Suffix).

Applications:

- **Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor**
- **Over-current, over-voltage, over-temperature protectors**
- **Dual-tracking power supply with RCA-CA3085**
- **Wide-frequency-range oscillator ■ Analog timer**
- **Level detector ■ Alarm systems ■ Voltage follower**
- **Ramp-voltage generator ■ High-power comparator**
- **Ground-fault interrupter (GFI) circuits**



Terminal Connections (Bottom View, Terminal End)

For a listing of the Screening Level Options available for the packaged devices and the chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see below.

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package TO-5 Style	
			With Straight Leads (T) Suffix	With Dual-In-Line Formed Leads (S) Suffix
Packaged Device				
CA3094	Custom	/1N	√	√
		/1R	√	√
CA3094A	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
CA3094B		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CA3094	Custom	/N	√	
CA3094A		/R	√	
CA3094B	Standard Chip		√	

Table II — Description of RCA Linear IC High-Reliability Part Numbers

Packaged Device, CA3094AT/IN

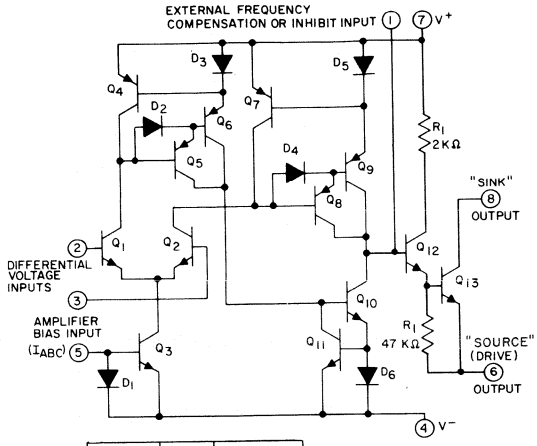
CA3094A T /1N

Part Number (Type Designation)	Package Suffix Letter	Screening Level
	T = TO-5 Style with Straight Leads S = TO-5 Style With Dual-In-Line Formed Leads	/IN, /IR, /1, /2, /3, /4 For Description, See RIC-202

Chip Version, CA3094AH/N

CA3094A H /N

Part Number (Type Designation)	Package Suffix Letter	Screening Level
	H = Chip Version	/N, /R For Description, See RIC-202



OUTPUT MODE	OUTPUT TERM.	INPUTS INV.	INPUTS NON-INV.
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig.1 – Schematic diagram of CA3094, CA3094A, and CA3094B Slash (/) Series Types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3094/Series	CA3094A/Series	CA3094B/Series	
DC Supply Voltage:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC Differential Input Voltage (Terminals 2 and 3)	± 5*			V
DC Common-Mode Input Voltage	Pin 4 ≤ Pins 2 & 3 ≤ Pin 7			
Peak Input Signal Current (Terminals 2 and 3)	± 1			mA
Peak Amplifier Bias Current (Terminal 5)	2			mA
Output Current:				
Peak	300			mA
Average	100			mA
Device Dissipation:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
Thermal Resistance (Junction to Air)	140			°C/W
Ambient Temperature Range:				
Operating	−55 to +125			°C
Storage	−65 to +150			°C
Lead Temperature (During Soldering):				
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

ELECTRICAL CHARACTERISTICS T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS	UNITS
		Test Circuit Fig. No.	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Char. Curves Fig. No.	Typ.	
INPUT PARAMETERS						
Input Offset Voltage	V_{IO}	17		2	0.4 –	mV mV
Input-Offset-Voltage Change	$\lvert\Delta V_{IO}\rvert$		Change in V_{IO} Between I_{ABC} = 100 μA and I_{ABC} = 5 μA		1	mV
Input Offset Current	I_{IO}	18		3	0.02 –	μA μA
Input Bias Current	I_I	19		4	0.2 –	μA μA
Device Dissipation	P_D	18	I_{out} = 0	5, 6	10	mW
Common-Mode Rejection Ratio	CMRR	20			110	dB
Common-Mode Input–Voltage Range	V_{CMR}	20	V^+ = 30 V $\frac{\text{High}}{\text{Low}}$	7	28.8 0.5	V V
			V^+ = 15 V V^- = 15 V	7	+13.8 –14.5	V V
Unity Gain-Bandwidth			I_C = 7.5 mA V_{CE} = 15 V I_{ABC} = 500 μA		30	MHz
Open-Loop Bandwidth At –3 dB Point	BW_{OL}		I_C = 7.5 mA V_{CE} = 15 V I_{ABC} = 500 μA	12	4	kHz
Total Harmonic Distortion (Class A Operation)	THD		P_D = 220 mW P_D = 600 mW		0.4 1.4	%
Amplifier Bias Voltage (Terminal (No.5 to Terminal No.4)	V_{ABC}				0.68	V
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$				4	μV/°C
Power-Supply Rejection	$\Delta V_{IO}/\Delta V$	17			15	μV/V
1/F Noise Voltage	E_N	21	f = 10 Hz I_{ABC} = 50 μA	8	18	nV/√Hz
1/F Noise Current	I_N	21	f = 10 Hz I_{ABC} = 50 μA	9	1.8	pA/√Hz
Differential Input Resistance	R_I		I_{ABC} = 20 μA		1	MΩ
Differential Input Capacitance	C_I		f = 1 MHz V^+ = 30 V		2.6	pF

ELECTRICAL CHARACTERISTICS T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS	UNITS
		Test Circuit Fig. No.	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Char. Curves Fig. No.	Typ.	
OUTPUT PARAMETERS (Differential Input Voltage = 1V)						
Peak Output Voltage: (Terminal No. 6) With Q13 "ON" With Q13 "OFF"	$+V_{OM}$ $-V_{OM}$		V^+ = 30 V R_L = 2 kΩ to ground		27 0.01	V V
Peak Output Voltage: (Terminal No. 6) Positive Negative	$+V_{OM}$ $-V_{OM}$		V^+ = +15 V, V^- = -15 V R_L = 2 kΩ to −15 V		+12 −14.99	V V
Peak Output Voltage: (Terminal No. 8) With Q13 "ON" With Q13 "OFF"	$+V_{OM}$ $-V_{OM}$		V^+ = 30 V R_L = 2 kΩ to 30 V		29.99 0.040	V V
Peak Output Voltage: (Terminal No. 8) Positive Negative	$+V_{OM}$ $-V_{OM}$		V^+ = 15 V, V^- = − 15 V R_L = 2 kΩ to + 15 V		+14.99 14.96	V V
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$		V^+ = 30 V I_C = 50 mA Terminal No.6 grounded	10	0.17	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)			V^+ = 30 V		2	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13})	h_{fe}		V^+ = 30 V V_{CE} = 5 V I_C = 50 mA	11	100,000	
Output Capacitance: Terminal No. 6 Terminal No. 8	C_O		f = 1 MHz All Remaining Terminals Tied to Terminal No. 4		5.5 17	pF pF
TRANSFER PARAMETERS						
Voltage Gain	A	22	V^+ = 30 V I_{ABC} = 100 μA ΔV_{out} = 20 V R_L = 2 kΩ	12	100,000 100	V/V dB
Forward Transconductance To Terminal No. 1	g_m			13	2200	μmhos
Slew Rate: Open Loop: Positive Slope Negative Slope	SR	23	I_{ABC} = 500 μA R_L = 2 kΩ	14	500 50	V/μs V/μs
Unity Gain (Non-Inverting, Compensated)		24	I_{ABC} = 500 μA R_L = 2 kΩ	15	0.7	V/μs

Table III – Pre Burn-In Electrical and Post Burn-In Electrical Tests, and Delta Limits*

Characteristic	Symbol	Test Conditions $V^+ = 30$ V, $I_{ABC} = 100\ \mu A$ $T_A = 25^oC$	Limits Min	Limits Max	Limits Max$^\triangle$	Units
Input Offset Voltage	V_{IO}		–	0.6	±0.2	V
Input Offset Current	I_{IO}		–	0.22	±0.02	μA
Input Bias Current	I_I		0.04	1.1	±0.1	μA
Forward Transconductance To Terminal No.1	g_m		1850	4000	±660	μmho
Collector-to-Emitter Saturation Voltage (Terminal No.8)	$V_{CE(sat)}$	$I_C = 50$ mA Terminal No.6 grounded	0.05	1.0	±0.02	V

* Levels /IN, /IR, /1, and /2 require pre and post burn-in electrical tests and delta limits. Level /3 requires pre-burn in electrical test only. The burn-in circuit is shown in Fig.26.

Table IV – Final Electrical Tests

Characteristic	Symbol	Test Conditions $V^+ = 30$ V, $I_{ABC} = 100\ \mu A$ Unless Otherwise Specified	Limits For Indicated Temperatures (°C) Minimum –55	Minimum +25	Minimum +125	Maximum –55	Maximum +25	Maximum +125	Units
Input Offset Voltage	V_{IO}		–	–	–	0.6	0.5	0.6	V
Input Offset Current	I_{IO}		–	–	–	0.85	0.2	0.22	μA
Input Bias Current	I_I		–	–	–	3.2	0.5	1.1	μA
Forward Transconductance To Terminal No. 1	g_m		910	1650	1850	2100	2750	4000	μmho
Input Offset Voltage Change	$\lvert\triangle V_{IO}\rvert$	Change in V_{IO} between $I_{ABC} = 100\ \mu A$ and $I_{ABC} = 5\ \mu A$	–	–	–	–	8	–	mV
		Change in V_{IO} between $I_{ABC} = 100\ \mu A$ and $I_{ABC} = 15\ \mu A$	–	–	–	3.2	–	3.2	mV
Peak Output Voltage (Terminal No.6) with Q_{13} "ON"	V^+_{OM}	$R_L = 2\ k\Omega$ to ground	26	26	26	–	–	–	V
Common Mode Rejection Ratio	CMRR		70	70	70	–	–	–	dB
Supply Current	I^+_{Supply}		–	–	–	400	400	400	μA
Power Supply Rejection	$\triangle V_{IO}/\triangle V$		–	–	–	150	150	150	μV/V
Power Dissipation	P_D	$I_{OM} = 0$	–	8	–	–	12	–	mW
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$	$I_C = 50$ mA Terminal No.6 Grounded	0.05	0.05	0.05	0.8	0.8	1.0	V

Table V – Group A Electrical Sampling Inspection

Characteristic	Symbol	Test Conditions V^+ = 30 V, I_{ABC} = 100 μA Unless Otherwise Specified	Limits For Indicated Temperatures (°C) Minimum –55	Minimum +25	Minimum +125	Maximum –55	Maximum +25	Maximum +125	Units
Input Offset Voltage	V_{IO}		–	–	–	0.6	0.5	0.6	V
Input Offset Current	I_{IO}		–	–	–	0.85	0.2	0.22	μA
Input Bias Current	I_I		–	–	–	3.2	0.5	1.1	μA
Forward Transconductance To Terminal No. 1	g_m		910	1650	1850	2100	2750	4000	μmho
Input Offset Voltage Change	$\lvert\triangle V_{IO}\rvert$	Change in V_{IO} between I_{ABC} = 100 μA and I_{ABC} = 5 μA	–	–	–	–	8	–	mV
		Change in V_{IO} between I_{ABC} = 100 μA and I_{ABC} = 15 μA	–	–	–	3.2	–	3.2	mV
Peak Output Voltage (Terminal No.6) with Q_{13} "ON"	V^+_{OM}	R_L = 2 kΩ to ground	26	26	26	–	–	–	V
Common Mode Rejection Ratio	CMRR		70	70	70	–	–	–	dB
Supply Current	I^+_{Supply}		–	–	–	400	400	400	μA
Power Supply Rejection	$\triangle V_{IO}/\triangle V$		–	–	–	150	150	150	μV/V
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$	I_C = 50 mA Terminal No.6 Grounded	0.05	0.05	0.05	0.8	0.8	1.0	V
Output Leakage Current Q_{13} "OFF"	$-I_{OL}$	V^+ = 25 V	–10	–10	–10	0.1	0.1	0.1	μA
Max. Output Current Q_{13} "ON"	$-I_{OM}$	I_{ABC} = 15 μA	–140	–140	–140	–98	–98	–98	mA

Table VI – Group C Electrical Characteristics Sampling Tests (T_A = 25°C)

Characteristic	Symbol	TEST CONDITIONS V^+ = 30 V, I_{ABC} = 100 μA Unless Otherwise Specified	LIMITS Min	LIMITS Max	Units
Input Offset Voltage	V_{IO}		–	0.6	V
Input Offset Current	I_{IO}		–	0.25	μA
Forward Transconductance to Terminal No. 1	g_m		1420	3350	μmho
Peak Output Voltage (Terminal No.6) with Q_{13} "ON"	$+V_{OM}$	R_L = 2 kΩ to ground	25	–	V
Supply Current	I^+_{Supply}		–	400	μA
Output Leakage Current Q_{13} "OFF"	$-I_{OL}$	V^+ = 25 V	–15	–	μA
Max. Output Current Q_{13} "ON"	$-I_{OM}$	I_{ABC} = 3 μA	–	–45	mA

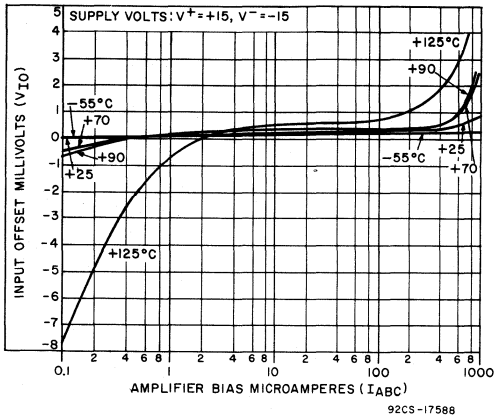


Fig.2 – Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

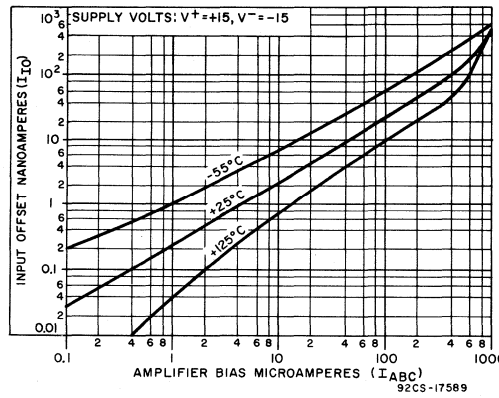


Fig.3 – Input offset current vs. amplifier bias current (I_{ABC}, terminal No.5).

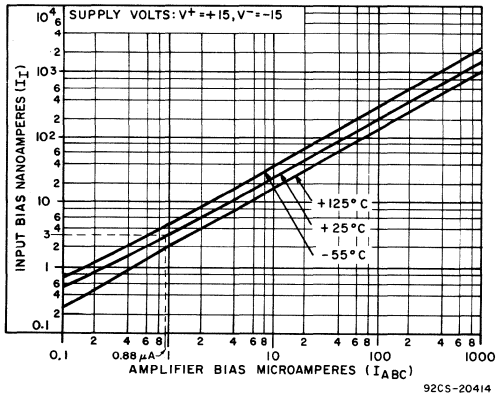


Fig.4 – Input bias current vs. amplifier bias current (I_{ABC}, terminal No.5).

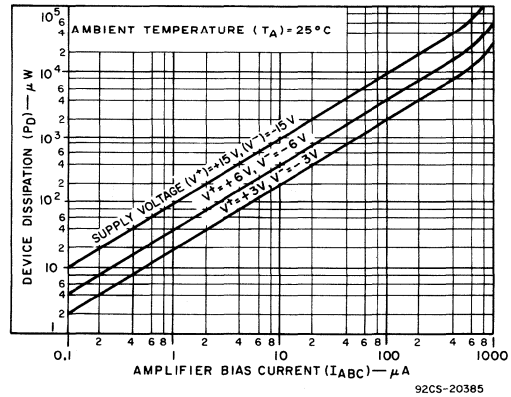


Fig.5 – Device dissipation vs. amplifier bias current (I_{ABC}, terminal No.5).

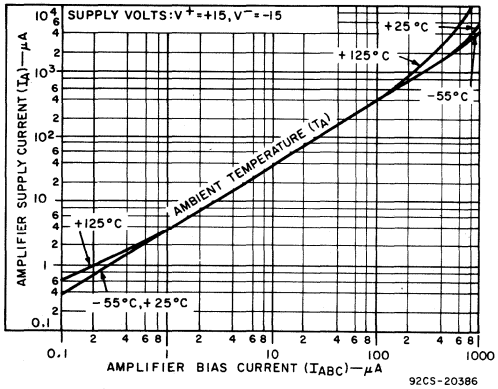


Fig.6 – Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No.5).

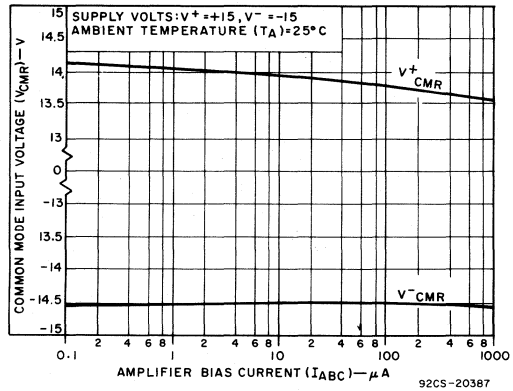


Fig.7 – Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

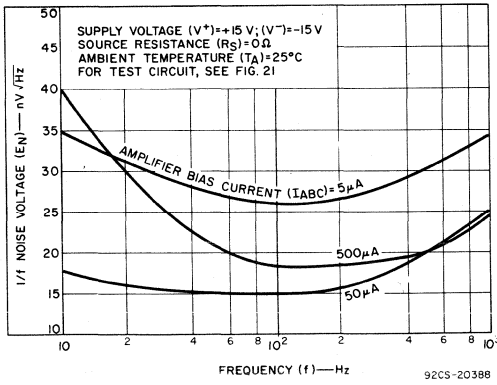


Fig.8 – 1/f Noise voltage vs. frequency.

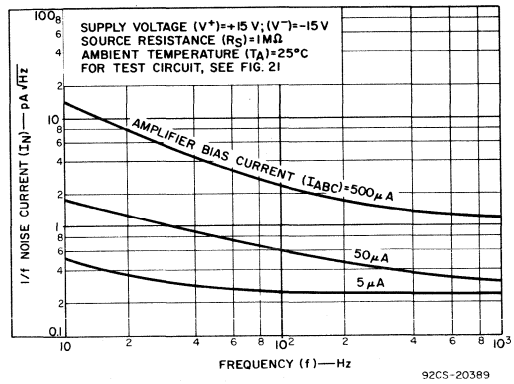


Fig.9 – 1/f Noise current vs. frequency.

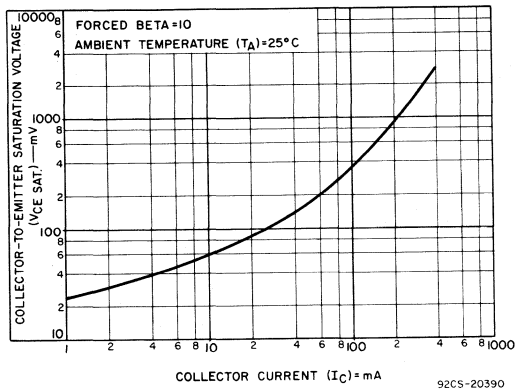


Fig.10 – Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.

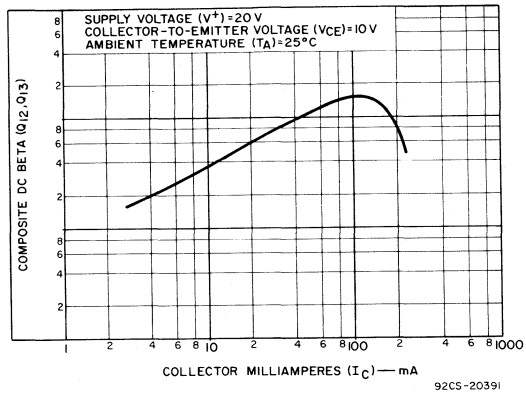


Fig.11 – Composite dc beta vs. collector current of Darlington-connected output transistors Q_{12}, Q_{13}.

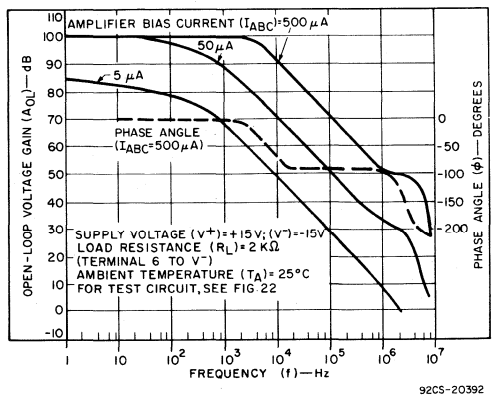


Fig.12 – Open-loop voltage gain vs. frequency.

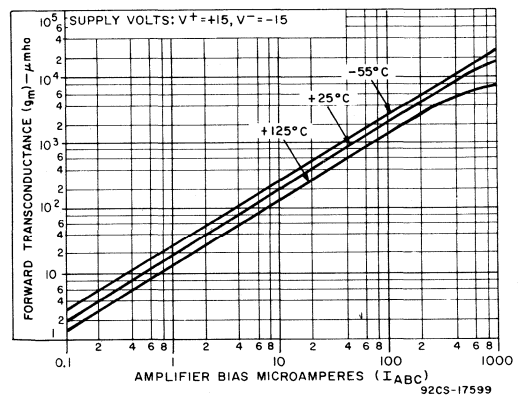


Fig.13 – Forward transconductance vs. amplifier bias current.

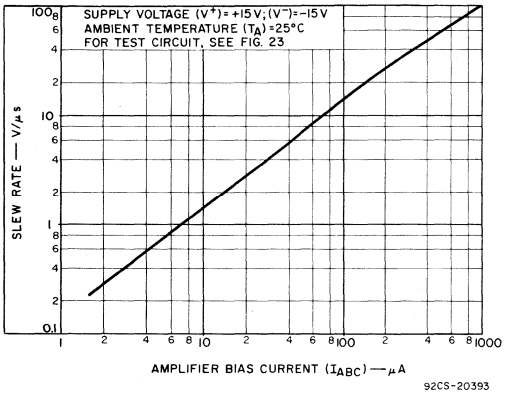


Fig. 14 – Slew rate vs. amplifier bias current.

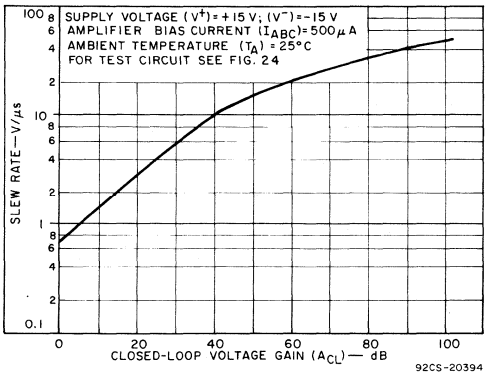


Fig. 15 – Slew rate vs. closed-loop voltage gain.

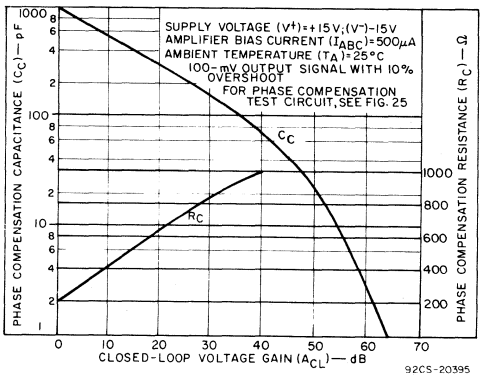


Fig. 16 – Phase compensation capacitance and resistance vs. closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No. 8) and the "Drive" Output (terminal No. 6) of the CA3094T are not inherently current (or power) limited. Therefore, if a load is connected between terminal No. 6 and terminal No. 4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No. 7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No. 8 and terminal No. 7, the current-limiting resistor should be connected between terminal 6 and terminal No. 4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No. 7 and the V^+ supply.

TEST CIRCUITS

1/f Noise Measurement Circuit

When using the CA3094T, AT, or BT audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig. 21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No. 2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for ^{E} noise and ^{I} noise measurements, respectively. These measurements are made at frequencies of 10 Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 μA I_{ABC} are $E_n = 18\ nV/\sqrt{Hz}$ and $I_N = 1.8\ pA/\sqrt{Hz}$.

Test Circuits

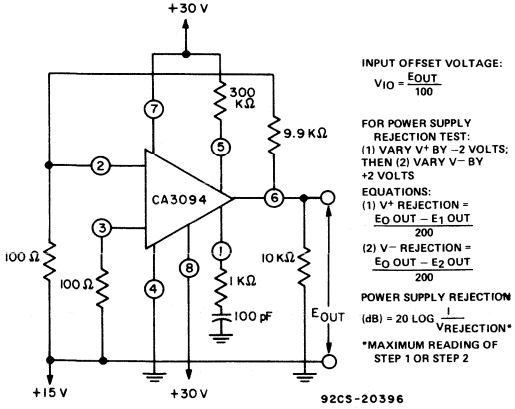


Fig. 17—Input offset voltage and power-supply rejection test circuit.

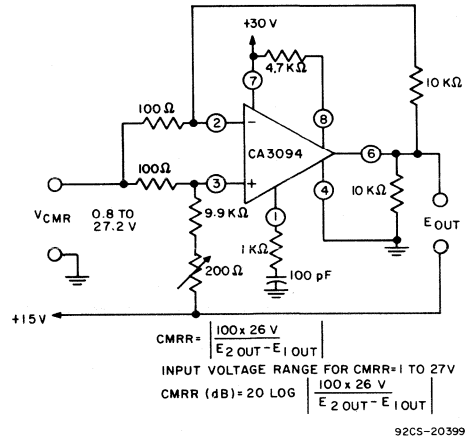


Fig. 20—Common-mode range and rejection ratio test circuit.

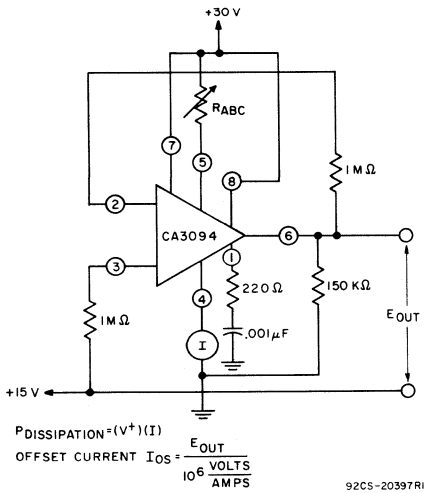


Fig. 18—Input offset current test circuit.

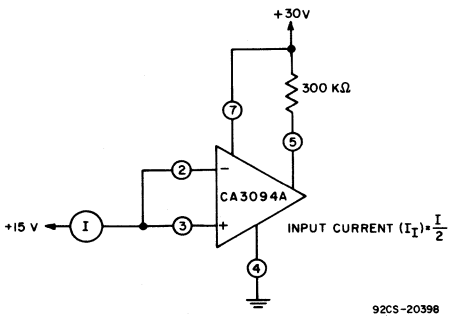
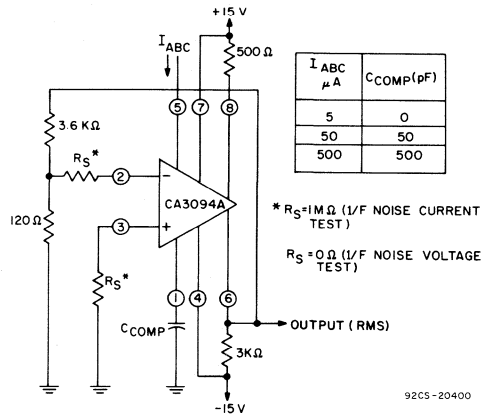
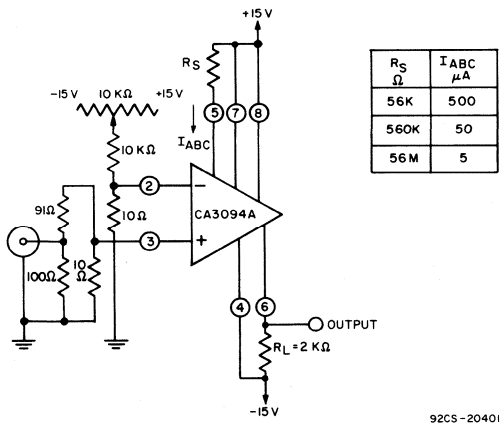


Fig. 19—Input bias current test circuit.



IABC μA	CCOMP(pF)
5	0
50	50
500	500

Fig. 21 — 1/f noise test circuit.



RS Ω	IABC μA
56K	500
560K	50
56M	5

Fig. 22—Open-loop gain vs. frequency test circuit.

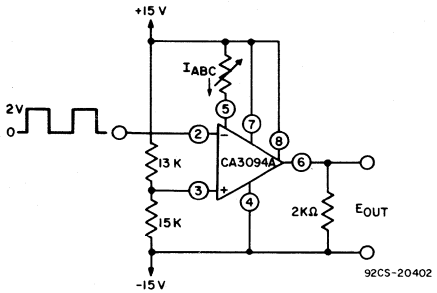


Fig.23—Open-loop slew rate vs. I_{ABC} test circuit.

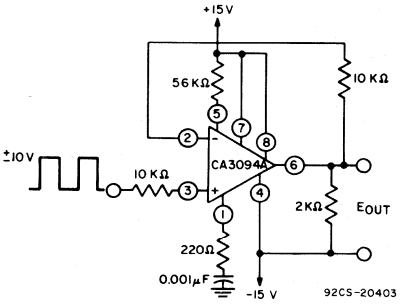
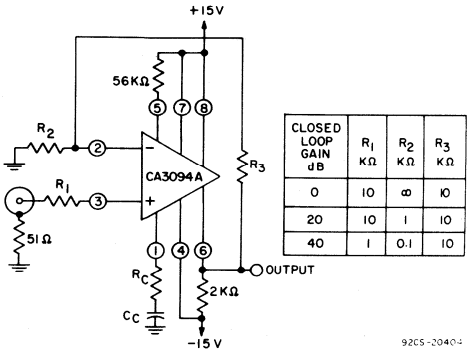


Fig.24—Slew rate vs. non-inverting unity gain test circuit.



CLOSED LOOP GAIN dB	R_1 KΩ	R_2 KΩ	R_3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig.25—Phase compensation test circuit.

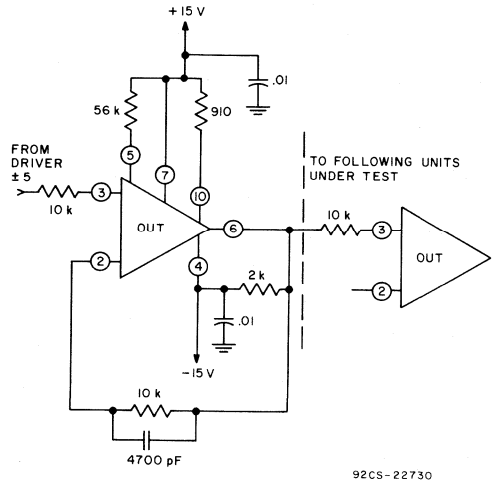
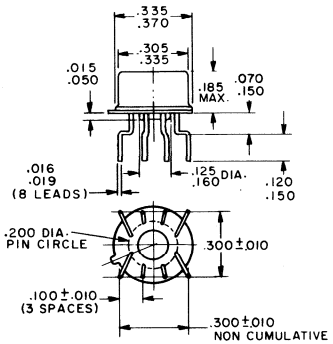


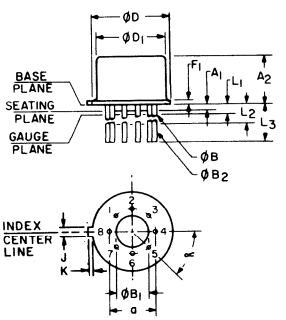
Fig.26 — Burn-in and life-test circuit.

8-LEAD TO-5 WITH DUAL-IN-LINE FORMED LEADS



DIMENSIONAL OUTLINES

8-LEAD TO-5 JEDEC MO-002-AL



SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
a	0.200 TP		2	5.88 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0.125	0.160		3.18	4.06
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

1. Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radium of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2.øB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

Lead Finish

In accordance with MIL-M-38510. Paragraph 3.6.2.5, Lead Finish "A".

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

RCA Solid State Division

Linear Integrated Circuits

High-Reliability CA3000 Slash [/] Series Types

Screened to MIL-STD-883

RCA linear high-reliability slash (/) series integrated circuits are available for applications in aerospace, military, and industrial equipment. These circuits are supplied to six screening levels (/1N, /1R, /1, /2, /3, /4) which meet the electrical, mechanical, and environmental test methods and procedures established for micro-electronic devices in MIL-STD-883. These six screening levels are equivalent to MIL-STD-883 Classes A, B, C and are summarized in Table 1.

This bulletin defines the test procedures employed with linear IC devices to meet the reliability standards required by MIL-STD-883. The level /1N part includes SEM (Scanning Electron Microscope) Inspection to NASA-Goddard Specification GSFC-S-311-P-12 of MIL-M-38510, and Precap Visual Inspection, Condition A, Method 2010-1, MIL-STD-883. The level /R part includes the SEM inspection in addition to the requirements of level /1 part.

The Product Flow Diagram shown in Fig. 1 lists a summary of processing, screening, tests, and sampling procedures followed in the manufacture of linear integrated circuits.

Table 2 gives detailed information for the screening tests included in the Product Flow Diagram. Tables 3 and 4 give test criteria for Final Electrical and Group A Electrical Tests. Tables 5 and 6 describe Group B and C Environmental Sampling Inspection Tests.

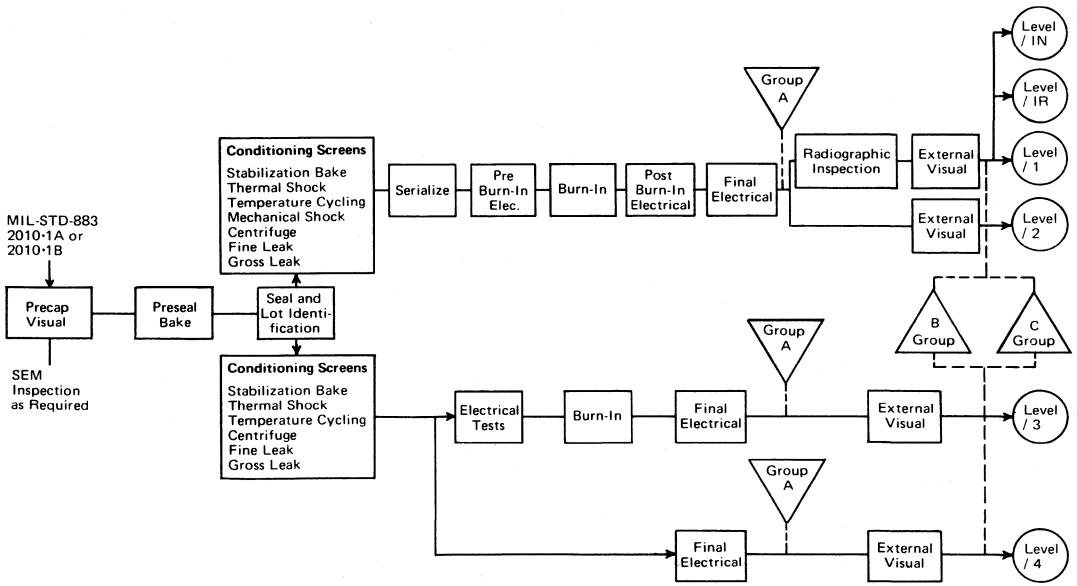


Fig. 1 — Product Flow Diagram (See Tables 2, 3, 4, 5, and 6 for Details)

Table 1 – Description of RCA Integrated-Circuit Screening Levels

Screening Levels		Application	Description
RCA Levels	**Equivalent to MIL-STD-883, Method 5004.1**		
For Packaged Devices			
/1N	Class A with SEM* Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **impossible and reliability is imperative**
/1R	Class A with SEM* Inspection and Condition B Precap Visual Inspection		
/1	Class A with Condition B Precap Visual Inspection		
/2	Class A with Condition B Precap Visual Inspection. Radiographic Inspection Omitted	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **extremely difficult or impossible and reliability is imperative**
/3	Class B	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement **can be performed but are difficult and expensive**
/4	Class C	Military and Industrial. For example, on Ground Based Electronics	For devices intended for use where replacement can readily be accomplished
For Chips			
/N	SEM* Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For hybrid applications where maintenance and replacement **are extremely difficult and reliability is imperative**
/R	SEM* Inspection and Condition B Precap Visual Inspection		
Standard Types	Condition B Precap Visual Inspection	Military and Industrial	For general applications

*SEM – Scanning Electron Microscope Inspection per NASA Specification GSFC-S-311-P-12

Note A: For details on Condition A and Condition B Precap Visual Inspection, refer to MIL-STD-883 Method 2010.1

Note B: Lot acceptance testing for chips is available on a custom basis

Ordering Information

1. **Packaged Device and Chip Type Number Identification**
When ordering a packaged device or a chip, it is important that the desired Screening Level and Package Designation for the Packaged Device, and the desired Screening Level for the Chip Version indicated by the appropriate suffix letters be added to the Part Number as shown below. For example, a CA3094A in an 8-lead TO-5 package and processed to meet MIL-STD-883 Class A requirements with SEM Inspection plus Condition A Precap Visual would be identified as the CA3094AT/1N. In similar manner, a CA3094 Chip having SEM inspection plus Condition A Precap Visual would be identified as the CA3094H/N.

2. **Data Supplied With Order for Packaged Devices**

	For the Following RCA Screening Levels
a) Product Screening Data	
Certificate of Compliance Signed by RCA Representative – Provides lot identity, customer order identity, lists and certifies tests, methods and conditions of required processing per MIL-STD-883	All
Group A Subgroup – Test Summary Attributes Data	All
Variables Data, Pre Burn-In and Post Burn-In	/1N, /1R, /1, /2
Radiographic Inspection Film and Film Inspection Record	/1N, /1R, /1
SEM Inspection Certificate of Compliance to NASA Specification GSFC-S-311-P-12 Includes lot identification and one worst-case photograph	/1N, /1R

b) Lot Quality Conformance Data –
Group B and Group C Subgroups

Attributes Data Summary of the Latest Group B and/or Group C Subgroup can be ordered at a nominal charge.

Special Group B and/or Group C quality conformance tests on samples from the specific lot of parts ordered will be considered on a custom basis only.

Description of RCA Linear IC High-Reliability Part Numbers.

Packaged Device CA3094AT/1N

CA3094A	T	/1N
	Package Suffix Letter	**Screening Level**
Type Designation	T = TO-5 Style Package	/1N /2 /1R /3 /1 /4 For Description, See Table 1

Chip Version, CA3094H/N

CA3094	H	/N
	Package Suffix Letter	**Screening Level**
Type Designation	H = Chip Version	/N /R For Description, See Table 1

Table 2 – Description of Total Lot Screening (X = 100% Testing)

Test	Conditions	MIL-STD-883		RCA Screening Levels					
		Method	Conditions	/1N	/1R	/1	/2	/3	/4
SEM Inspection	NASA Per GSFC-S-311-P-12	–	–	X	X	–	–	–	–
Precap Visual	–	2010.1	A	X	–	–	–	–	–
Precap Visual	–	2010.1	B	–	X	X	X	X	X
Preseal Bake	16 to 32 hrs at 200°C	–	–	X	X	X	X	X	X
Seal & Lot Identification	–	–	–	X	X	X	X	X	X
Stabilization Bake	48 hrs. at 150°C	1008	C	X	X	X	X	X	X
Thermal Shock	15 cycles	1011	C	X	X	X	X	–	–
Temperature Cycling	10 cycles	1010	C	X	X	X	X	X	X
Mechanical Shock	5 pulses, Y_1 direction	2002	B	X	X	X	X	–	–
Centrifuge	Y_2, Y_1 direction	2001	E	X	X	X	X	–	–
	Y_1 direction only	2001	E	–	–	–	–	X	X
Fine Leak	–	1014	A	X	X	X	X	X	X
Gross Leak	–	1014	C	X	X	X	X	X	X
Electrical Tests	See Note 1	–	–	X	X	X	X	X	–
Serialize	–	–	–	X	X	X	X	–	–
Pre Burn-in Electrical	See Note 2	–	–	X	X	X	X	–	–
Burn-in	240 hours	1015	B, D or E	X	X	X	X	–	–
	168 hours	1015	B, D or E	–	–	–	–	X	–
Post Burn-in Electrical	Delta Requirements (See Note 2)	–	–	X	X	X	X	–	–
Final Electrical	–	–	–	–	–	–	–	–	–
a) 25°C	see Table 4	–	–	X	X	X	X	X	X
b) -55 and +125°C	see Table 4	–	–	X	X	X	X	X	S
Radiographic Inspection	1 view	2012	–	X	X	X	–	–	–
External Visual	–	2009	–	X	X	X	X	X	X

Note 1: See specific type Slash (/) Series type data bulletin for test conditions and limits

Note 2: For requirements, see specific Slash (/) Series type data bulletin

Table 3 – Final Electrical Tests

TEMPERATURE (T_A)	TEST	TEST CRITERIA		
		LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
+25°C	Selected Static Parameters	100%	100%	100%
+125°C	Selected Static Parameters	100%	100%	–
-55°C	Selected Static Parameters	100%	100%	–
+25°C	Selected Dynamic Parameters	100%	100%	–

Table 4 – Group A Electrical Sampling Inspection

SUBGROUP	TEST	CONDITION	LTPD		
			LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Selected Static Parameters	T_A = +25°C	5	5	5
2	Selected Static Parameters	T_A = +125°C	5	7	10
3	Selected Static Parameters	T_A = -55°C	5	7	10
4	Selected Dynamic Parameters	T_A = +25°C	5	5	5

Table 5 – Group B Environmental Sampling Inspection (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Physical Dimensions	2003	Test Cond. A per applicable data sheet	10	15	20
2	Marking Permanency	2008	Test Cond. B per Par. 3.2.1	4 devices (no failures)		
	Visual and Mechanical	2008	Test Cond. B 10 X mag.	1 device (no failure)		
	Bond Strength	2011	Test Cond. D 10 Devices minimum	5	15	20
3	Solderability	2003		10	15	15
4	Lead Fatigue	2004	Test Cond. B2 any 5 leads	10	15	15
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			

Note 1: Group B tests limited to a production period not to exceed 6 weeks
Note 2: Operating life circuits are included in specific type high-reliability data bulletins

Table 6 – Group C Environmental Sampling Inspection (Note 3)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Thermal Shock	1011	Test Cond. C	10	15	15
	Temperature Cycling	1010	Test Cond. C			
	Moisture Resistance	1004	No Voltage Applied			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests – Note 4					
2	Mechanical Shock	2002	Test Cond. B, 0.5 ms	10	15	15
	Vibration, Var. Freq.	2007	Test Cond. A			
	Constant Acceleration	2001	Test Cond. E			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests – Note 4					
3	Salt Atmosphere	1009	Test Cond. A Omit Initial Conditioning	10	15	15
4	High Temp. Storage	1008	Test Cond. C	7	7	7
	Critical Post Tests – Note 4		1000 hours			
5	Operating Life	1005	T_A - 125°C, 1000 hrs.	5	5	5
	Critical Post Tests – Note 4		Test Circuit (Note 2)			
6	Steady State Bias	1015	Test Cond. A, 72 hrs.	7	–	–
	Critical Post Tests – Note 4		At T_A = 150°C (Note 4)			

Note 3: Group C tests performed at 3 month intervals
Note 4: Static parameters and limits are shown in specific type high-reliability data bulletins

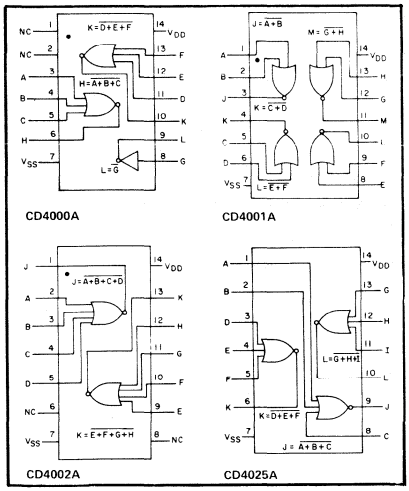
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4000A/..., CD4001A/... CD4002A/..., CD4025A/...



High-Reliability COS/MOS NOR Gates (Positive Logic)

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Dual 3 Input plus Inverter — — — CD4000A/
Quad 2 Input — — — — — — — — CD4001A/
Dual 4 Input — — — — — — — — CD4002A/
Triple 3 Input — — — — — — — — CD4025A/

Special Features:

- **Medium speed operation . . . $t_{PHL} = t_{PLH}$ = 25 ns (typ.) at C_L = 15 pF**
- **Low "high"- and "low" -level output impedance . . .500 Ω and 200 Ω (typ.), respectively, at $V_{DD} - V_{SS}$ = 10 V**
- **Low power — 10 nW typ. for gates**
- **Logic compatibility T^2L and DTL interfacing (see ICAN-6602)**
- **High fanout**
- **Excellent temperature stability — ±1.5% shift in transfer characteristics over −55 to +125°C**
- **Inputs fully protected**

RCA CD4000A, CD4001A, CD4002A, and CD4025A "Slash" (/) Series are high-reliability COS/MOS integrated circuit NOR Gates (Positive Logic). They are intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The combination of these devices and the RCA NAND Positive Logic Gate Series CD4011A, CD4012A, and CD4023A can contribute to appreciable package count savings in many of these logic function configurations. These devices are electrically and mechanically identical with standard COS/MOS types CD4000A, CD4001A, CD4002A, and CD4025A described in data Bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4000A	MIL-M-38510/05201
CD4001A	MIL-M-38510/05202
CD4002A	MIL-M-38510/05203
CD4025A	MIL-M-38510/05204

The packaged types in the CD4000A, CD4001A, CD4002A, and CD4025A "Slash" (/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

COS/MOS high-reliability integrated circuit part numbers, see the chart below.

The CD4000A, CD4001A, CD4002A, and CD4025A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4000AD, CD4000AK, CD4001AD,	Custom	/1N	√	√
		/1R	√	√
CD4001AK, CD4002AD, CD4002AK, CD4025AD, CD4025AK	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4000AH, CD4001AH, CD4002AH,	Custom	/N	√	
		/R	√	
CD4025AH	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N For /1R Descrip- /1 tion, /2 See /3 SSD- /4 207

Chip Version, CD4000AH/N

CD4000A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N For Descrip- /R tion, See SSD-207

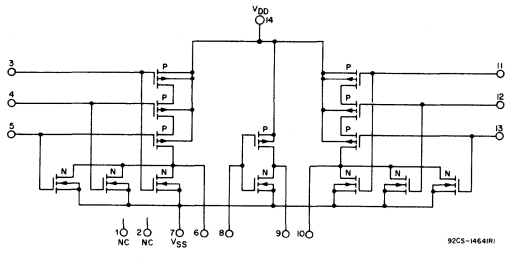


Fig. 1– Schematic diagram for type CD4000A.

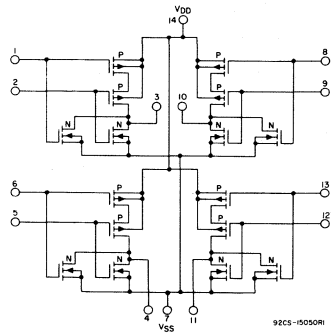


Fig. 2– Schematic diagram for type CD4001A.

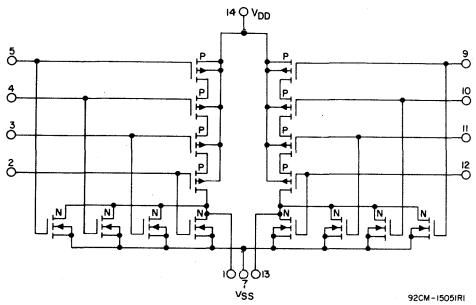


Fig. 3– Schematic diagram for type CD4002A.

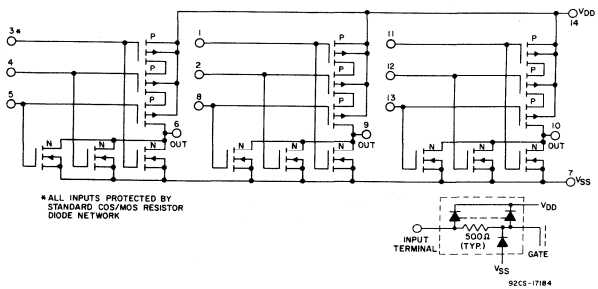


Fig. 4– Schematic diagram for type CD4025A.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
					CD4000AD, CD4001AD, CD4002AD, CD4025AD, CD4000AK, CD4001AK, CD4002AK, CD4025AK											
					−55°C			25°C			125°C					
		V_O Volts	V_{DD} Volts		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I_L			5	–	–	0.05	–	0.001	0.05	–	–	3	μA	–	1
				10	–	–	0.1•	–	0.001	0.1•	–	–	2•			
Quiescent Device Dissipation/Package	P_D			5	–	–	0.25	–	0.005	0.25	–	–	15	μW	–	–
				10	–	–	1	–	0.01	1	–	–	20			
Output Voltage Low-Level	V_{OL}	$V_I=V_{DD}$ $I_O=0$		5	–	–	0.01	–	0	0.01	–	–	0.05	V	5,6	1
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.6•	–	–	0.7•			
High-Level	V_{OH}	$V_I=V_{SS}$ $I_O=0$		5	4.99	–	–	4.99	5	–	4.95	–	–	V	7	1
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.4•	–	–	14.3•	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D=-10\ \mu A$			−0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	–	2
P-Channel	V_{THP}	$I_D=10\ \mu A$			0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity	V_{NL}	$I_O=0$	3.6	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	–	2
			7.2	10	3•	–	–	3•	4.5	–	2.9•	–	–			
For Definition, See Appendix SSD-207	V_{NH}		0.95	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V	–	–
			2.9	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: N-Channel	I_DN	$V_I=V_{DD}$	0	3	0.02•	–	–	0.025•	–	–	–	–	–	mA	8,10	2
			0.4▲	5	0.5	–	–	0.40•	1	–	0.28	–	–			
			0.5	10	1.1	–	–	0.9•	2.5	–	0.65	–	–			
P-Channel	I_DP	$V_I=V_{SS}$	3	3	−0.02•	–	–	−0.025•	–	–	–	–	–	mA	9,11	2
			2.5†	5	−0.62	–	–	−0.5•	−2	–	−0.35	–	–			
			9.5	10	−0.62	–	–	−0.5•	−1	–	−0.35	–	–			
Diode Test	V_{DF}				–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

▲Maximum noise-free saturated Bipolar output voltage.
†Minimum noise-free saturated Bipolar output voltage.

For Noise Immunity Test Circuits, Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations see Appendix.

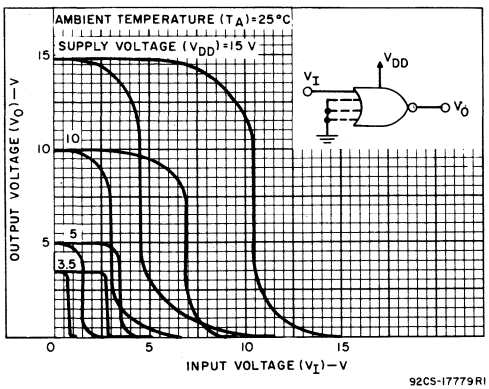


Fig. 5— Min. and max. voltage transfer characteristics.

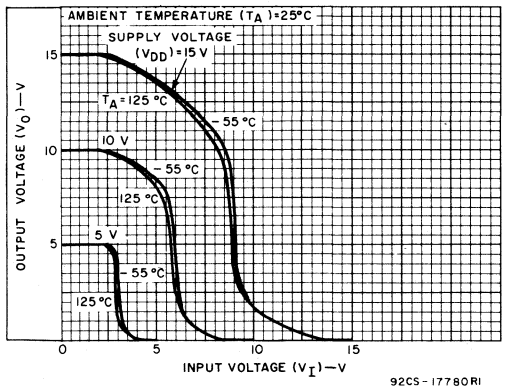


Fig. 6— Typ. voltage transfer characteristics as a function of temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4000AD,CD4000AK CD4001AD,CD4001AK CD4002AD,CD4002AK CD4025AD,CD4025AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		Fig. No.	
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	–	35	50	ns	13	–
			10	–	25	40●			
Low-to-High Level	t_{PLH}		5	–	35	95	ns	13	–
			10	–	25	45●			
Transition Time: High-to-Low Level	t_{THL}		5	–	65	125	ns	14	–
			10	–	35	70●			
Low-to-High Level	t_{TLH}		5	–	65	175	ns	14	–
			10	–	35	75●			
Input Capacitance	C_I	Any Input		–	5	–	pF		1

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing

Note 1: Test is a one input one output only.

DYNAMIC ELECTRICAL CHARACTERISTICS (Driving TTL, DTL) at T_A = 25°C, $V_{DD} - V_{SS}$ = 5 V, C_L = 5 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4000AD,CD4001AD CD4002AD,CD4025AD CD4000AK,CD4001AK CD4002AK,CD4025AK			UNITS	TYPICAL CHARACTERISTICS CURVES
			Driving TTL,DTL	Min.	Typ.	Max.		Fig. No.
Propagation Delay Time: High-to-Low Level	t_{PHL}	R_L = 2 KΩ	Med. Power	–	35	65	ns	15
		R_L =20 KΩ	Low Power	–	35	65		
Low-to-High Level	t_{PLH}	R_L = 2 KΩ	Med. Power	–	15	30	ns	16
		R_L =20 KΩ	Low Power	–	20	40		
Transition Time	t_{THL}	R_L = 2 KΩ	Med. Power	–	40	75	ns	–
	t_{TLH}	R_L =20 KΩ	Low Power	–	40	75		

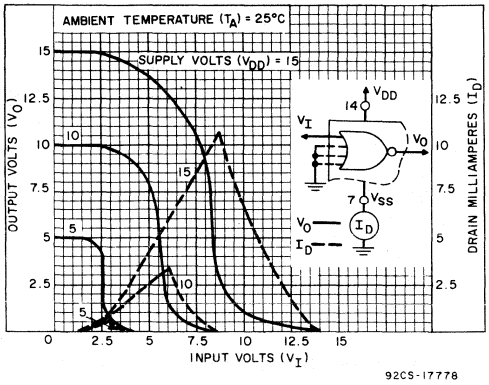


Fig. 7— Typ. current and voltage transfer characteristics.

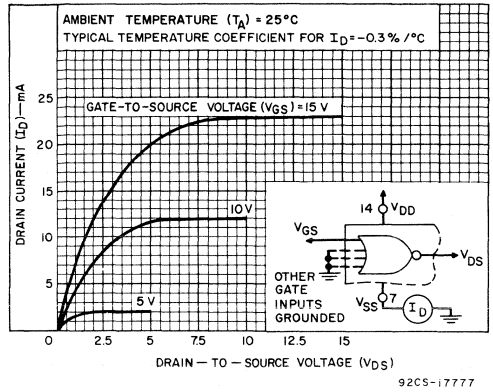


Fig. 8— Typ. n-channel drain characteristics.

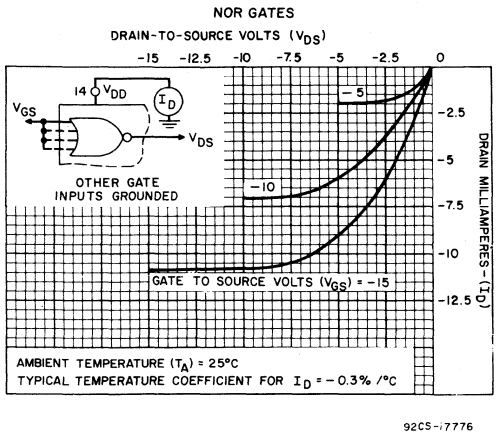


Fig. 9— Typ. p-channel drain characteristics.

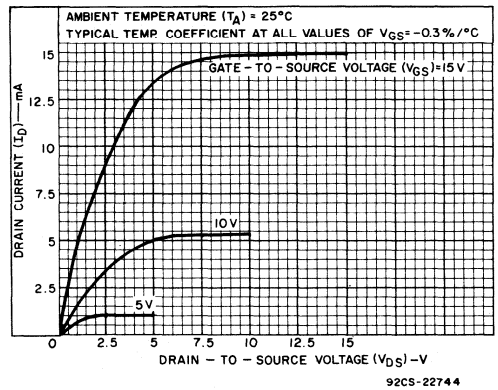


Fig. 10— Min. n-channel drain characteristics.

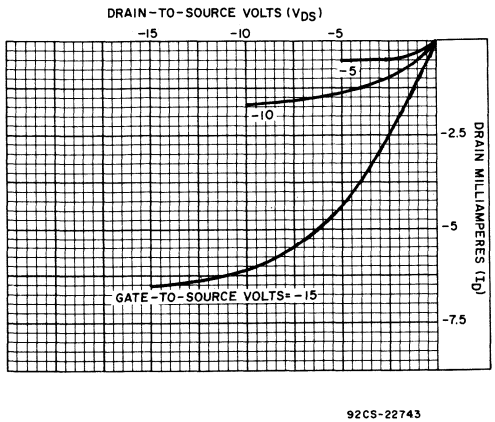


Fig. 11— Min. p-channel drain characteristics.

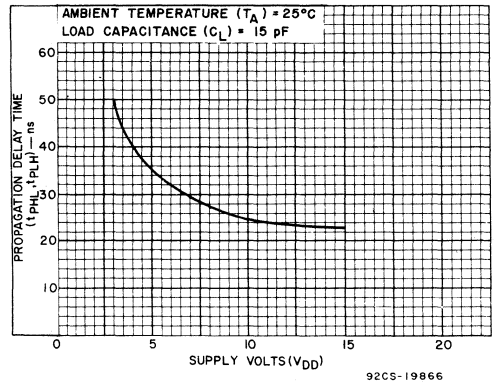


Fig. 12— Typ. propagation delay time vs. V_{DD}.

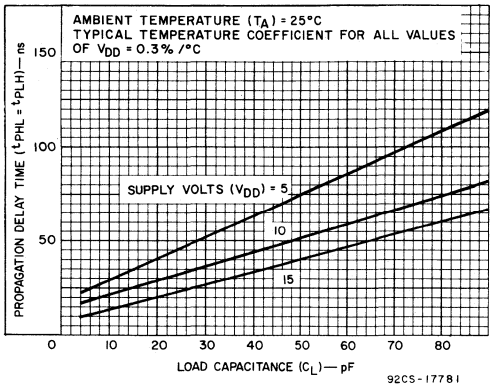


Fig. 13– Typ. propagation delay time vs.C_L.

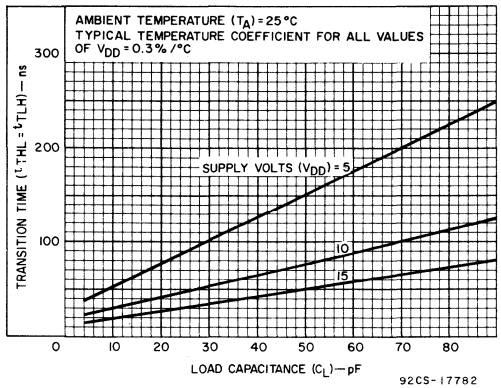


Fig. 14– Typ. transition time vs. C_L.

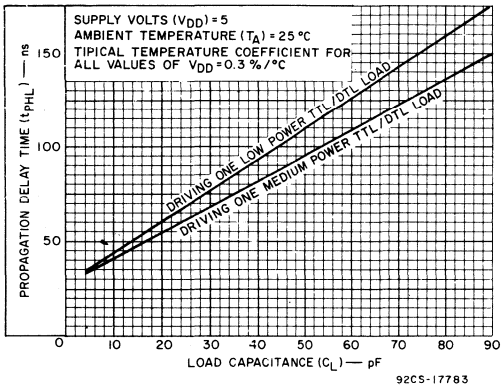


Fig. 15– Typ. low-level propagation delay time vs. C_L – driving TTL and DTL.

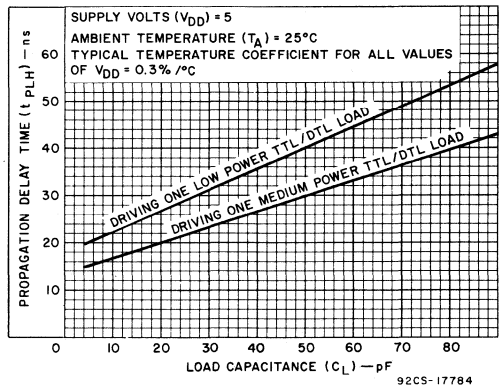


Fig. 16– Typ. high-level propagation delay time vs. C_L – driving TTL and DTL.

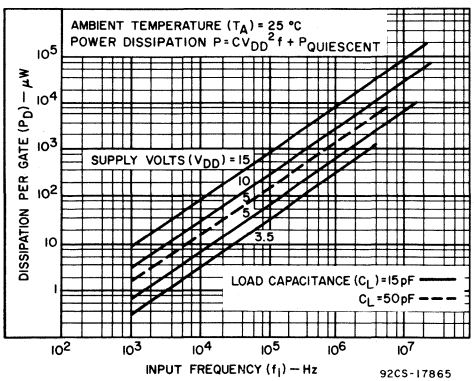
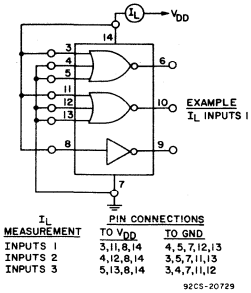


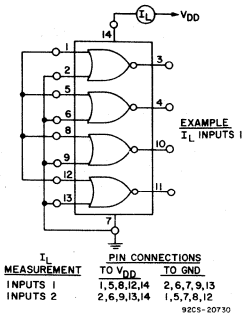
Fig. 17– Typ. dissipation characteristics.

TEST CIRCUITS



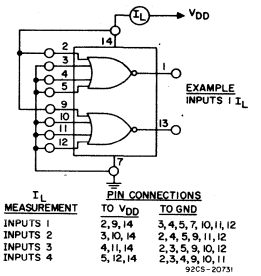
I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	3,11,8,14	4,5,7,12,13
INPUTS 2	4,12,8,14	3,5,7,11,13
INPUTS 3	5,13,8,14	3,4,7,11,12

Fig. 18– Quiescent device current test circuit for CD4000A.



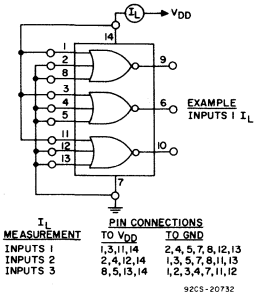
I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	1,5,8,12,14	2,6,7,9,13
INPUTS 2	2,6,9,13,14	1,5,7,8,12

Fig. 19– Quiescent device current test circuit for CD4001A.



I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	2,9,14	3,4,5,7,10,11,12
INPUTS 2	3,10,14	2,4,5,9,11,12
INPUTS 3	4,11,14	2,3,5,9,10,12
INPUTS 4	5,12,14	2,3,4,9,10,11

Fig. 20– Quiescent device current test circuit for CD4002A.



I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	1,3,11,14	2,4,5,7,8,12,13
INPUTS 2	2,4,12,14	1,3,5,7,8,11,13
INPUTS 3	8,5,13,14	1,2,3,4,7,11,12

Fig. 21– Quiescent device current test circuit for CD4025A.

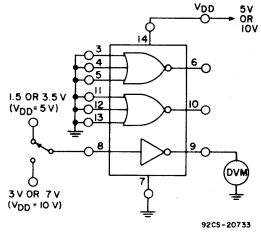


Fig. 22– Noise immunity test circuit for CD4000A.

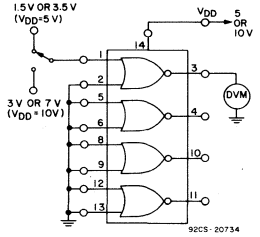


Fig. 23– Noise immunity test circuit for CD4001A.

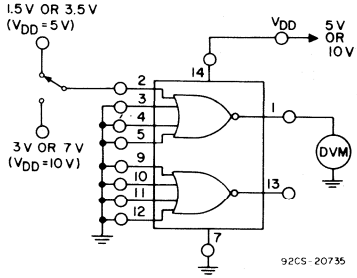


Fig. 24 – Noise immunity test circuit for CD4002A.

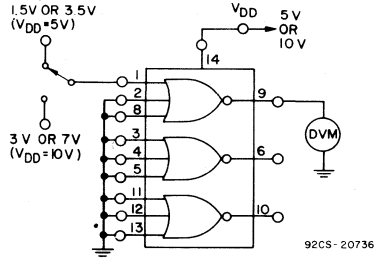


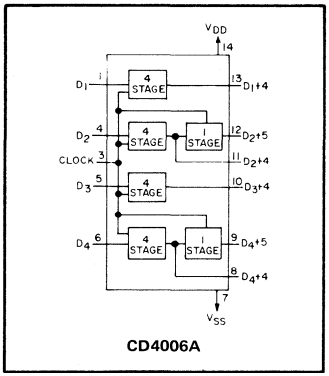
Fig. 25 – Noise immunity test circuit for CD4025A.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4006A/...



CD4006A

High-Reliability COS/MOS 18-Stage Static Shift Register

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

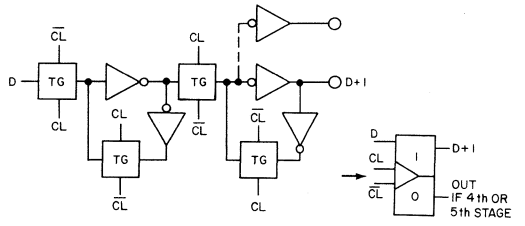
- **Fully static operation**
- **Up to 5 MHz shifting rates**
- **Permanent register storage with clock line "high" or "low" – no information recirculation required**

Applications:

- **Serial shift registers**
- **Time delay circuits**
- **Frequency division**

RCA CD4006A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. CD4006A types are comprised of 4 separate "shift register" sections; two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent "single rail" data path.

A common clock signal is used for all stages. Data is shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17, and 18 can be implemented using one CD4006A package. Longer shift register sections can be assembled by using more than one CD4006A.



TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL ▲	D+1
0	↓	0
1	↓	1
X	↑	NC

NC = NO CHANGE
X = DON'T CARE
▲ = LEVEL CHANGE

92CS-17887

Fig. 1– Logic diagram and truth table (one register stage) for type CD4006A.

These devices are electrically and mechanically identical with standard COS/MOS CD4006A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as shown in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4006A	MIL-M-38510/05701

The packaged types in the CD4006A "Slash" (/) Series can be supplied to six screening levels–/1N, /1R, /1, /2, /3, and /4– which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

screening levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the chart below.

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4006AD, CD4006AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4006AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

The CD4006A "Slash" Series Types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4006AD/1N

CD4006A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4006AH/N

CD4006A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

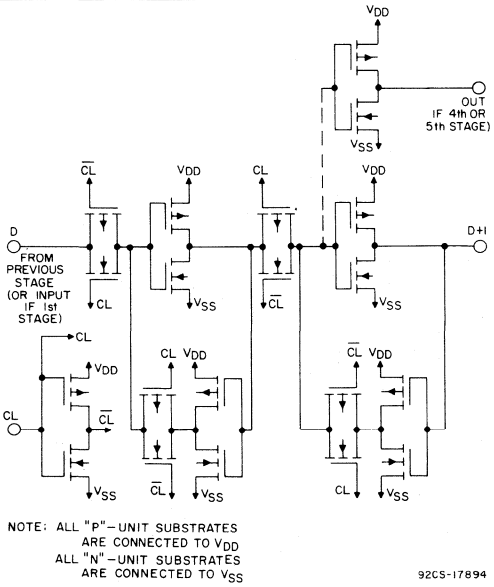


Fig. 2— Schematic diagram (one register stage) for type CD4006A.

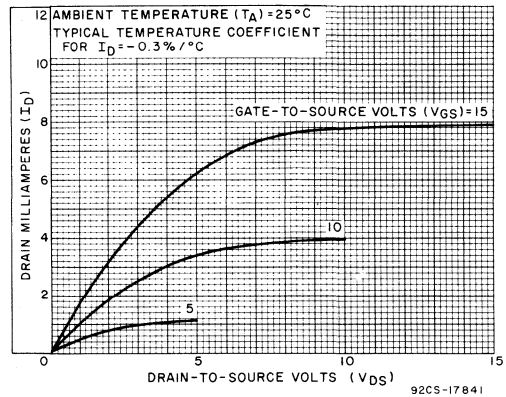


Fig. 3— Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

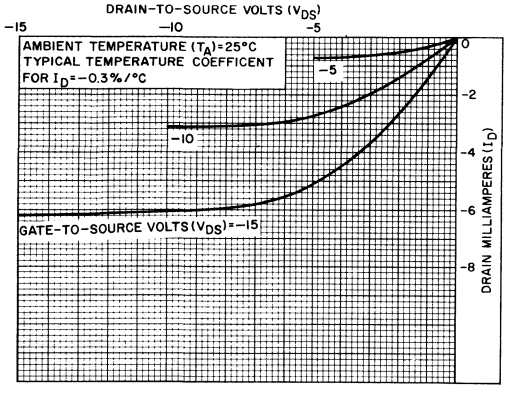
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4006AD, CD4006AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	0.5	–	0.01	0.5	–	–	30	μA	11	1
			10	–	–	1•	–	0.01	1•	–	–	20•			
Quiescent Device Dissipation/Package	P_D		5	–	–	2.5	–	0.05	2.5	–	–	150	μW	–	–
			10	–	–	10	–	0.1	10	–	–	200			
Output Voltage Low-Level	V_{OL}		3	–	–	0.55•	–	–	0.5•	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5•	–	–	0.55•			
High-Level	V_{OH}		3	2.25•	–	–	2.3•	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5•	–	–	14.45•	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = −20 μA		−0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	–	2
P-Channel	V_{THP}	I_D = 20 μA		0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity (Any Input)	V_{NL}	0.5	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	12	1
For Definition, See Appendix SSD-207		0.5	10	3•	–	–	3•	4.5	–	2.9•	–	–			
	V_{NH}	4.5	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V		
		9.5	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: N-Channel	I_DN	0.5	5	0.155	–	–	0.125•	0.25	–	0.085	–	–	mA	3,5	2
		0.5	10	0.31	–	–	0.25•	0.5	–	0.175	–	–			
P-Channel	I_DP	4.5	5	−0.125	–	–	−0.1•	−0.15	–	−0.07	–	–	mA	4,6	2
		9.5	10	−0.25	–	–	−0.2•	−0.3	–	−0.14	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

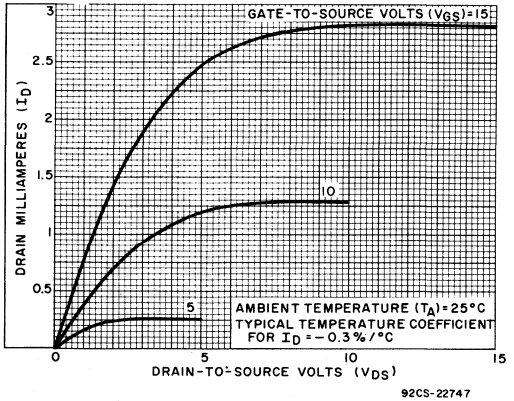
Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.



92CS-17843

Fig. 4— Typical p-channel drain characteristics.



92CS-22747

Fig. 5— Minimum n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			CD4006AD,CD4006AK					
		V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	250	400	ns	7	1
		10	–	125	200●			
Transition Time	t_{THL}, t_{TLH}	5	–	250	400	ns	8	1
		10	–	125	200●			
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	200	500	ns	–	–
		10	–	100	200			
Clock Rise & Fall Time	t_rCL, t_fCL*	5	–	–	15	μs	–	1
		10	–	–	5●			
Set-Up Time		5	–	50	80	ns	–	–
		10	–	25	40			
Maximum Clock Frequency	f_{CL}	5	1	2.5	–	MHz	10	1
		10	2.5●	5	–			
Input Capacitance	C_I	Data Input	–	5	–	pF	–	–
		Clock Input	–	30	–			

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

* If more than one unit is cascaded t_fCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

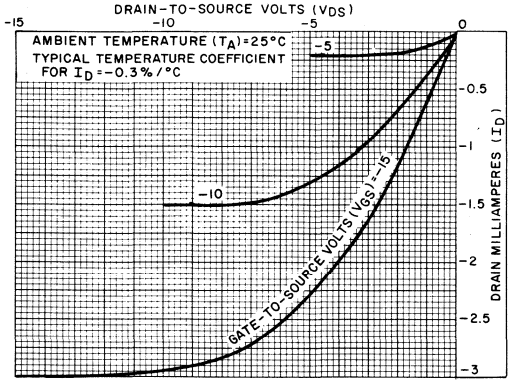


Fig. 6— Minimum p-channel drain characteristics.

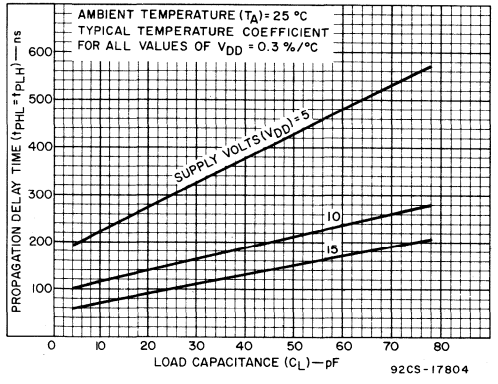


Fig. 7— Typical propagation delay time vs. C_L.

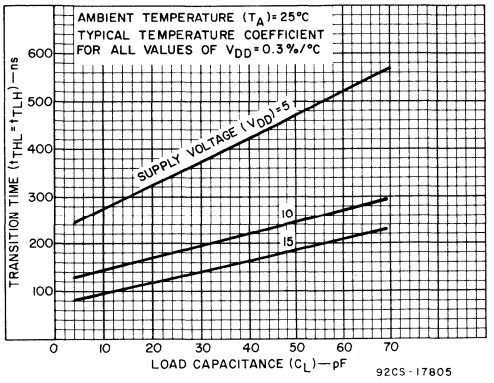


Fig. 8– Typical transition time vs. C_L.

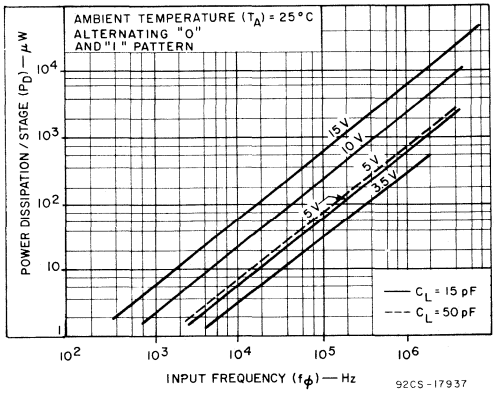


Fig. 9– Typical dissipation characteristics.

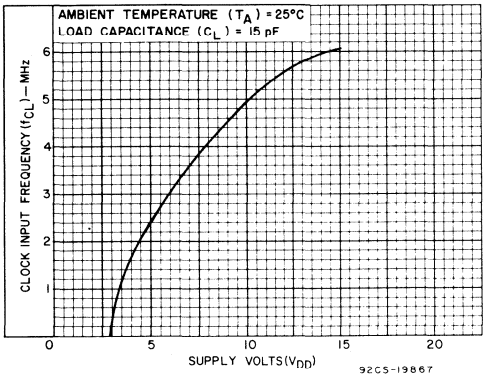
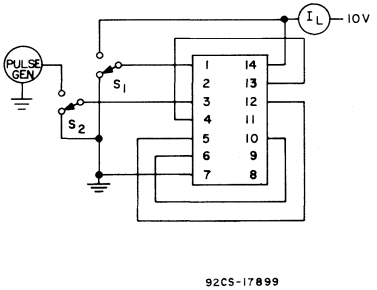


Fig. 10– Typical clock frequency vs. V_{DD}.



With S_1 at ground, clock unit 18 times by connecting S_2 to pulse generator. Return S_2 to ground and measure leakage current. Repeat with S_2 at V_{DD}.

Fig. 11– Quiescent device current test circuit.

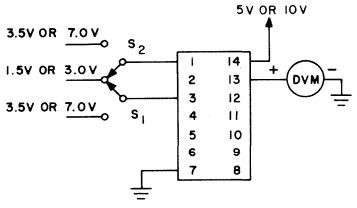


Fig. 12– Noise immunity test circuit.

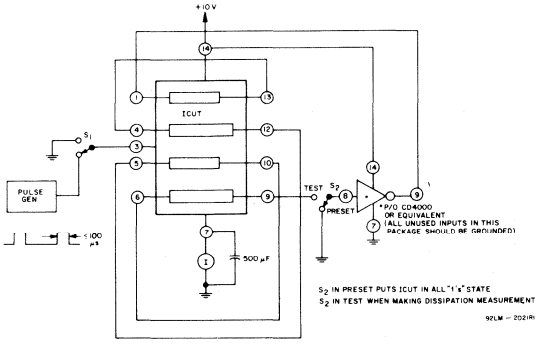


Fig. 13– Device dissipation test setup.

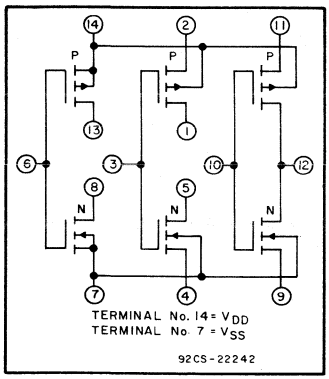
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4007A/...



High-Reliability COS/MOS Dual Complementary Pair Plus Inverter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation . . . $t_{PHL} = t_{PLH}$ = 20 ns (typ.) at C_L = 15 pF**
- **Low "high"- and "low"-output impedance . . . 500 Ω (typ.) at $V_{DD} - V_{SS}$ = 10 V**

Applications:

- **Extremely high-input impedance amplifiers, inverters, shapers, linear amplifiers, threshold detectors**

RCA CD4007A "Slash" (/) Series high-reliability COS/MOS integrated circuits are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits shown in Fig. 1. More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed. For proper operation $V_{SS} \leq V_I \leq V_{DD}$ must be satisfied.

The CD4007A "Slash" (/) Series are electrically and mechanically identical to the standard COS/MOS CD4007A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as shown in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4007A	MIL-M-38510/05301

The packaged types in the CD4007A "Slash" (/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the following page.

The CD4007A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4007AD, CD4007AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4007AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4007AD/1N

CD4007A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4007AH/N

CD4007A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

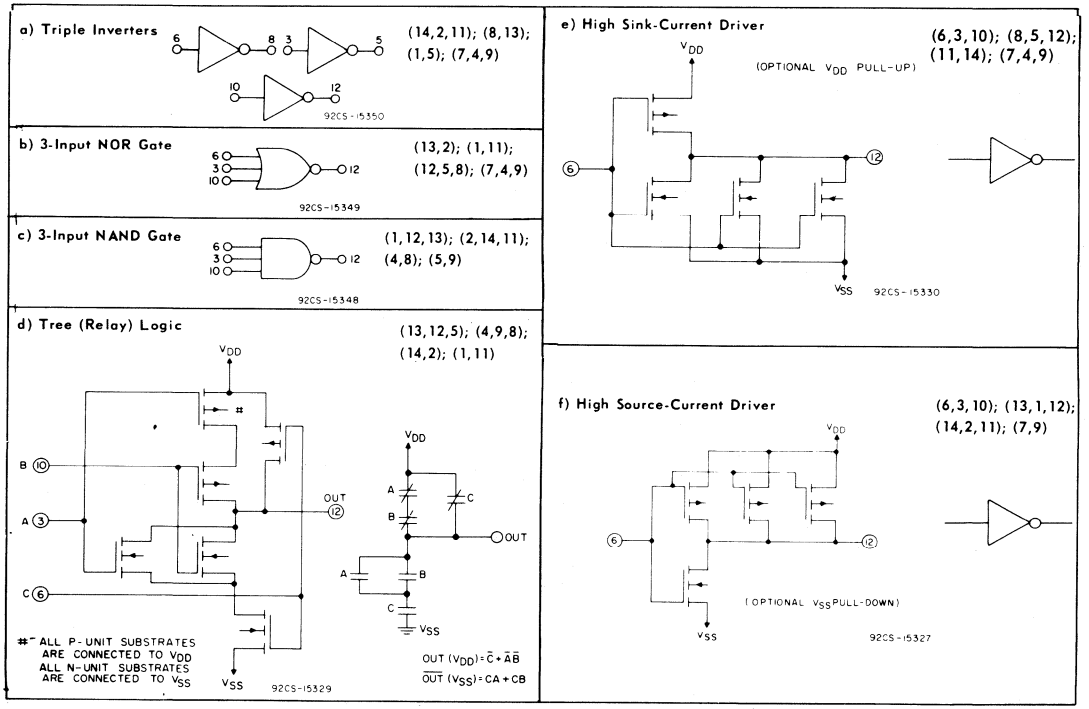


Fig. 1– Sample COS/MOS logic circuit arrangements using type CD4007A. (Continued)

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4007AD, CD4007AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	0.05	–	0.001	0.05	–	–	3	μA	3	1
			10	–	–	0.1•	–	0.001	0.1•	–	–	2•			
Quiescent Device Dissipation/Package	P_D		5	–	–	0.25	–	0.005	0.25	–	–	15	μW	–	–
			10	–	–	1	–	0.01	1	–	–	200			
Output Voltage Low-Level	V_{OL}		5	–	–	0.01	–	0	0.01	–	–	0.05	V	4,5,6 7,8	1
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.6•	–	–	0.7•			
High-Level	V_{OH}		5	4.99	–	–	4.99	5	–	4.95	–	–	V		
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.4•	–	–	14.3•	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	I_D=−10 μA		−0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	–	2
P-Channel	$V_{TH}P$	I_D=10 μA		0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity (Any Input)	V_{NL}	3.6	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	2	1
		7.2	10	3•	–	–	3•	4.5	–	2.9•	–	–			
	V_{NH}	0.95	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V		
		2.9	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: N-Channel	I_DN	V_I=V_{DD} 0	3	0.04•	–	–	0.05•	–	–	–	–	–	mA	9,11	2
		0.4▲	5	0.75	–	–	0.6•	1	–	0.4	–	–			
		0.5	10	1.6	–	–	1.5•	2.5	–	0.95	–	–			
P-Channel	I_DP	V_I=V_{SS} 3	3	−0.04•	–	–	−0.05•	–	–	–	–	–	mA	10,12	2
		2.5†	5	−1.75	–	–	−1.4•	−4	–	−1	–	–			
		9.5	10	−1.35	–	–	−1.1•	−2.5	–	−0.75	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

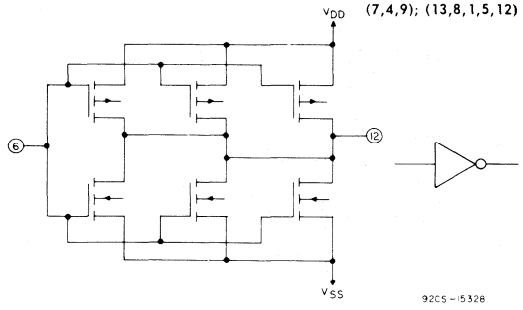
Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

▲Maximum noise-free saturated Bipolar output voltage.
†Minimum noise-free saturated Bipolar output voltage.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

g) High Sink- and Source-Current Driver (6,3,10); (14,2,11); (7,4,9); (13,8,1,5,12)



h) Dual Bi-Directional Transmission Gating (1,5,12); (2,9); (11,4); (8,13,10); (6,3)

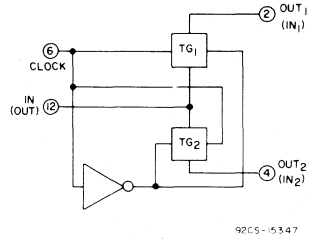


Fig. 1– Sample COS/MOS logic circuit arrangements using type CD4007A.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4007AD,CD4007AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.		Fig. No.	
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	–	35	60	ns	13,15	1
			10	–	20	40●			
Low-to-High Level	t_{PLH}		5	–	35	60	ns	13,15	1
			10	–	20	40●			
Transition Time: High-to-Low Level	t_{THL}		5	–	50	75	ns	14	1
			10	–	30	40●			
Low-to-High Level	t_{TLH}		5	–	50	75	ns	14	1
			10	–	30	40●			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

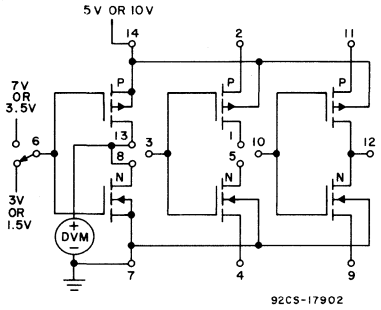


Fig. 2– Noise immunity test circuit.

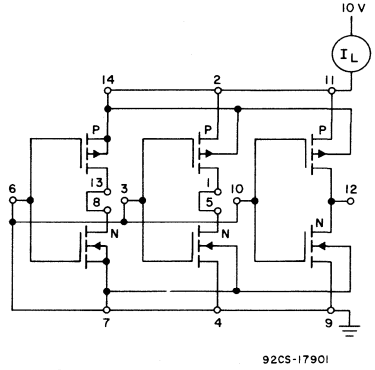


Fig. 3– Quiescent device current test circuit.

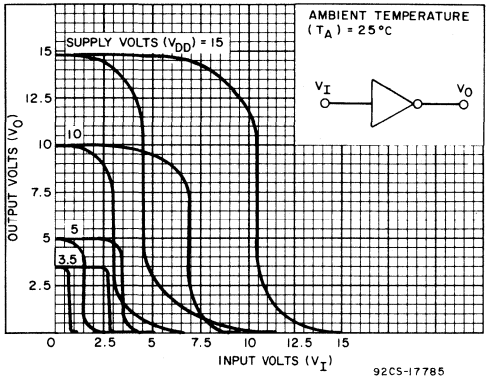


Fig. 4– Min. and max. voltage transfer characteristics for inverter.

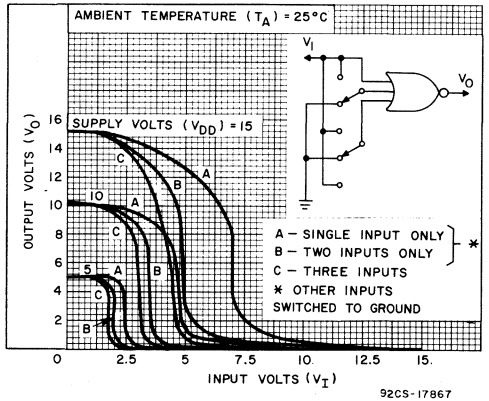


Fig. 5– Typ. voltage transfer characteristics for NOR gate.

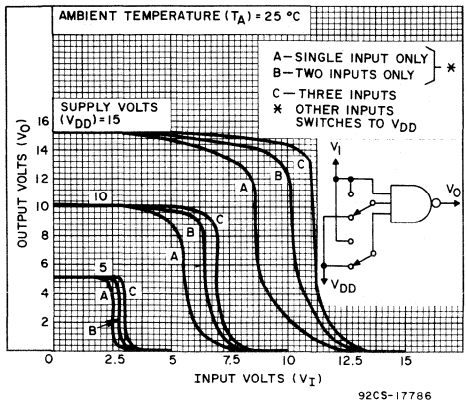


Fig. 6— Typ. voltage transfer characteristics for NAND gate.

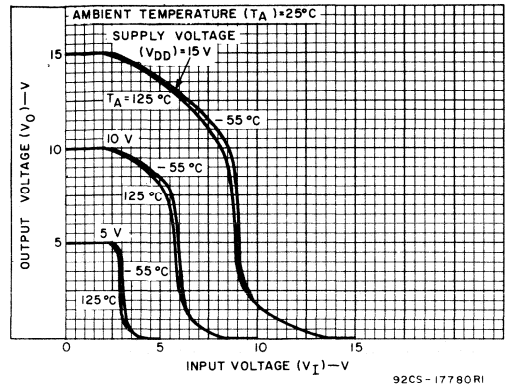


Fig. 7— Typ. voltage transfer characteristics as a function of temp.

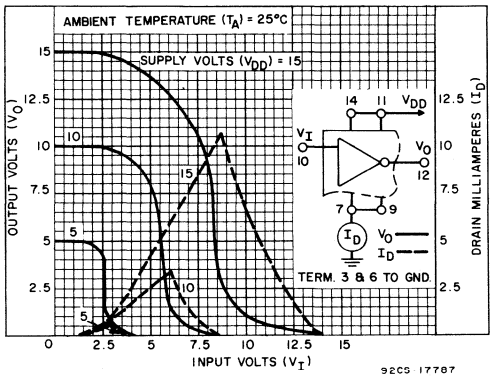


Fig. 8— Typ. current and voltage transfer characteristics for inverter.

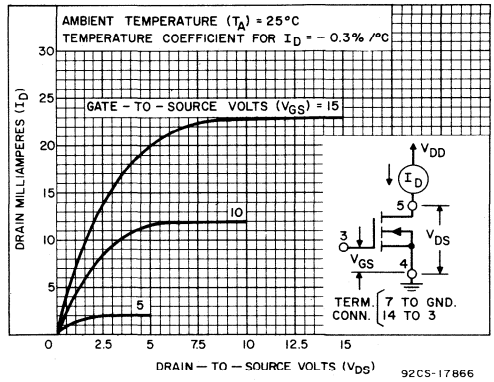


Fig. 9— Typ. n-channel drain characteristics.

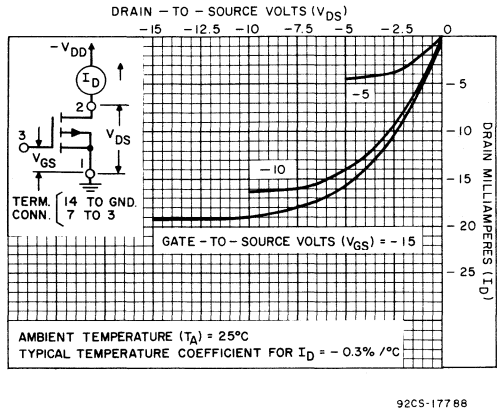


Fig. 10— Typ. p-channel drain characteristics.

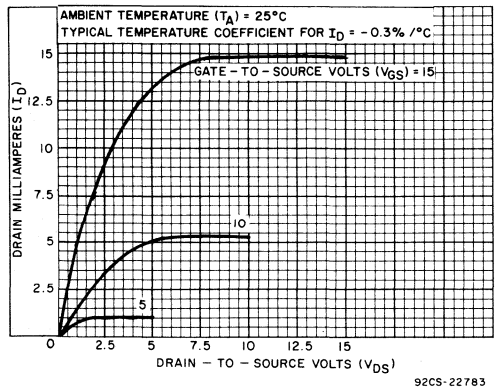


Fig. 11— Minimum n-channel drain characteristics.

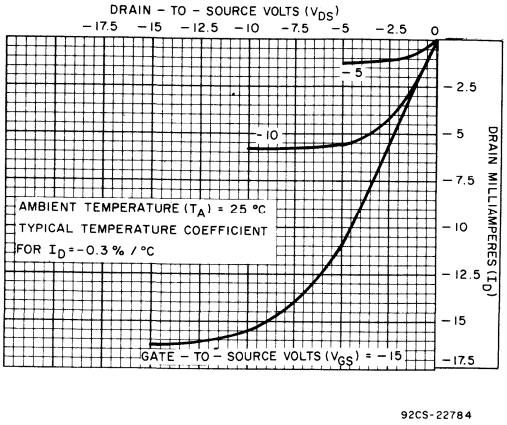


Fig. 12– Minimum p-channel drain characteristics.

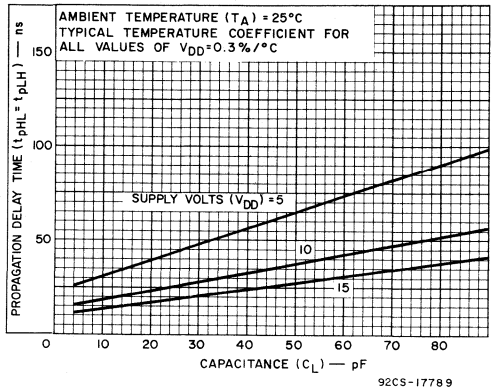


Fig. 13– Typical propagation delay time vs. C_L.

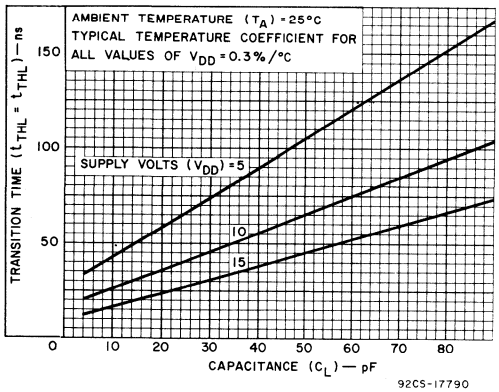


Fig. 14– Typical transition time vs. C_L.

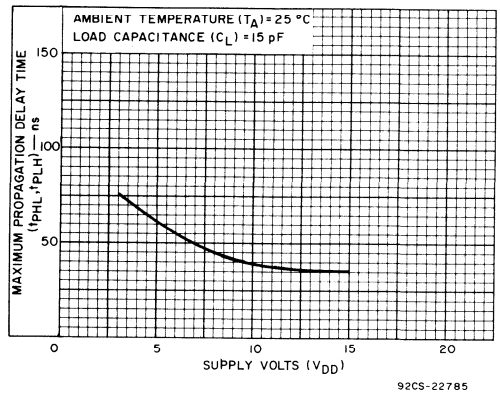


Fig. 15– Maximum propagation delay time vs. V_{DD}.

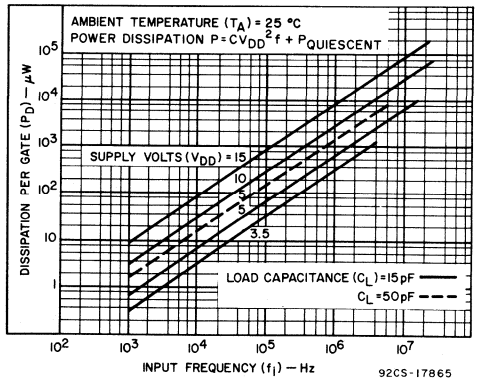


Fig. 16– Typical dissipation characteristics.

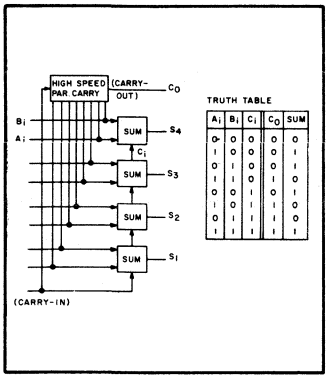
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4008A/...



High-Reliability COS/MOS Four-Bit Full Adder With Parallel Carry-Out

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **MSI complexity on a single chip . . . 4 Sum Outputs plus parallel Carry Output**
- **High speed operation . . . Carry-In to Carry-Out delay, t_{PHL}, t_{PLH} = 45 ns at C_L = 15 pF**

Applications:

- **Binary addition/arithmetic units**

RCA CD4008A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4008A types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008A's. CD4008A inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "carry-in" bit from a previous section. CD4008A outputs include the four sum bits, S_1 to S_4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008A section.

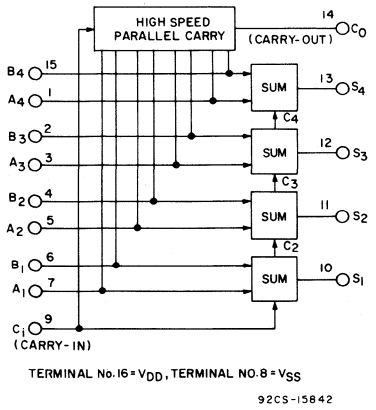


Fig. 1– Logic diagram for type CD4008A.

These devices are electrically and mechanically identical to the standard COS/MOS CD4008A described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4008A	MIL-M-38510/05401

The packaged types in the CD4008A "Slash" (/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended	
DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended	
Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering)	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the chart below.

The CD4008A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4008AD, CD4008AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4008AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4008AD/1N

CD4008A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4008AH/N

CD4008A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

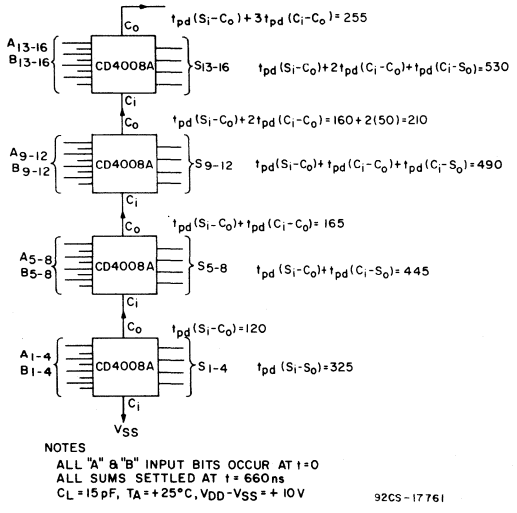


Fig. 2— Typical speed characteristics of a 16-bit adder.

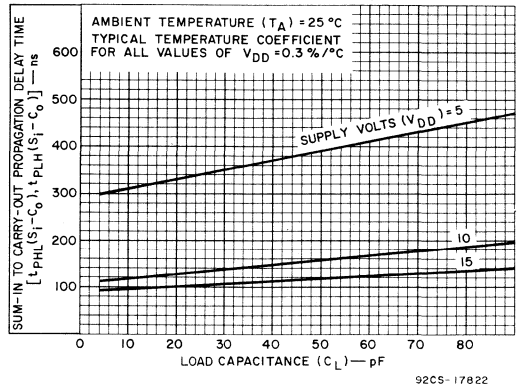


Fig. 3— Sum-in to carry-out propagation delay time vs. C_L.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4008AD,CD4008AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.3	5	–	–	300	μA	9	1
			10	–	–	10•	–	0.5	10•	–	–	200•			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	1.5	25	–	–	1500	μW	–	–
			10	–	–	100	–	5	100	–	–	2000			
Output Voltage Low-Level	V_{OL}		3	–	–	0.55•	–	–	0.5•	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5•	–	–	0.55•			
High-Level	V_{OH}		3	2.25•	–	–	2.3•	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5•	–	–	14.45•	–	–			
Threshold Voltage N-Channel	$V_{TH}N$	I_D = −20 μA		−0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	–	2
P-Channel	$V_{TH}P$	I_D = 20 μA		0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity (Any Input)	V_{NL}	0.95	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	10	2
		2.9	10	3•	–	–	3•	4.5	–	2.9•	–	–			
For Definition, See Appendix SSD-207	V_{NH}	3.6	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V		
		7.2	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current N-Channel	$I_D N$	Carry Output 0.5	5	0.31		–	0.25•	0.5	–	0.175	–	–	mA	–	2
		0.5	10	0.93			0.75•	1.5	–	0.53	–	–			
		Sum Output 3	5	0.12	–	–	0.1•	0.2	–	0.07	–	–			
		3	10	0.31	–	–	0.25•	0.5	–	0.175	–	–			
P-Channel	$I_D P$	Carry Output 4.5	5	−0.31		–	−0.25•	−0.5	–	−0.175	–	–	mA		
		9.5	10	−0.93			−0.75•	−1.5	–	−0.53	–	–			
		Sum Output 2	5	−0.12	–	–	−0.1•	−0.2	–	0.07	–	–			
		7	10	−0.185	–	–	−0.15•	−0.3	–	−0.105	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

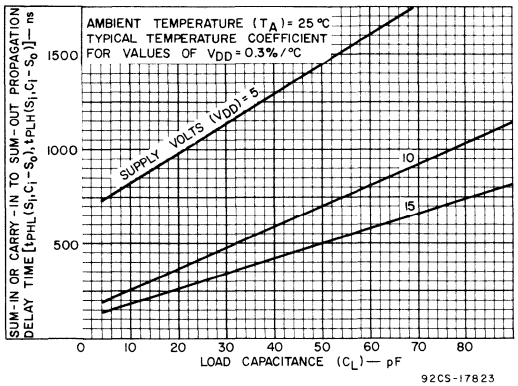


Fig. 4— Sum-in or carry-in to sum-out propagation delay time vs. C_L.

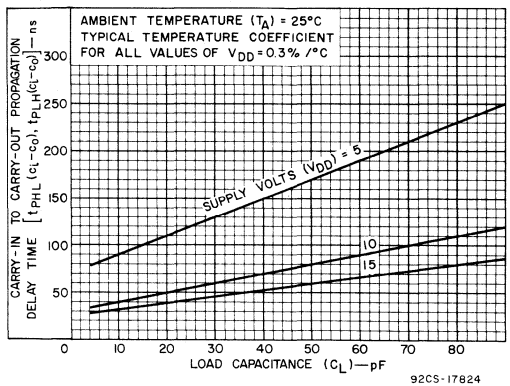


Fig. 5— Carry-in to carry-out propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4008AD,CD4008AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Propagation Delay Time: At Sum Outputs; From Sum Input	t_{PHL}, t_{PLH}	5	–	900	1300	ns	4	1
		10	–	325	500●			
From Carry Input		5	–	900	1300	ns		
		10	–	325	500			
At Carry Output; From Sum Input		5	–	320	600	ns	3	–
		10	–	120	200			
From Carry Input		5	–	100	175	ns	5	1
		10	–	45	75●			
Transition Time: At Sum Outputs	t_{THL}, t_{TLH}	5	–	1250	2200	ns	–	–
		10	–	550	900			
At Carry Output		5	–	125	225	ns	–	–
		10	–	45	75			
Input Capacitance	C_I	Any Input	–	10	–	pF	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

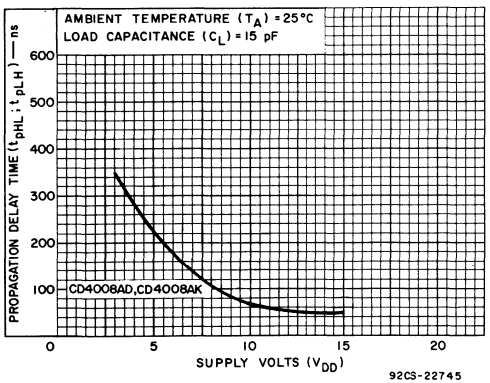


Fig. 6— Max. propagation delay time vs. V_{DD} for carry-in to carry-out.

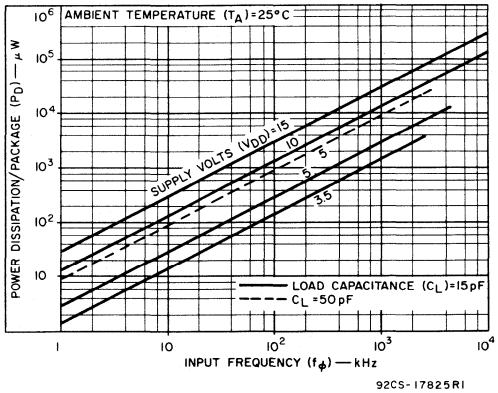


Fig. 7— Typical dissipation characteristics.

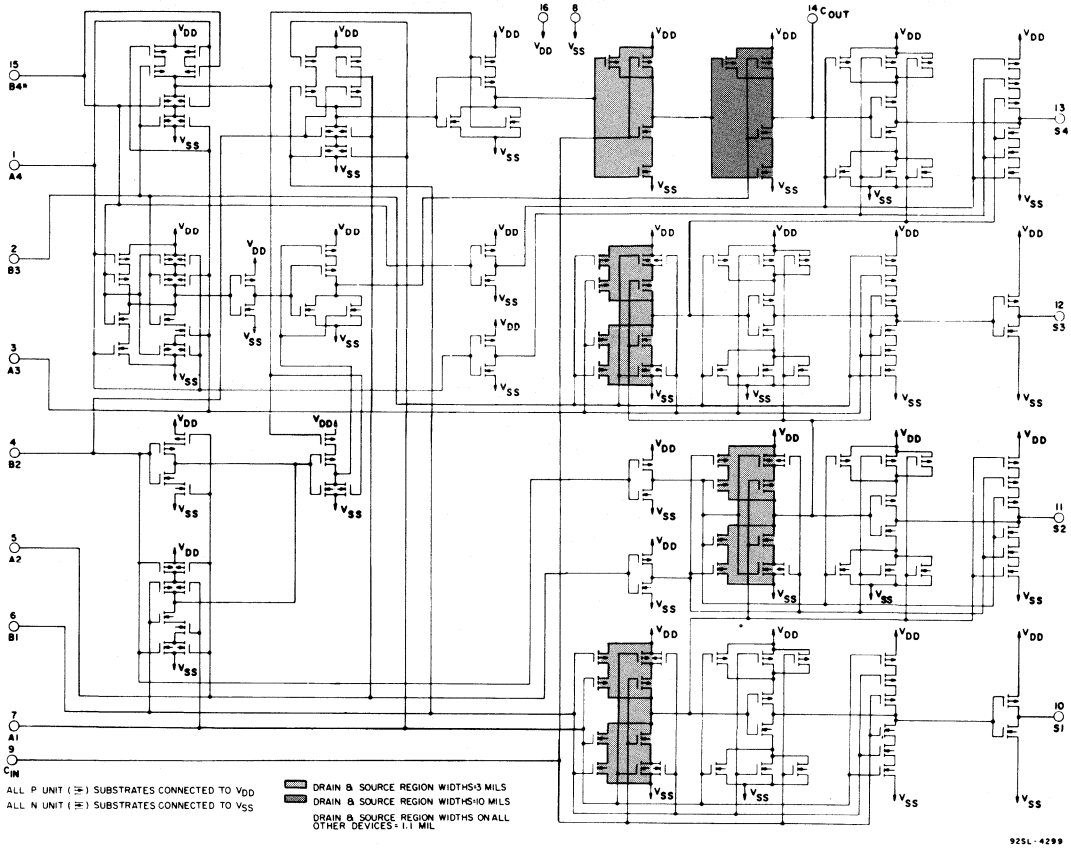


Fig. 8– Schematic diagram.

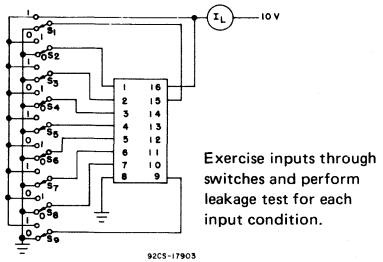


Fig. 9– Quiescent device current test circuit.

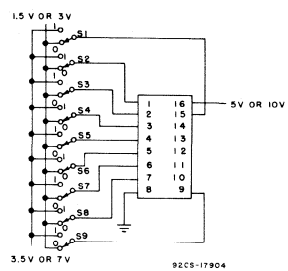


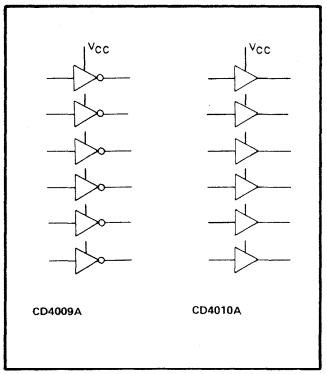
Fig. 10– Noise immunity test circuit.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4009A/..., CD4010A/...



High-Reliability COS/MOS Hex Buffers/Converters

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Inverting Type: CD4009AD, CD4009AK

Non-Inverting Type: CD4010AD, CD4010AK

Special Features (Each Buffer):

- **High current sinking capability . . . 8 mA (min. at V_{OL} = 0.5 V and V_{DD} = +10 V**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS hex inverter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS logic-level converter**
- **Multiplexer — 1 to 6 or 6 to 1**

CAUTION:
V_{CC} VOLTAGE LEVEL MUST BE EQUAL TO OR LESS THAN V_{DD}. FOR 10.5- TO 15-VOLT SUPPLIES, C_{LOAD} MUST BE EQUAL TO OR LESS THAN 5000 pF.

RCA CD4009A and CD4010A "Slash" (/) Series are high-reliability integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4009A types may be used as a hex COS/MOS inverter, a COS/MOS to DTL or TTL logic-level converter, or a COS/MOS current driver. CD4010A types may be used as a COS/MOS to DTL or TTL hex converter or a COS/MOS current driver.

Conversion ranges are from COS/MOS logic operating at +3 V to +15 V supply levels to DTL or TTL logic operating at +3 V to +6 V supply levels. Conversion to logic output levels greater than +6 V is permitted providing V_{CC}(DTL/TTL) $\leq$ V_{DD}(COS/MOS).

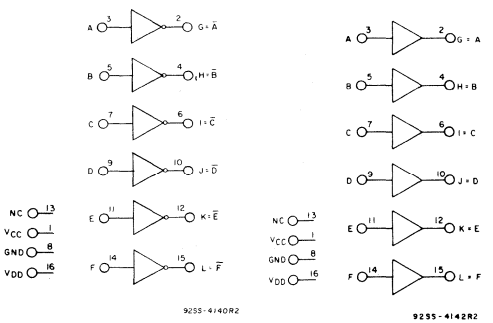


Fig. 1— Logic diagrams for types CD4009A and CD4010A.

These devices are electrically and mechanically identical with standard COS/MOS types CD4009A and CD4010A described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4009A	MIL-M-38510/05501
CD4010A	MIL-M-38510/05502

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

The packaged types in the CD4009A and CD4010A "Slash" (/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types"*

For a listing of the Screening Level Options available for both packaged devices and chips and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the chart below.

The CD4009A and CD4010A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4009AD, CD4009AK, CD4010AD, CD4010AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4009AH, CD4010AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4009AD/1N

CD4009A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4009AH/N

CD4009A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

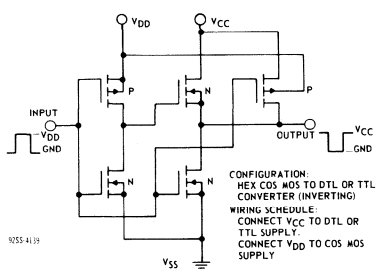


Fig. 2– Schematic diagram for types CD4009A (one of 6 identical stages).

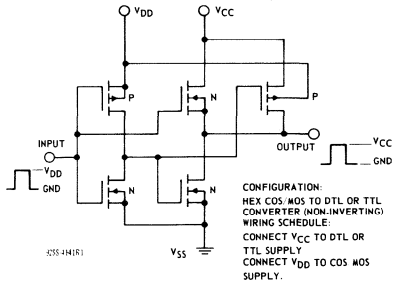


Fig. 3– Schematic diagram for types CD4010A (one of 6 identical stages).

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} < V_I < V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4009AD,CD4009AK,CD4010AD,CD4010AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			V_O	V_{DD}	−55°C			25°C			125°C					
			Volts	Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current:	I_L			5	–	–	0.3	–	0.01	0.3	–	–	20	μA	21	1
				10	–	–	0.5•	–	0.01	0.5•	–	–	10•			
Quiescent Device Dissipation/Package	P_D			5	–	–	1.5	–	0.05	1.5	–	–	100	μW	20	–
				10	–	–	5	–	0.1	5	–	–	100			
Output Voltage: Low-Level	V_{OL}			5	–	–	0.01	–	0	0.01	–	–	0.05	V	4,5,6 7,8,9	1
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.6•	–	–	0.7•			
High-Level	V_{OH}			5	4.99	–	–	4.99	5	–	4.95	–	–	V		
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.4•	–	–	14.3•	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	I_D=−10 μA			−0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	–	2
P-Channel	$V_{TH}P$	I_D=10 μA			0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity (Any Input) CD4009A	V_{NL}	V_{OH}=3.6 V		5	1	–	–	1•	2.25	–	0.9	–	–	V	22	1
		V_{OH}=7.2 V		10	2•	–	–	2•	4.5	–	1.9•	–	–			
CD4010A		V_{OL}=0.95 V		5	1.5	–	–	1.5•	2.25	–	1.4	–	–			
		V_{OL}=2.9 V		10	3•	–	–	3•	4.5	–	2.9•	–	–			
CD4009A	V_{NH}	V_{OL}=0.95 V		5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V		
		V_{OL}=2.0 V		10	2.9•	–	–	3•	4.5	–	3•	–	–			
CD4010A		V_{OH}=3.6 V		5	1.4	–	–	1.5•	2.25	–	1.5	–	–			
		V_{OH}=7.2 V		10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: N-Channel	I_DN	CD4009A & CD4010A	0.4	5	3.75	–	–	3•	4	–	2.1	–	–	mA	11,12	2
			0.5	10	10	–	–	8•	10	–	5.6	–	–			
		CD4009A	0	3	0.4•	–	–	0.5•	–	–	–	–	–			
		CD4010A	0	3	0.02•	–	–	0.025•	–	–	–	–	–			
P-Channel	I_DP	CD4009A & CD4010A	2.5	5	−1.85	–	–	−1.25•	−1.75	–	−0.9	–	–		11,12	2
			9.5	10	−0.9	–	–	−0.6•	−0.8	–	−0.4	–	–			
		CD4009A	3	3	−0.04•	–	–	−0.05•	–	–	–	–	–			
		CD4010A	3	3	−0.02•	–	–	−0.025•	–	–	–	–	–			
Diode Test	V_{DF}	100 μA Test Pin			–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4009AD,CD4009AK CD4010AD,CD4010AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Propagation Delay Time: High-to-Low Level	t_{PHL}	$V_{CC} = V_{DD}$	5	–	15	55	ns	13	1
			10	–	10	30●			
		V_{DD} = 10 V, V_{CC} = 5 V		–	10	25			
Low-to-High Level	t_{PLH}	$V_{CC} = V_{DD}$	5	–	50	80	ns	14	–
			10	–	25	55●			
		V_{DD} = 10 V, V_{CC} = 5 V		–	15	30			
Transition Time: High-to-Low Level	t_{THL}	$V_{CC} = V_{DD}$	5	–	20	45	ns	17	1
			10	–	16	40●			
Low-to-High Level	t_{TLH}	$V_{CC} = V_{DD}$	5	–	80	125	ns	18	1
			10	–	50	100●			
Input Capacitance (Any Input)	C_I	CD4009A		–	15	–	pF	–	–
		CD4010A		–	5	–			

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

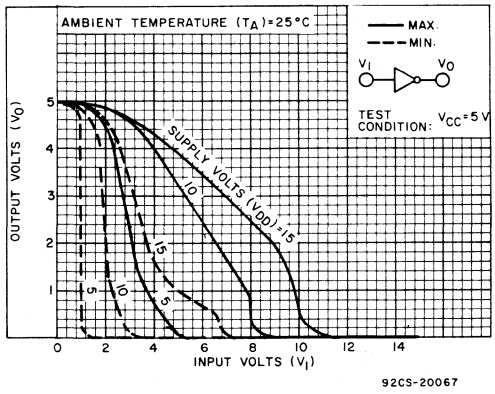


Fig. 4– Min. and max. voltage transfer characteristics – CD4009A.

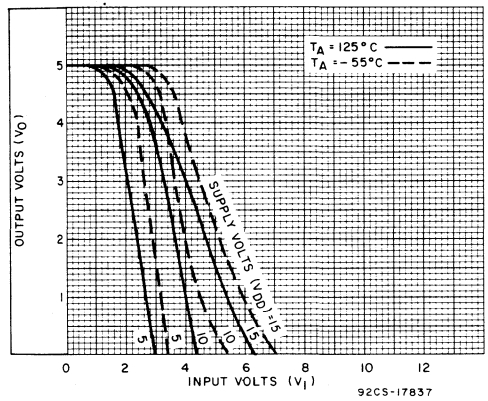


Fig. 5– Typical voltage transfer characteristics as function of temp. – CD4009A.

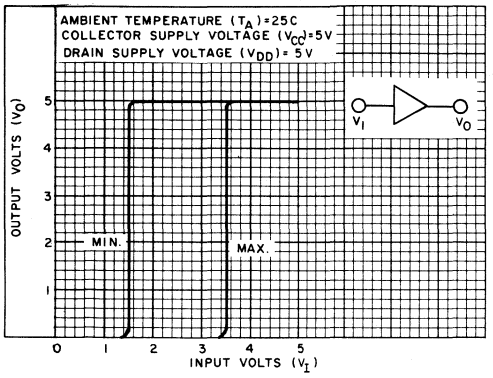


Fig. 6– Min. and max. voltage transfer characteristics (V_{DD} = 5) – CD4010A.

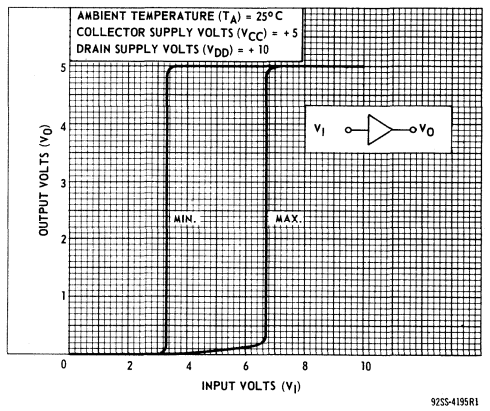


Fig. 7– Min. and max. voltage transfer characteristics (V_{DD} = 10) – CD4010A.

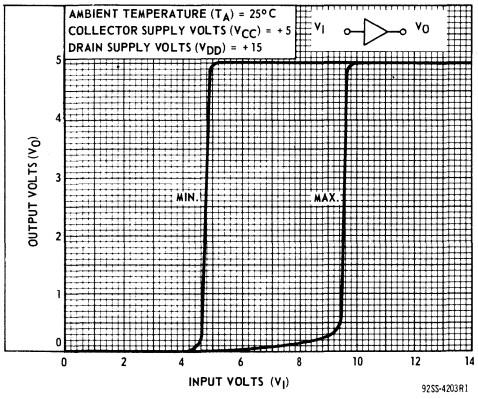


Fig. 8– Min. and max. voltage transfer characteristics (V_{DD} = 15) – CD4010A.

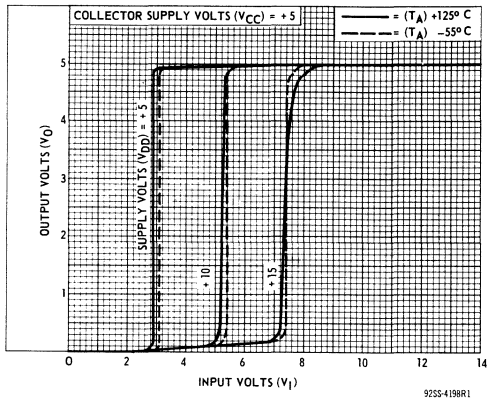


Fig. 9– Typical voltage transfer characteristics as a function of temp. – CD4010A.

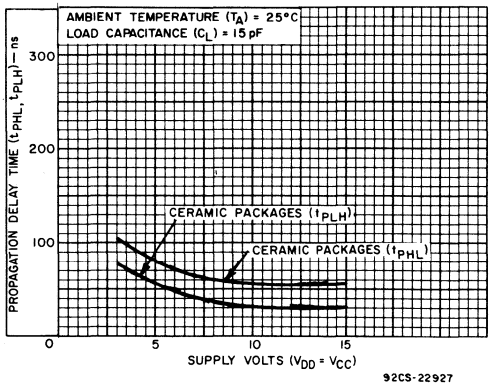


Fig. 10– Maximum propagation delay time vs. V_{DD} – CD4010A.

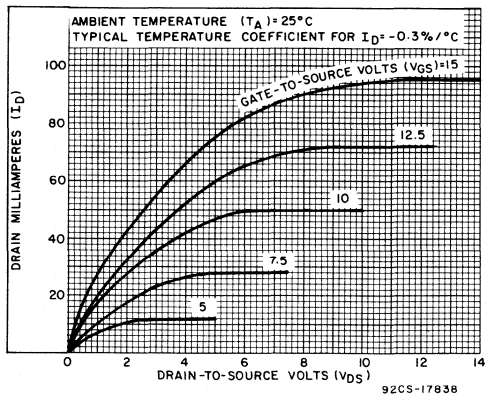


Fig. 11– Typical n-channel drain characteristics – CD4009A, CD4010A.

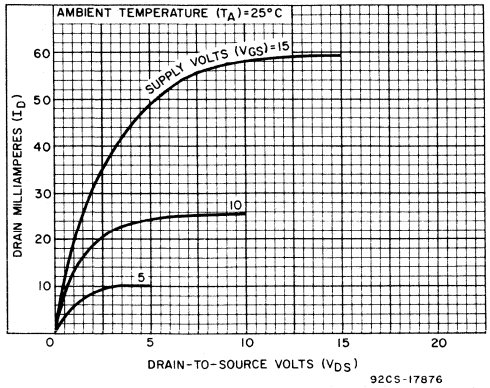


Fig. 12– Minimum n-channel drain characteristics.

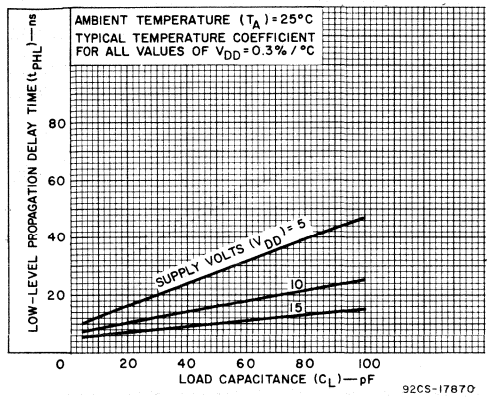


Fig. 13– Typical high-to-low level propagation delay time vs. C_L – CD4009A, CD4010A.

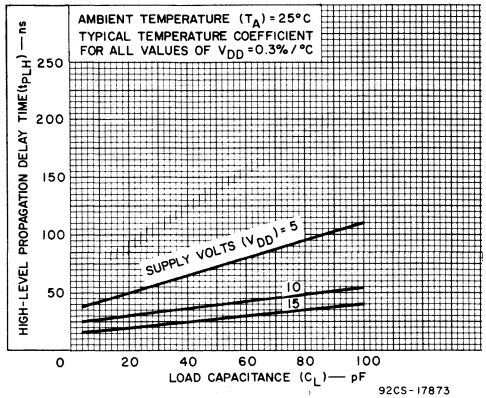


Fig. 14– Typical low-to-high level propagation delay time vs. C_L – CD4009A, CD4010A.

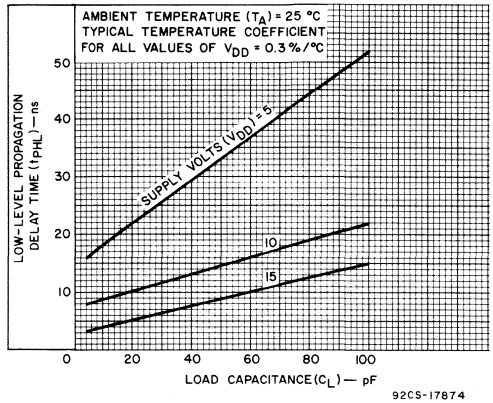


Fig. 15– Typical high-to-low level propagation delay time vs. C_L (driving TTL, DTL) – CD4009A, CD4010A.

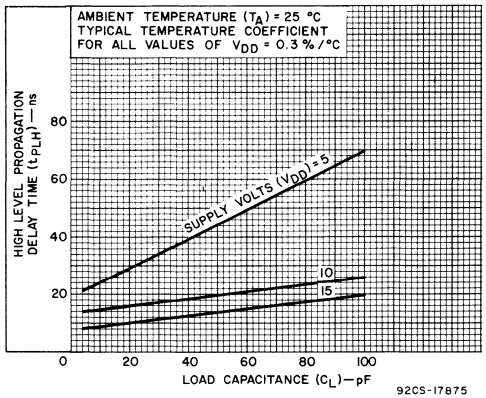


Fig. 16– Typical low-to-high level propagation delay time vs. C_L (driving TTL, DTL) – CD4009A, CD4010A.

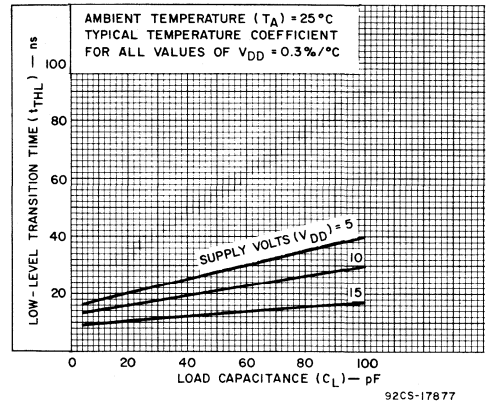


Fig. 17– Typical high-to-low level transition time vs. C_L – CD4009A, CD4010A.

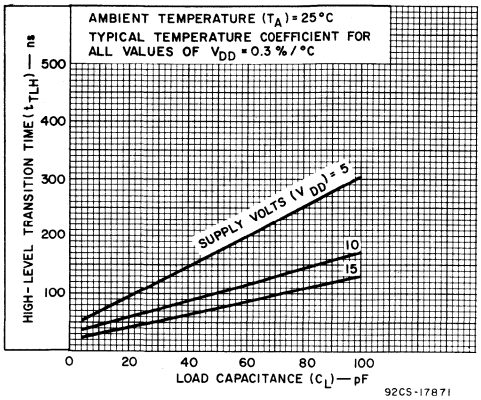


Fig. 18— Typical low-to-high level transition time vs. C_L — CD4009A, CD4010A.

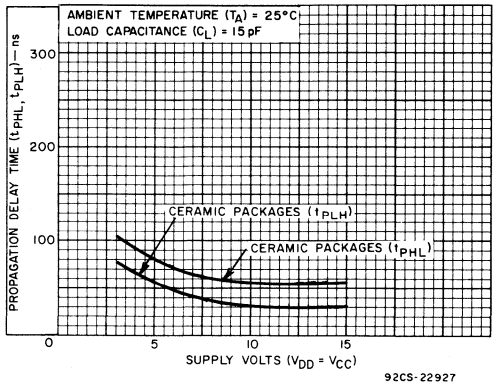


Fig. 19— Maximum propagation delay time vs. V_{DD} — CD4009A.

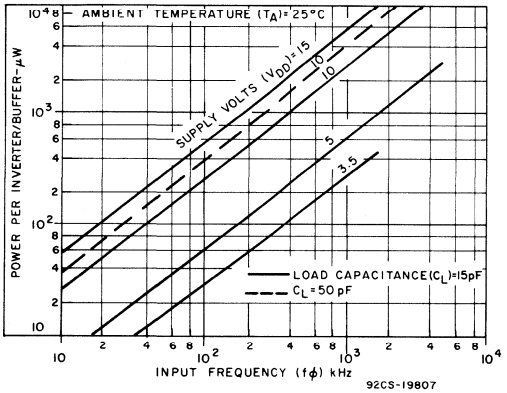


Fig. 20— Typical dissipation characteristics — CD4009A, CD4010A.

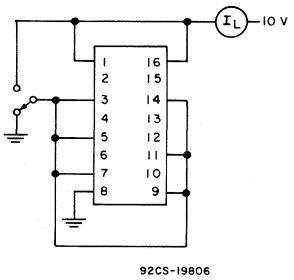


Fig. 21— Quiescent device current test circuit.

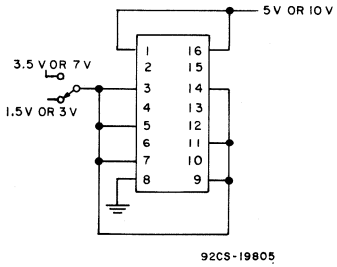


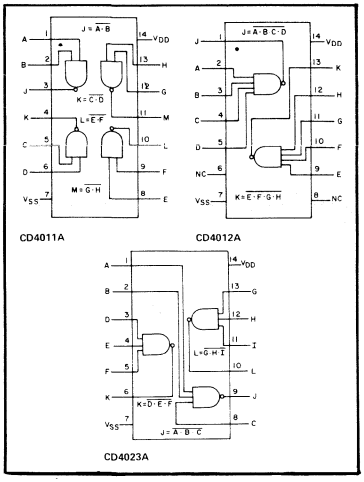
Fig. 22— Noise immunity test circuit.

RCA
Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4011A/..., CD4012A/..., CD4023A/...



High-Reliability COS/MOS NAND Gates (Positive Logic)

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Quad 2 Input — — — CD4011AD, CD4011AK
Dual 4 Input — — — CD4012AD, CD4012AK
Triple 3 Input — — — CD4023AD, CD4023AK

Special Features:

- **Medium speed operation . . . $t_{PHL} = t_{PLH}$ = 25 ns (typ.) at C_L = 15 pF**
- **Low "high"- and "low"-level output impedance . . . 400 and 800 Ω (typ.), respectively, at $V_{DD} - V_{SS}$ = 10 V**

RCA CD4011A, CD4012A, and CD4023A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. The combination of these devices and the RCA NOR positive logic gate types CD4000A, CD4001A, CD4002A, and CD4025A can account for appreciable package count savings in various logic function configurations. These devices are electrically and mechanically identical with standard COS/MOS types CD4011A, CD4012A, and CD4023A described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4011A	MIL-M-38510/05001
CD4012A	MIL-M-38510/05002
CD4023A	MIL-M-38510/05003

The packaged types in the CD4011A, CD4012A, and CD4023A "Slash" (/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the following page.

The CD4011A, CD4012A, and CD4023A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4011AD, CD4011AK, CD4012AD, CD4012AK, CD4023AD, CD4023AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4011AH, CD4012AH, CD4023AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4011AD/1N

CD4011A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4011AH/N

CD4011A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

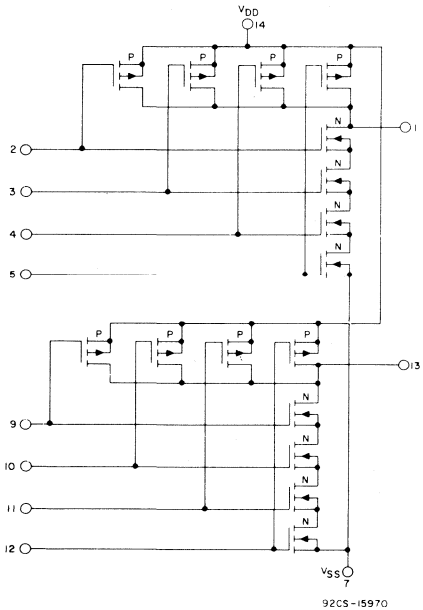


Fig. 1— Schematic diagram for type CD4012A.

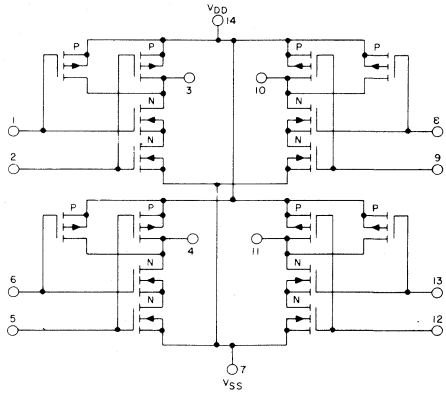


Fig. 2— Schematic diagram for type CD4011A.

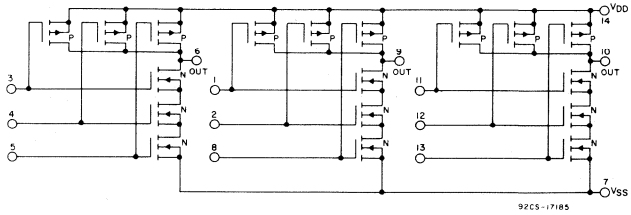


Fig. 3— Schematic diagram for type CD4023A.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
					CD4011AD,CD4012AD,CD4023AD, CD4011AK,CD4012AK,CD4023AK											
		V_O Volts	V_{DD} Volts		−55°C			25°C			125°C					
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I_L			5	–	–	0.05	–	0.001	0.05	–	–	3	μA	21, 23, 25	1
				10	–	–	0.1•	–	0.001	0.1•	–	–	2•			
Quiescent Device Dissipation/Package	P_D			5	–	–	0.25	–	0.005	0.25	–	–	15	μW	20	–
				10	–	–	1	–	0.01	1	–	–	20			
Output Voltage Low-Level	V_{OL}			5	–	–	0.01	–	0	0.01	–	–	0.05	V	4,5,6,7	1
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.6•	–	–	0.7•			
High-Level	V_{OH}			5	4.99	–	–	4.99	5	–	4.95	–	–	V		1
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.4•	–	–	14.3•	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	I_D=−10 μA			−0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	–	2
P-Channel	$V_{TH}P$	I_D=10 μA			0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity Any Input	V_{NL}		3.6	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	–	2
For Definition, See Appendix			7.2	10	3•	–	–	3•	4.5	–	2.9•	–	–			
	V_{NH}		0.95	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V	22, 24, 26	2
			2.9	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: N-Channel	I_DN	CD4011A CD4023A Series	0	3	0.02•	–	–	0.025•	–	–	–	–	–	mA	8, 10	2
			0.5	5	0.31	–	–	0.25•	0.5	–	0.175	–	–			
			0.5	10	0.62	–	–	0.5•	0.6	–	0.35	–	–			
		CD4012A Series	0	3	0.02•	–	–	0.025•	–	–	–	–	–	mA	8, 11	2
			0.5	5	0.15	–	–	0.12•	0.25	–	0.085	–	–			
			0.5	10	3.1	–	–	0.25•	0.6	–	0.175	–	–			
P-Channel	I_DP		3	3	−0.02•	–	–	−0.025•	–	–	–	–	–	mA	9, 12	2
			4.5	5	−0.31	–	–	−0.25•	−0.5	–	−0.175	–	–			
			9.5	10	−0.75	–	–	−0.6•	−1.2	–	−0.4	–	–			
Diode Test	V_{DF}	100 μA Test Pin			–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

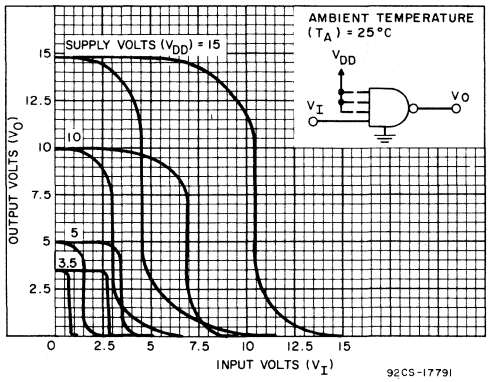


Fig. 4— Min. and max. voltage transfer characteristics.

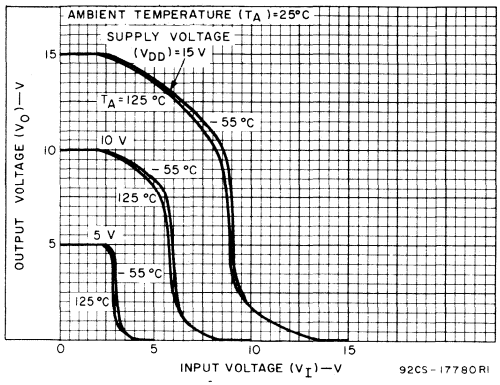


Fig. 5— Typical voltage transfer characteristics as a function of temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4011AD, AK CD4012AD, AK CD4023AD, AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Propagation Delay Time: Low-to-High Level	t_{PLH}	5	–	50	75	ns	13	1
		10	–	25	40●		19	
High-to-Low Level CD4011A and CD4023A Series	t_{PHL}	5	–	50	75	ns	14	1
		10	–	25	40●		19	
CD4012A Series		5	–	100	150	ns	15	1
		10	–	50	75●		19	
Transition Time: Low-to-High Level	t_{TLH}	5	–	75	100	ns	16	1
		10	–	40	60●			
High-to-Low Level CD4011A and CD4023A Series	t_{THL}	5	–	75	125	ns	17	1
		10	–	50	75●			
CD4012A Series		5	–	250	375	ns	18	1
		10	–	125	200●			
Input Capacitance	C_I	Any Input	–	5	–	pF	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

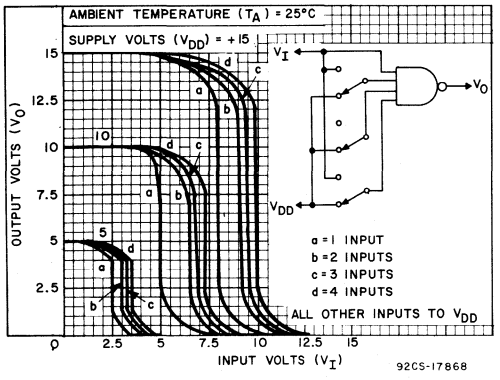


Fig. 6— Typical multiple input switching transfer characteristics for CD4012A.

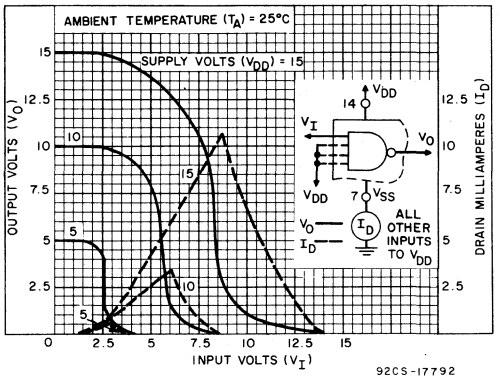


Fig. 7— Typical current and voltage transfer characteristics.

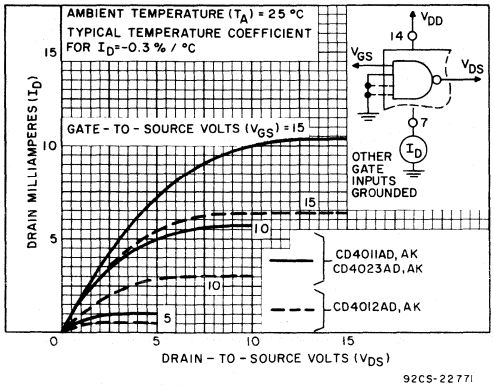


Fig. 8– Typical n-channel drain characteristics.

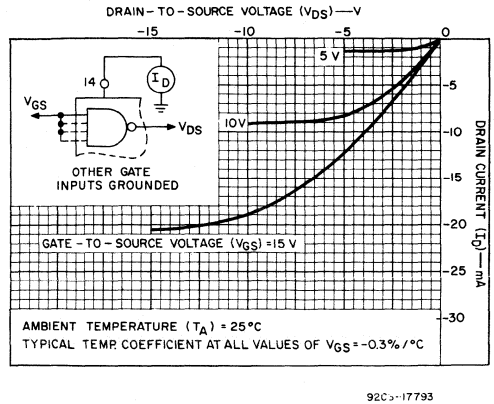


Fig. 9– Typical p-channel drain characteristics.

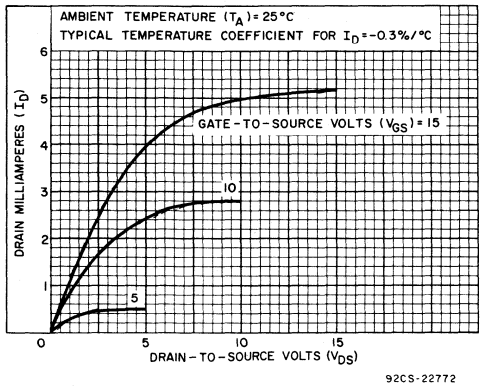


Fig. 10– Minimum n-channel drain characteristics – CD4011A and CD4023A.

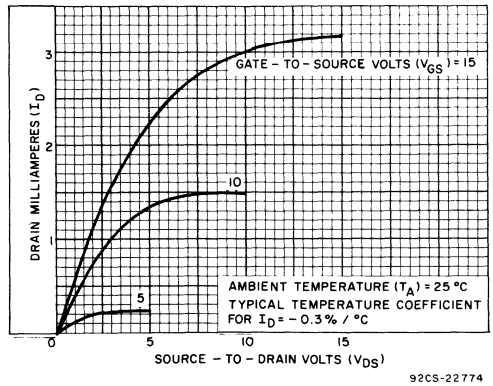


Fig. 11– Minimum n-channel drain characteristics – CD4012A.

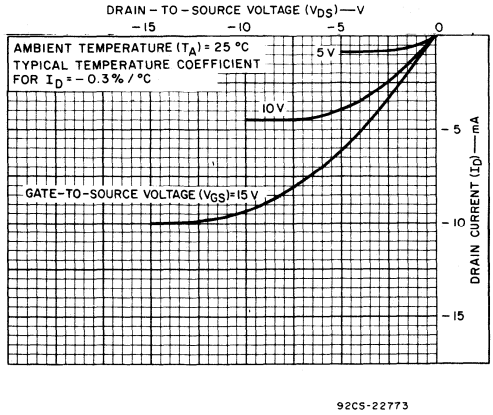


Fig. 12– Minimum p-channel drain characteristics.

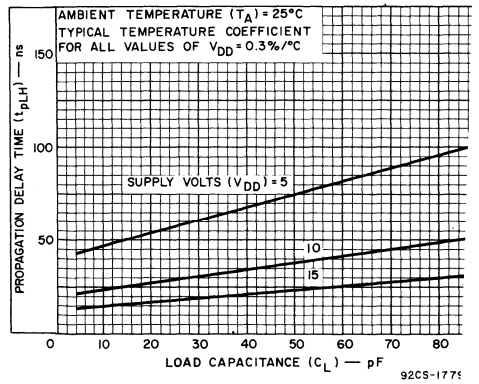


Fig. 13– Typical low-to-high level propagation delay time vs. C_L.

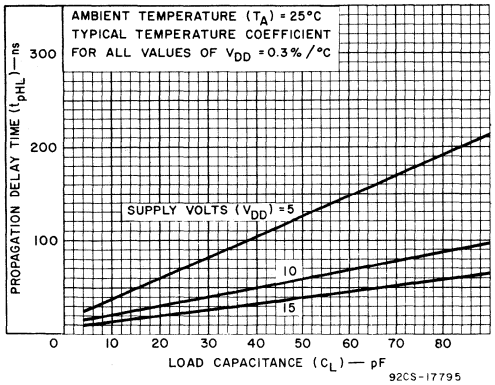


Fig. 14— Typical high-to-low level propagation delay time vs. C_L — CD4011A and CD4023A.

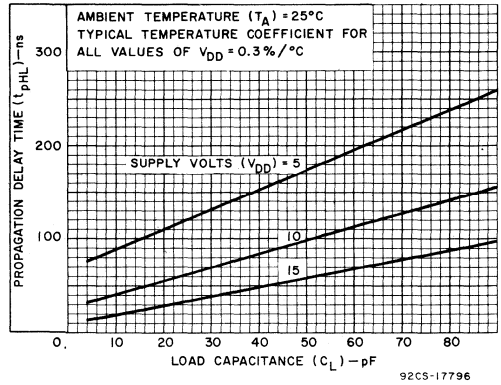


Fig. 15— Typical high-to-low level propagation delay time vs. C_L — CD4012A.

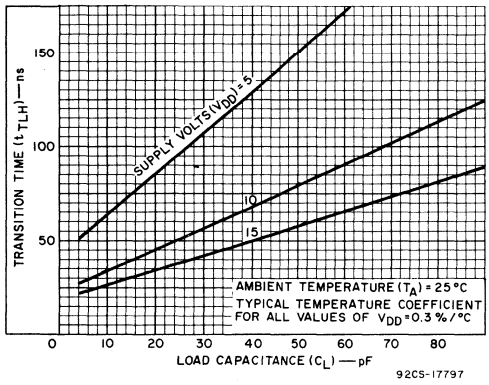


Fig. 16— Typical low-to-high transition time vs. C_L.

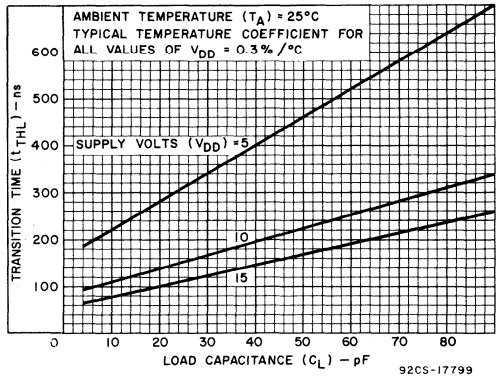


Fig. 17— Typical high-to-low level transition time vs. C_L — CD4011A and CD4023A.

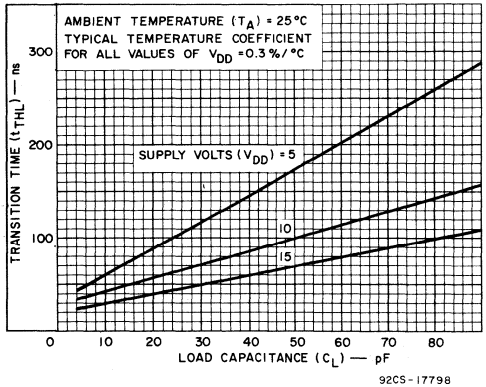


Fig. 18— Typical high-to-low level transition time vs. C_L — CD4012A.

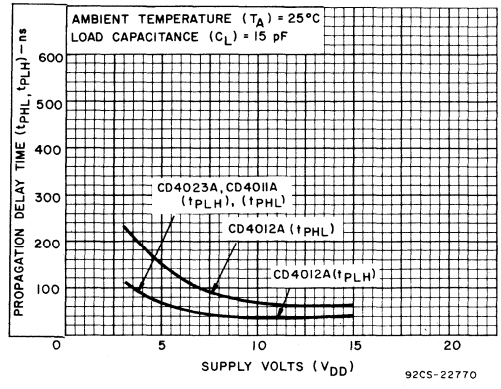


Fig. 19— Minimum propagation delay time vs. V_{DD}.

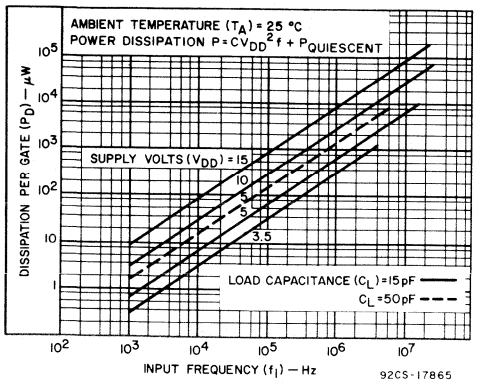
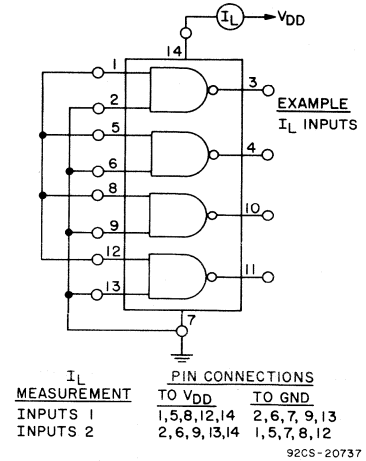


Fig. 20– Typical dissipation characteristics.



I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	1,5,8,12,14	2,6,7, 9,13
INPUTS 2	2,6,9,13,14	1,5,7,8,12

Fig. 21– Quiescent device current test circuit for CD4011A.

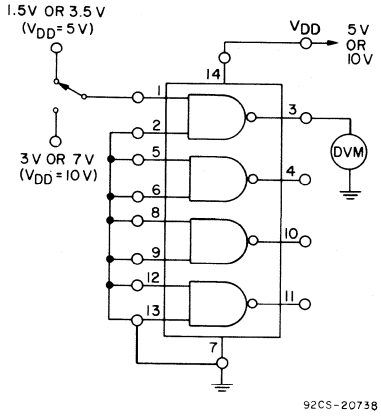
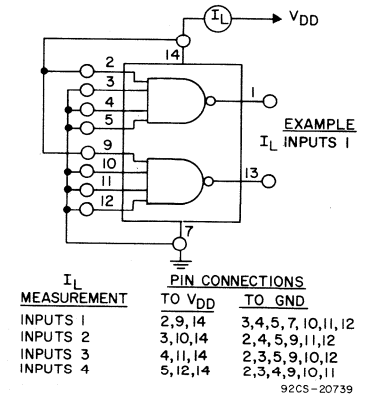


Fig. 22– Noise-immunity test circuit for CD4011A.



I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	2,9,14	3,4,5,7,10,11,12
INPUTS 2	3,10,14	2,4,5,9,11,12
INPUTS 3	4,11,14	2,3,5,9,10,12
INPUTS 4	5,12,14	2,3,4,9,10,11

Fig. 23– Quiescent device current test circuit for CD4012A.

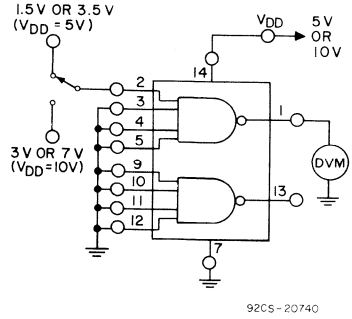
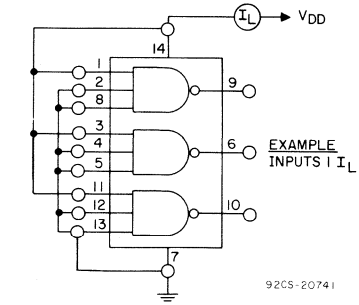


Fig. 24– Noise-immunity test circuit for CD4012A.



I_L MEASUREMENT	PIN CONNECTIONS TO V_{DD}	TO GND
INPUTS 1	1,3,11,14	2,4,5,7,8,12,13
INPUTS 2	2,4,12,14	1,3,5,7,8,11,13
INPUTS 3	8,5,13,14	1,2,3,4,7,11,12

Fig. 25– Quiescent device current test circuit for CD4023A.

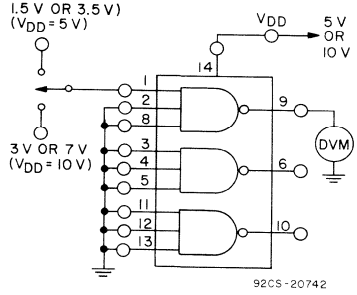


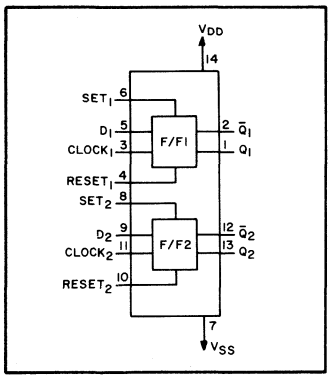
Fig. 26– Noise-immunity test circuit for CD4023A.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4013A/...



High-Reliability Dual "D"-Type Flip-Flop With Set-Reset Capability

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Static flip-flop operation . . . retains state indefinitely with clock level either "high" or "low"**
- **Medium speed operation . . . 10 MHz (typ.) clock toggle rate at $V_{DD} - V_{SS} = 10$ V**
- **Low "high"- and "low"-output impedance . . . 400 Ω and 200 Ω, respectively, at $V_{DD} - V_{SS} = 10$ V**

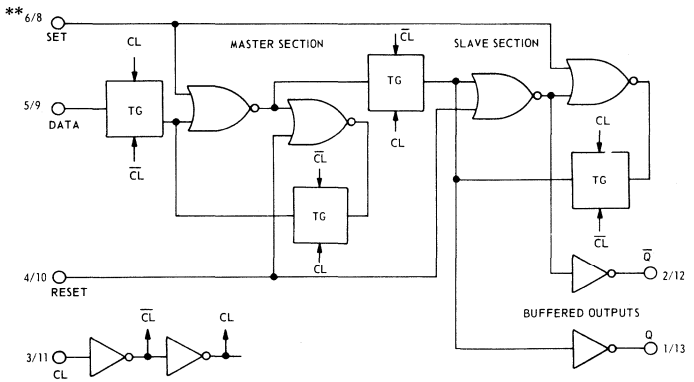
Applications:

- **Register, counters, control circuits**

RCA CD4013A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. CD4013A types consist of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\bar{Q}$" outputs. These devices can be used for shift register applications, and, by connecting "$\bar{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the "Q" output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

This device is electrically and mechanically identical with standard COS/MOS CD4013A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4013A	MIL-M-38510/05101



TRUTH TABLE

CL▲	D	R	S	Q	$\bar{Q}$	
⌒	0	0	0	0	1	
⌒	1	0	0	1	0	
⌣	X	0	0	Q	$\bar{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

▲ = LEVEL CHANGE

X = DON'T CARE CASE

** = FF1/FF2 TERMINAL ASSIGNMENTS

92SS-4386

TERMINAL 14 = V_{DD}
TERMINAL 7 = GND

Fig. 1— Logic diagram and truth table (one of two identical flip-flops).

The packaged types in the CD4013A "Slash" (/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the chart below.

The CD4013A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4013AD, CD4013AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4013AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4013AD/1N

CD4013A, D, /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4013AH/N

CD4013A, H, /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

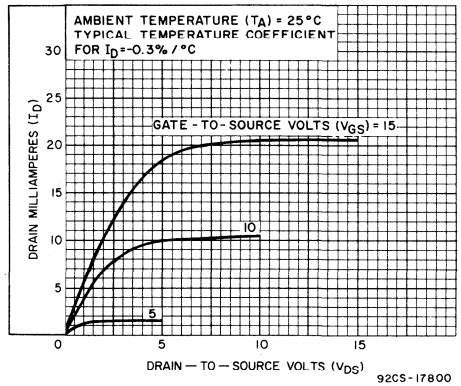


Fig. 2— Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4013AD,CD4013AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	—	—	1	—	0.005	1	—	—	60	μA	10	1
			10	—	—	2•	—	0.005	2•	—	—	40•			
Quiescent Device Dissipation/Package	P_D		5	—	—	5	—	0.025	5	—	—	300	μW	6	—
			10	—	—	20	—	0.05	20	—	—	400			
Output Voltage Low-Level	V_{OL}		3			0.55•	—	—	0.5•			—	V	—	1
			5	—	—	0.01	—	0	0.01	—	—	0.05			
			10	—	—	0.01	—	0	0.01	—	—	0.05			
			15	—	—	—	—	—	0.5•	—	—	0.55•			
High-Level	V_{OH}		3	2.25•	—	—	2.3•	—	—	—	—	—	V	—	1
			5	4.99	—	—	4.99	5	—	4.95	—	—			
			10	9.99	—	—	9.99	10	—	9.95	—	—			
			15	—	—	—	14.5•	—	—	14.45•	—	—			
Threshold Voltage: N-Channel	$V_{TH}N$	I_D = 20 μA		0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	—	2
P-Channel	$V_{TH}P$	I_D = 20 μA		0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity (All Inputs) *For Definition, See Appendix*	V_{NL}	0.8	5	1.5	—	—	1.5•	2.25	—	1.4	—	—	V	11	1
		1	10	3•			3•	4.5		2.9•	—	—			
	V_{NH}	4.2	5	1.4	—	—	1.5•	2.25	—	1.5	—	—	V		
		9	10	2.9•	—	—	3•	4.5	—	3•	—	—			
Output Drive Current: N-Channel	I_DN	0.5	5	0.65	—	—	0.5•	1	—	0.35	—	—	mA	2, 4	2
		0.5	10	1.25	—		1•	2.5	—	0.75	—	—			
P-Channel	I_DP	4.5	5	−0.31	—	—	−0.25•	−0.5	—	−0.175	—	—	mA	3, 5	2
		9.5	10	−0.8	—	—	−0.65•	−1.3	—	−0.45	—	—			
Diode Test, 100 μA Test Pin	V_{DF}			—	—	1.5•	—	—	1.5•	—	—	1.5•	V	—	3
Input Current	I_I			—	—	—	—	10	—	—	—	—	pA	—	—

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

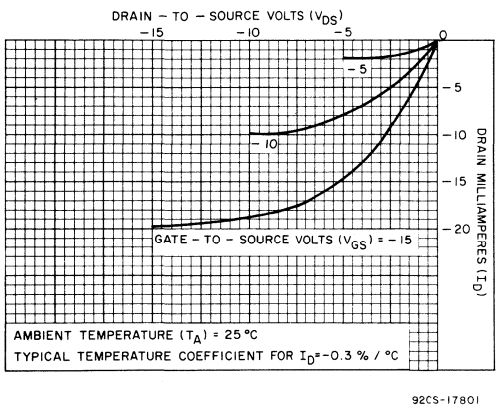


Fig. 3— Typical p-channel drain characteristics.

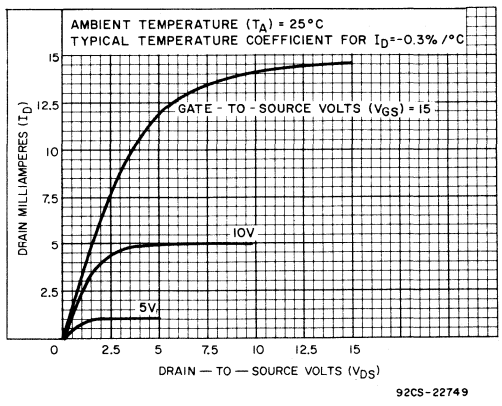


Fig. 4— Minimum n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL (See Appendix for Waveforms)

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			CD4013AD, CD4013AK					
		V_{DD} (Volts)	Min.	Typ.	Max.			
CLOCKED OPERATION								
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	150	300	ns	8	1
		10	–	75	110●			
Transition Time	t_{THL}, t_{TLH}	5	–	75	125	ns	9	–
		10	–	50	70			
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	125	200	ns	–	–
		10	–	50	80			
Clock Rise & Fall Time	*t_rCL, t_fCL	5	–	–	15	μs	–	1
		10	–	–	5●			
Set-Up Time		5	–	20	40	ns	–	–
		10	–	10	20			
Maximum Clock Frequency	f_{CL}	5	2.5	4	–	MHz	7	1
		10	7●	10	–			
Input Capacitance	C_I	Any Input	–	5	–	pF	–	–
SET & RESET OPERATION								
Propagation Delay Time:	$t_{PHL(R)}$, $t_{PLH(R)}$	5	–	175	300	ns	–	–
		10	–	75	110			
Minimum Set and Reset Pulse Widths	$t_{WH(S)}$, $t_{WH(R)}$	5	–	125	250	ns	–	–
		10	–	50	100			

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

* If more than one unit is cascaded in a parallel clocked operation, t_fCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

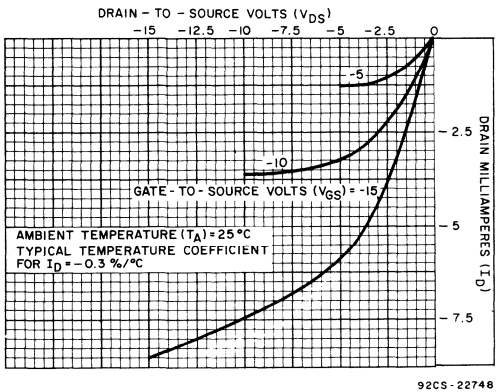


Fig. 5– Minimum p-channel drain characteristics.

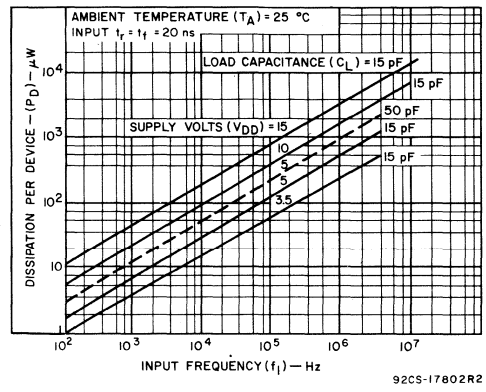


Fig. 6– Typical dissipation characteristics.

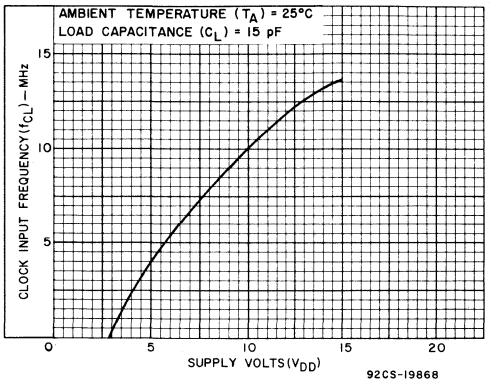


Fig. 7– Typical clock frequency vs. V_{DD}.

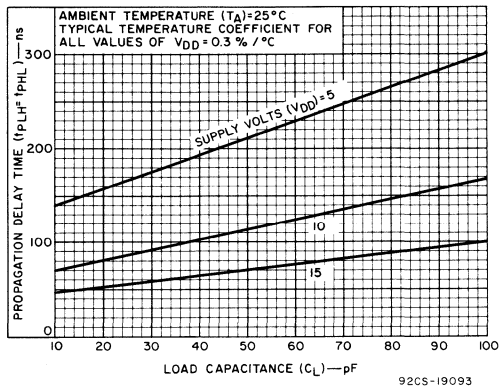


Fig. 8– Typical propagation delay time vs. C_L.

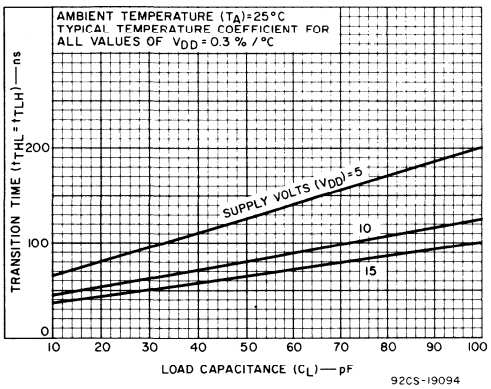
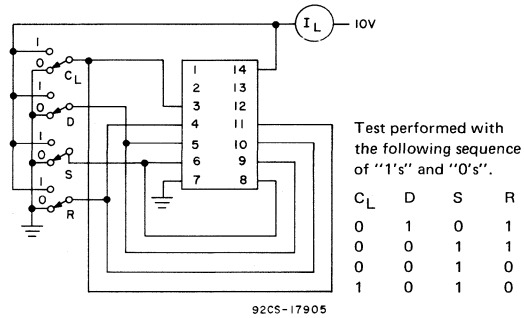


Fig. 9– Typical transition time vs. C_L.



Test performed with the following sequence of "1's" and "0's".

C_L	D	S	R
0	1	0	1
0	0	1	1
0	0	1	0
1	0	1	0

Fig. 10– Quiescent device current test circuit.

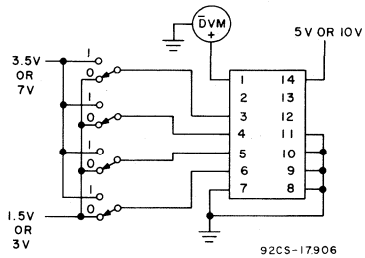


Fig. 11–Noise immunity test circuit.

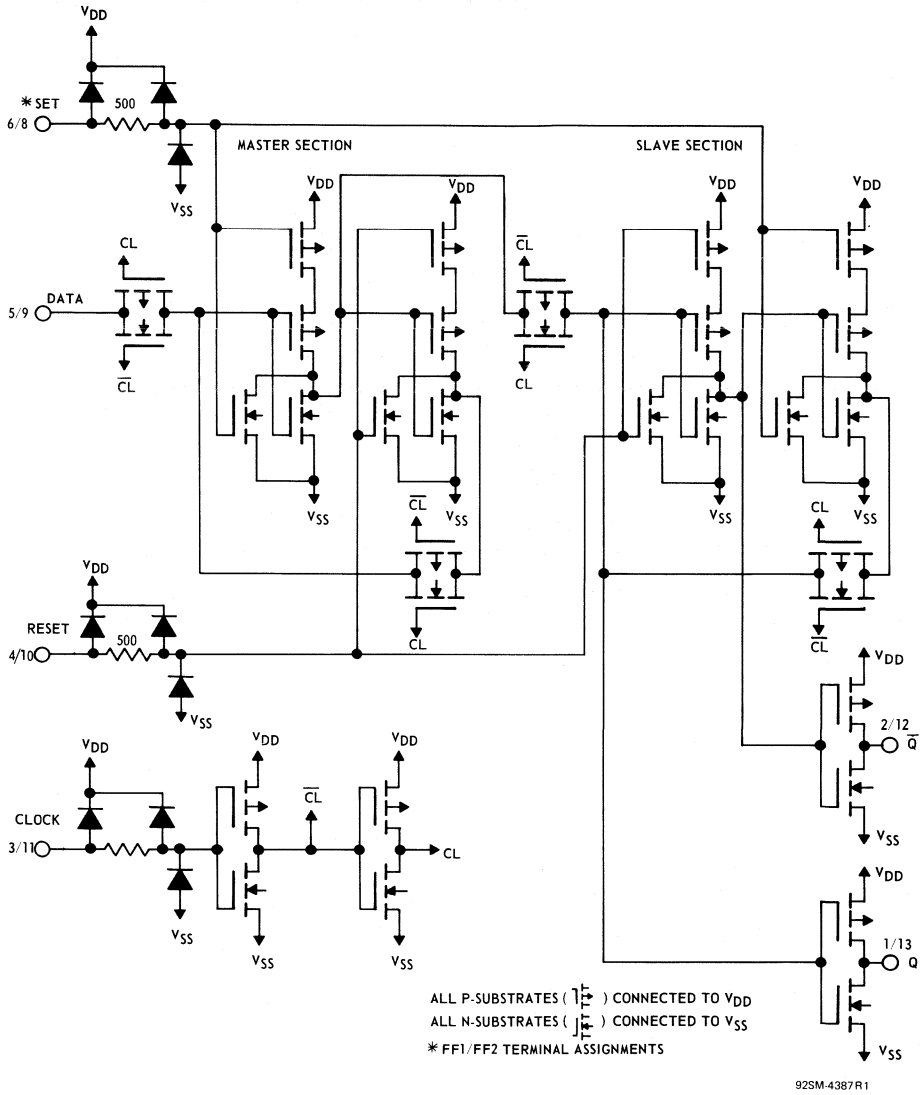


Fig. 12– Schematic diagram (one of two identical flip-flops).

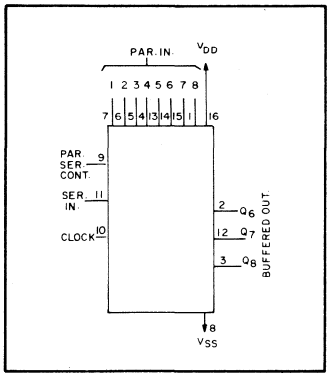
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4014A/...



High-Reliability COS/MOS 8-Stage Static Shift Register

Synchronous Parallel or Serial Input/Serial Output

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation. . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10 V**
- **Fully static operation**
- **MSI complexity on a single chip. . . . . 8 master-slave flip-flops plus output buffering and control gating**

Applications:

- **Synchronous parallel input/serial output data queueing**
- **Parallel to serial data conversion**
- **General purpose register**

RCA CD4014A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4014A types are 8-stage parallel-input/serial output registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7.

Parallel as well as serial entry is made into the register synchronous with the positive clock line transition and under control of the Parallel/Serial Control input. When the Parallel/Serial Control input is "low", data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the Parallel/Serial Control input is "high", data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. Register expansion using multiple CD4014A packages is permitted.

These types are electrically and mechanically identical to standard COS/MOS CD4014A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4014A	MIL-M-38510/05702

The packaged types in the CD4014A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1, /2, /3, /4 --- which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels --- /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the following page.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

The CD4014A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4014AK, CD4014AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4014AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4014AD/1N

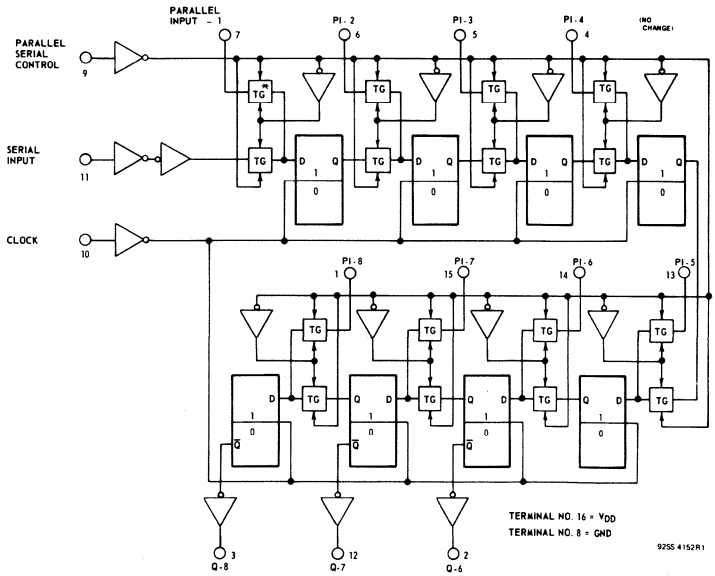
CD4014A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4014AH/N

CD4014A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R



CL ▲	SER IN	PAR/SER CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n
⌒	X	1	0	0	0	0
⌒	X	1	1	0	1	0
⌒	X	1	0	1	0	1
⌒	X	1	1	1	1	1
⌒	0	0	X	X	0	Q_n-1
⌒	1	0	X	X	1	Q_n-1
⌒	X	X	X	X	Q_1	Q_n

X = DON'T CARE ▲ = LEVEL CHANGE

Fig. 1–Logic block diagram and truth table.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4014AD, CD4014AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.5	5	–	–	300	μA	6	1
			10	–	–	10●	–	1	10●	–	–	300●			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	2.5	25	–	–	1500	μW	–	–
			10	–	–	100	–	10	100	–	–	2000			
Output Voltage Low Level	V_{OL}		3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	14.45	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D = -20\,\mu A$		−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	V_{THP}	$I_D = 20\,\mu A$		0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}		0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	7	1
			0.5	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix SSD-207	V_{NH}		4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
			9.5	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_DN		0.5	5	0.15	–	–	0.15●	0.3	–	0.085	–	–	mA	–	2
			0.5	10	0.31	–	–	0.25●	0.5	–	0.175	–	–			
P-Channel	I_DP		4.5	5	−0.1	–	–	−0.08●	−0.16	–	−0.055	–	–	mA	–	2
			9.5	10	−0.25	–	–	−0.2●	−0.44	–	−0.14	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

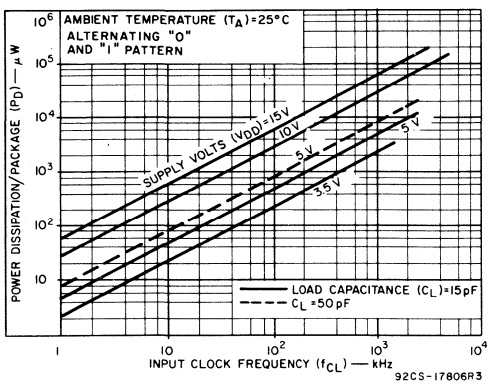


Fig. 2—Typ. dissipation characteristics.

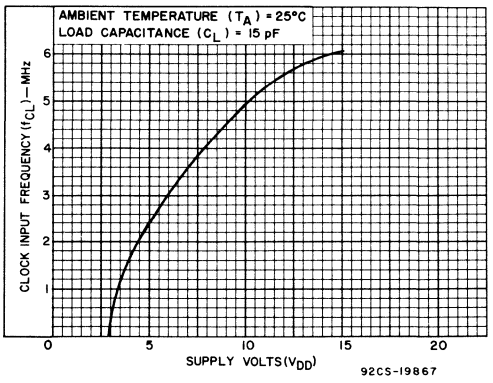


Fig. 3—Typ. clock frequency vs. V_{DD}

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25^\circ C$, $C_L = 15$ pF, and input rise and fall times = 20 ns except t_rCL, t_fCL Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/^\circ C$ (See Appendix for Waveforms)*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			CD4014AD, CD4014AK					
		V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	300	750	ns	4	1
		10	–	100	225●			
Transition Time	t_{THL}, t_{TLH}	5	–	150	300	ns	5	–
		10	–	75	125			
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	200	500	ns	–	–
		10	–	100	175			
Clock Rise & Fall Time	t_rCL, t_fCL*	5	–	–	15	μs	–	1
		10	–	–	15●			
Set-Up Time		5	–	100	350	ns	–	–
		10	–	50	80			
Maximum Clock Frequency	f_{CL}	5	1	2.5	–	MHz		1
		10	3●	5	–			
Input Capacitance	C_I	Any Input	–	5	–	pF	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

* If more than one unit is cascaded t_fCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

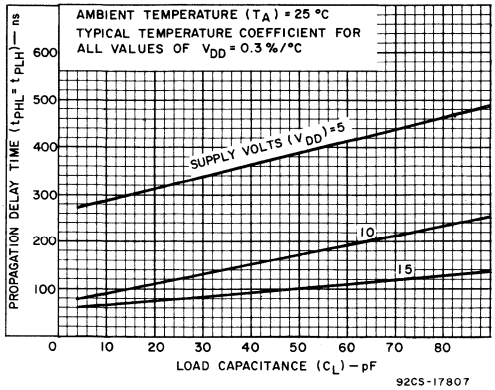


Fig. 4—Typ. propagation delay time vs. C_L.

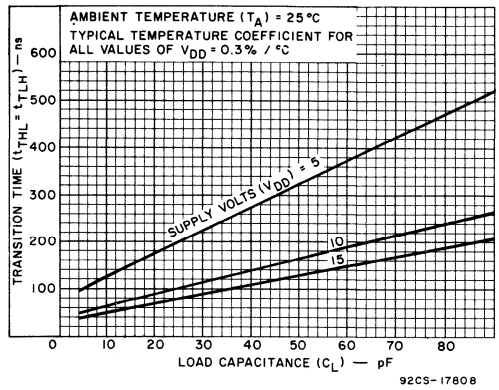
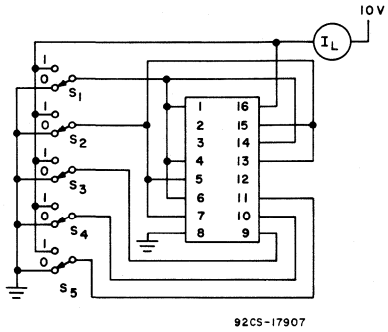


Fig. 5—Typ. transition time vs. C_L.



Test performed with the following sequence of "1's" and "0's"

	S_1	S_2	S_3	S_4	S_5
Don't Test	0	1	1	0	0
Test	0	1	1	1	0
Test	1	0	0	0	0
Test	1	0	1	1	1
Test	1	0	0	0	1

Fig. 6—Quiescent device current test circuit.

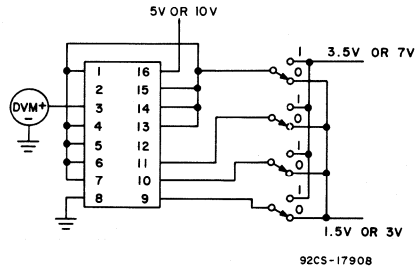


Fig. 7—Noise immunity test circuit.

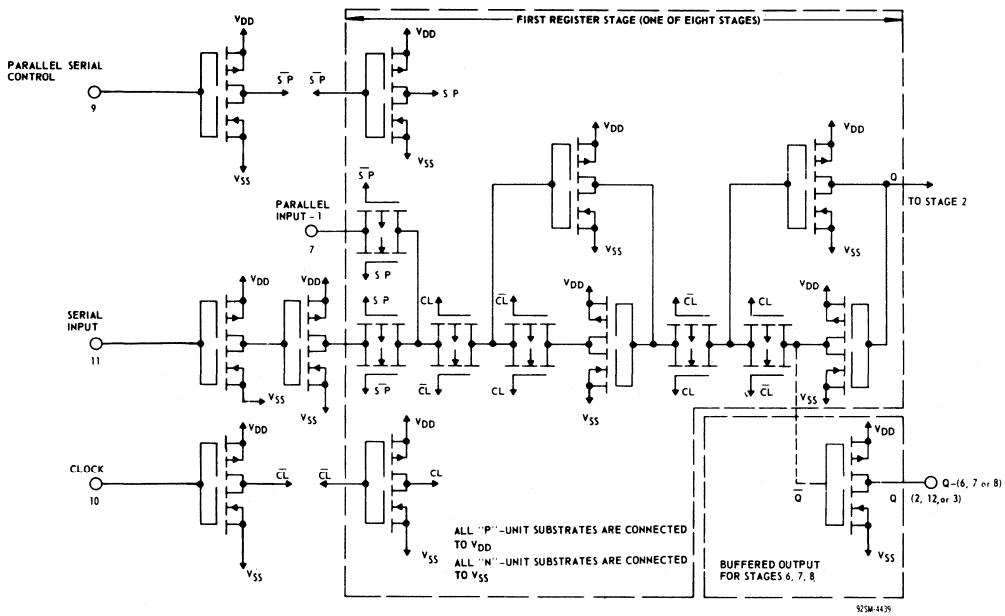


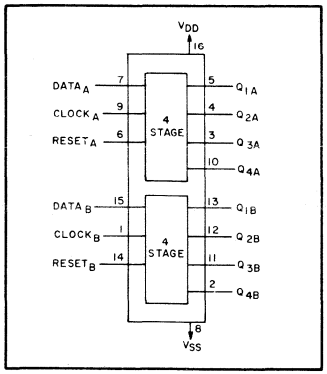
Fig. 8—Schematic diagram — CD4014A.

RCA Solid State Division

Digital Integrated Circuits
Monolithic Silicon

High-Reliability Slash(/) Series

CD4015A/...



High-Reliability COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- **Medium speed operation. . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10 V**
- **Fully static operation**
- **MSI complexity on a single chip. . . . . 8 master-slave flip-flops plus output buffering**

Applications

- **Serial-input/parallel-output data queueing**
- **Serial to parallel data conversion**
- **General purpose register**

RCA CD4015A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. CD4015A types consist of two identical, independent, 4-stage serial input/parallel-output registers. Each register has independent "Clock" and "Reset" inputs as well as a single serial "Data" input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015A package, or to more than 8 stages using additional CD4015A packages is possible.

These devices are electrically and mechanically identical with standard COS/MOS CD4015A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4015A	MIL-M-38510/05703

The packaged types in the CD4015A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1, /2, /3, /4 --- which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels --- /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the following page.

The CD4015A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4015AD, CD4015AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4015AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4015AD/1N

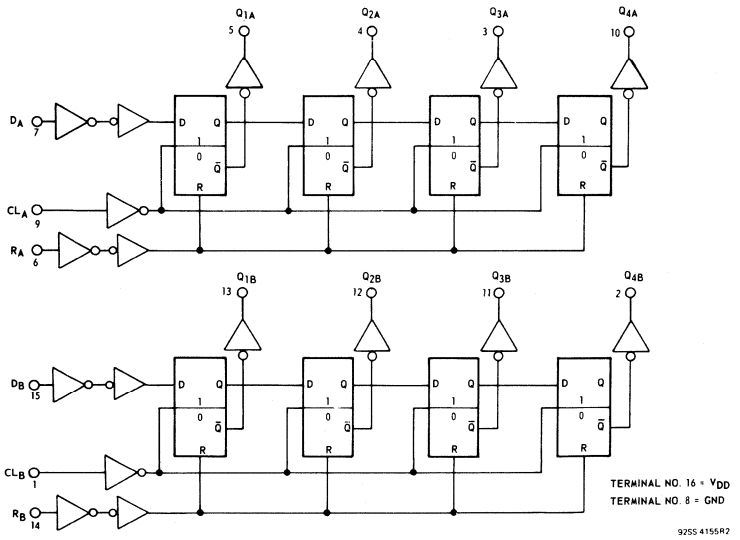
CD4015A D /1N

	Package Suffix Letter	Screening Level
Type Designation	D = Dual in Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4015AH/N

CD4015A H /N

	Package Suffix Letter	Screening Level
Type Designation	H = Chip Version	/N /R



TRUTH TABLE

CL▲	D	R	Q_1	Q_n	
⌐⌐	0	0	0	Q_{n-1}	
⌐⌐	1	0	1	Q_{n-1}	
⌐_	X	0	Q_1	Q_n	(NO CHANGE)
X	X	1	0	0	

▲ = LEVEL CHANGE
X = DON'T CARE CASE

Fig. 1—Logic diagram and truth table.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs ... $V_{SS} \leq V_I \leq V_{DD}$)*
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4015AD, CD4015AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.5	5	–	–	300	μA	6	1
			10	–	–	0.5●	–	1	0.5●	–	–	10●			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	2.5	2.5	–	–	1500	μW	–	–
			10	–	–	5	–	10	5	–	–	100			
Output Voltage Low-Level	V_{OL}		3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$		0.3●	−1.7	−3●	−0.7●	−1.5	−3●	−0.7●	−1.3	−3●	V	–	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$		0.3●	1.7	3●	0.7●	1.5	3●	0.7●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}	0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	7	1
		1	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix SSD-207	V_{NH}	4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		9	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	$I_D N$	0.5	5	0.15	–	–	0.125●	0.3	–	0.085	–	–	mA	–	2
		0.5	10	0.31	–	–	0.25●	0.5	–	0.175	–	–			
P-Channel	$I_D P$	4.5	5	−0.1	–	–	−0.08●	−0.16	–	−0.055	–	–	mA	–	2
		9.5	10	−0.25	–	–	−0.2●	−0.44	–	−0.14	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

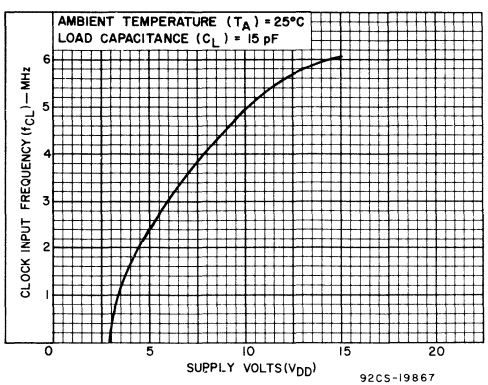


Fig. 2—Typ. clock frequency vs. V_{DD}.

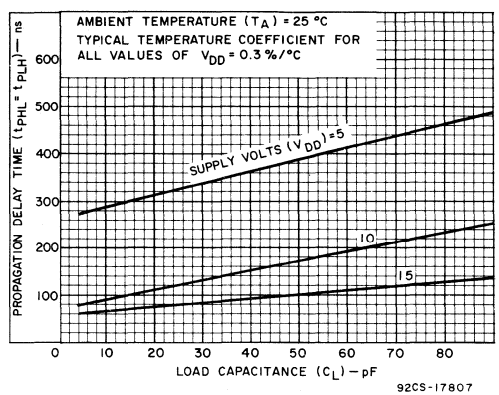


Fig. 3—Typ. propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C and C_L = 15 pF*

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4015AD, CD4015AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
CLOCKED OPERATION								
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	300	750	ns	3	1
		10	–	100	225●			
Transition Time	t_{THL}, t_{TLH}	5	–	150	300	ns	4	–
		10	–	75	125			
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	200	500	ns	–	–
		10	–	100	175			
Clock Rise & Fall Time	*t_{rCL}, t_{fCL}	5	–	–	15	μs	–	1
		10	–	–	15●			
Set-Up Time		5	–	100	350	ns	–	–
		10	–	50	80			
Maximum Clock Frequency	f_{CL}	5	1	2.5	–	MHz	–	1
		10	3●	5	–			
Input Capacitance	C_I		–	5	–	pF	–	–
RESET OPERATION								
Propagation Delay Time	$t_{PHL(R)}$	5	–	300	750	ns	–	–
		10	–	100	225			
Minimum Set and Reset Pulse Widths	$t_{WH(R)}$	5	–	200	500	ns	–	–
		10	–	100	175			

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1. Test is a one input one output only.

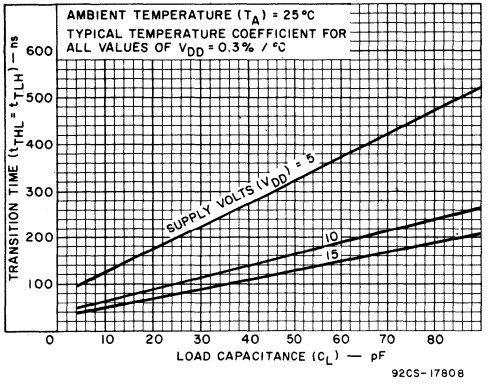


Fig. 4—Typ. transition time vs. C_L.

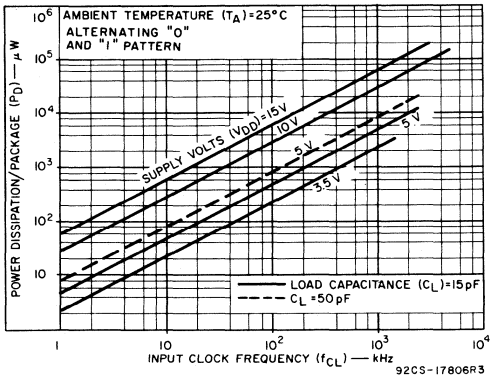
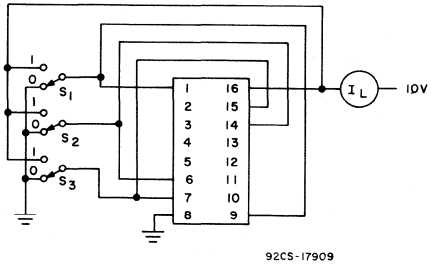


Fig. 5—Typ. dissipation characteristics.



Test performed with the following sequence of "1's" and "0's"

	S_1	S_2	S_3
Test	0	1	0
Don't Test	0	0	1
Don't Test	1	0	1
Don't Test	0	0	0
Don't Test	1	0	0
Don't Test	0	0	1
Test	1	0	1
Don't Test	0	0	0
Test	1	0	0

Fig. 6—Quiescent device current test circuit.

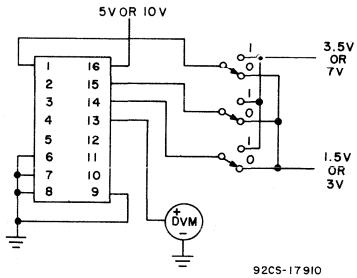
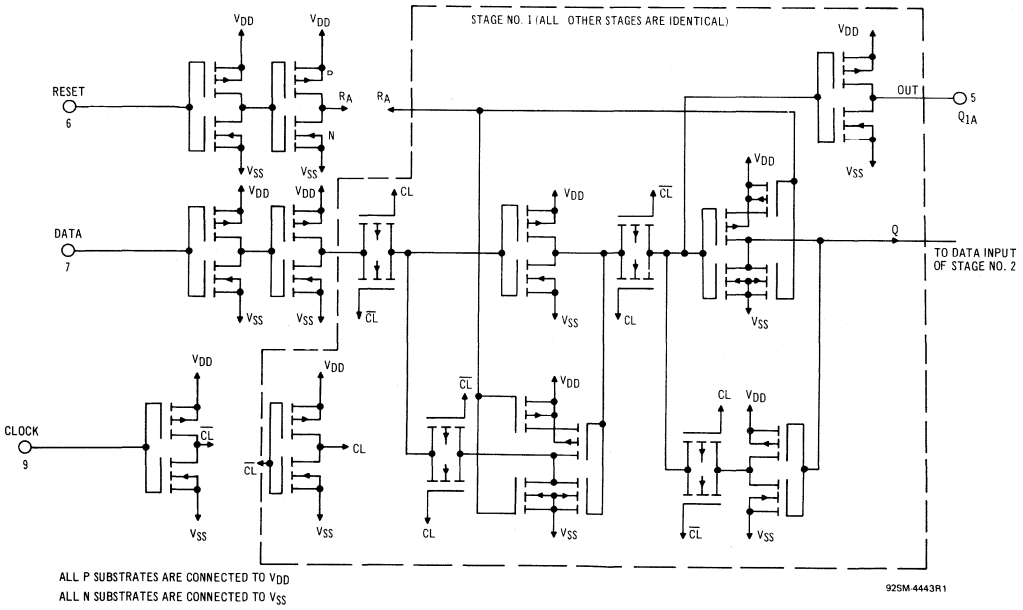


Fig. 7—Noise immunity test circuit.



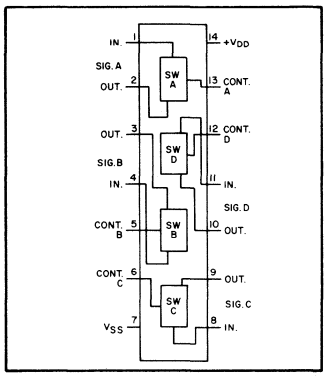
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4016A/...



High-Reliability COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- **Wide range of digital and analog signal levels — Digital or analog signal to 15 V peak Analog signal ± 7.5 V peak**
- **Low "ON" resistance— 300 Ω typ. over 15 V_{p-p} signal input range, for $V_{DD} - V_{SS}$ = 15 V**
- **Matched switch characteristics — 40 Ω typ. difference between R_{ON} values at a fixed bias point over 15 V_{p-p} signal input range $V_{DD} - V_{SS}$ = 15 V**
- **High "On/Off" output voltage ratio — 65 dB type@ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity — < 0.5% distortion typ. @ f_{is} = 1kHz, $V_{is} = 5V_{p-p}$, $V_{DD}-V_{SS} \geq 10$ V, R_L = 10 kΩ.**

RCA CD4016A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. These devices are electrically and mechanically identical with standard COS/MOS CD4016A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4016A	MIL-M-38510/05801

The packaged types in the CD4016A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1, /2, /3, and /4 --- which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels --- /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

Applications

- **Analog signal switching/multiplexing**
  - **Signal gating**
  - **Squelch control**
  - **Chopper**
  - **Modulator**
  - **Demodulator**
  - **Commutating switch**
- **Digital signal switching/Multiplexing**
- **COS/MOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**
- **Extremely low "OFF" switch leakage resulting in very low offset current and high effective "OFF" resistance — 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25° C**
- **Extremely high control input impedance (control circuit isolated from signal circuit) — 10^{12} Ω typ.**
- **Low crosstalk between switches — −50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitances — Reduces output signal transients**
- **Transmits frequencies up to 10 MHz**

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see tables below.

The CD4016A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4016AK, CD4016AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4016AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4016AD/1N

CD4016A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4016AH/N

CD4016A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

NOTE: All switch P-channel substrates are internally connected to terminal No. 14.
All switch N-channel substrates are internally connected to terminal No. 7.

NORMAL OPERATION:

Control-Line Biasing
Switch "ON": V_C "1" = V_{DD}
Switch "OFF": V_C "0" = V_{SS}

SIGNAL-LEVEL RANGE:
$V_{SS} \leq V_{is} \leq V_{DD}$

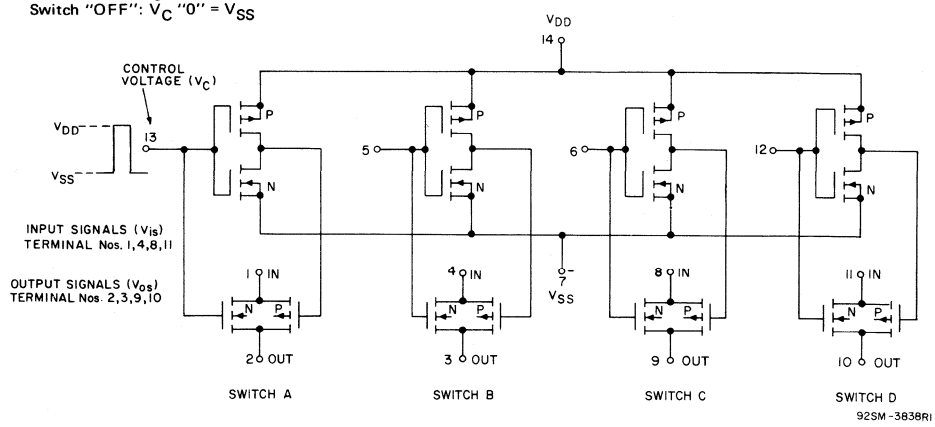


Fig. 1–Schematic diagram.

ELECTRICAL CHARACTERISTICS *(All inputs . . . . . $V_{SS} \leq V_I \leq V_{DD}$) (Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . . . . .3 to 15V)*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS CD4016AD, CD4016AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CURVES & WAVE FORMS Fig. No.	NOTES
Quiescent Dissipation per Package All Switches "OFF"	P_D	V_{DD} 14 +10; V_{SS} 7 GND	–	–	5	–	0.1	5	–	–	300	μW	–	1
Quiescent Device Current	I_L	V_C 5, 6, 12, 13 GND; V_{is} 1, 4, 8, 11 ≷ +10; V_{os} 2, 3, 9, 10 ≶ +10	–	–	0.5●	–	–	0.5●	–	–	10●			
Quiescent Dissipation per Package All Switches "ON"	P_D	V_{DD} 14 +10; V_{SS} 7 GND	–	–	5	–	0.1	5	–	–	300	μW	–	1
Quiescent Device Current	I_L	V_C 5, 6, 12, 13 +10; $V_{is}=V_{os}$ 1-4, 8-11 ≶ +10	–	–	0.5●	–	–	0.5●	–	–	10●			
Output Voltage Low-Level	V_{OL}	V_{DD} 3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
		V_{DD} 15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}	V_{DD} 3	2.25●	–	–	2.3●	–	–	–	–	–			
		V_{DD} 15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = −10 μA Terminal 13 = GND; V_{DD} = 5V, 10V	−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	20	2
P-Channel	$V_{TH}P$	I_{DS} = 10 μA Terminal 13 = GND; V_{DD} = 5V, 10V	0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●	V	–	2
Diode Test	V_{DF}	100 μA Test pin	–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
● SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})														
"ON" Resistance	R_{ON}	R_L = 10k Ω; V_C = V_{DD}, V_{SS}, V_{is}: +7.5V	–	120	360●	–	200	400●	–	300	600●	Ω	5	2
		+7.5V, −7.5V, −7.5V	–	120	360●	–	200	400●	–	300	600●	Ω	5	2
		±0.25V	–	130	775	–	280	850	–	470	1230			
		+5V, −5V, +5V	–	130	600●	–	250	660●	–	400	960●	Ω	6	2
		−5V	–	130	600●	–	250	660●	–	400	960●	Ω	6	2
		±0.25V	–	325	1870	–	580	2000	–	900	2600			
		+15V, +15V, 0V, +15V	–	120	360●	–	200	400●	–	300	600●	Ω	2	2
		+0.25V	–	120	360	–	200	400	–	300	600	Ω	2	2
		9.3V	–	150	775	–	300	850	–	490	1230			
		+10V, +10V, 0V, +10V	–	130	600●	–	250	660●	–	400	960●	Ω	3	2
		+0.25V	–	130	600	–	250	660	–	400	960	Ω	3	2
		5.6V	–	300	1870	–	560	2000	–	880	2600			
▲"ON" Resistance Between Any 2 of 4 Switches	▲R_{ON}	+7.5V, −7.5V, ±7.5V	–	–	–	–	10	–	–	–	–	Ω	–	–
		+5V, −5V, ±5V	–	–	–	–	15	–	–	–	–	Ω	–	–
Sine Wave Response (Distortion)		R_L = 10k Ω; f_{is} = 1kHz; +5V, −5V, 5V (p-p)	–	–	–	–	0.4	–	–	–	–	%	13	–
Input or Output Leakage—Switch "OFF" (Effective "OFF" Resistance)		V_{DD} +7.5V, V_C −7.5V, V_{is} +7.5V	–	–	–	–	±100	–	–	–	–	nA	19	1
		V_{DD} +7.5V, V_C −7.5V, V_{is} −7.5V	–	–	–	–	±100	–	–	–	–	nA	19	1
		V_{DD} +5V, V_C −5V, V_{is} +5V	–	–	–	–	100	500	–	–	–	nA	19	1
		V_{DD} +5V, V_C −5V, V_{is} −5V	–	–	–	–	100	500	–	–	–	nA	19	1
Frequency Response—Switch "ON" (Sine Wave Input)		R_L = 1kΩ; V_{is} = 5V (p-p); V_C = V_{DD} = −5V V_{SS} = −5V; $20\ Log_{10}\frac{V_{os}}{V_{is}}$ = −3dB	–	–	–	–	40	–	–	–	–	MHz	11	–
Feedthrough Switch "OFF"		V_{is} = 5V (p-p); V_{DD} = +5V, V_C = V_{SS} = −5V; $20\ Log_{10}\frac{V_{os}}{V_{is}}$ = −50dB	–	–	–	–	1.25	–	–	–	–	MHz	9	–
Crosstalk Between Any 2 of the 4 Switches (Frequency at −50dB)		R_L = 1kΩ; $V_{is}(A)$ = 5V (p-p); $V_C(A)$ V_{DD} = +5V; $V_C(B)$ = V_{SS} = −5V; $20\ Log_{10}\frac{V_{os}(B)}{V_{is}(A)}$ = −50dB	–	–	–	–	0.9	–	–	–	–	MHz	10	–
Capacitance Input	C_{IS}	V_{DD} = +5V, V_C = V_{SS} = −5V	–	–	–	–	4	–	–	–	–	pF	25	–
Output	C_{OS}		–	–	–	–	4	–	–	–	–	pF	25	–
Feedthrough	C_{IOS}		–	–	–	–	0.2	–	–	–	–	pF	25	–
Propagation Delay Signal Input to Signal Output	t_{pd}	V_C = V_{DD} = +10V, V_{SS} = GND, C_L = 15pF; V_{is} = 10V (square wave); t_r = t_f = 20 ns (input signal)	–	–	–	–	10	25●	–	–	–	ns	21	2

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or a one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

•±10 x 10^{-3} ▲Symmetrical about 0 volts

ELECTRICAL CHARACTERISTICS *(All Inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)*

(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4016AD, CD4016AK –55°C Min.	–55°C Typ.	–55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CURVES & WAVE-FORMS Fig. No.	NOTES
CONTROL (V_C)															
Switch Threshold Voltage	V_{TH}^N		$V_{DD} - V_{SS}$ = 15V, 10V, 5V, I_{IS} = 10μA	0.7	–	2.9	0.5	1.5	2.7	0.2	–	2.4		20	–
Input Current	I_C	$V_{IS} \leq V_{DD}$	$V_{DD} - V_{SS}$ = 10V, $V_C \leq V_{DD} - V_{SS}$	–	–	–	–	±10	–	–	–	–	pA	–	–
Noise Immunity (Control Inputs)	V_{NL}	V_{DD} = 10V		0.5●	–	–	0.7●	–	–	0.5●	–	–	V	–	1
For Definition, See Appendix SSD-207	V_{NH}			–	–	3●	–	–	2.7●	–	–	3●			
Average Input Capacitance	C_C			–	–	–	–	–5	–	–	–	–	pF	–	–
Crosstalk – Control Input to Signal Output		$V_{DD}-V_{SS}$ = 10V, V_C = 10V (square wave) $t_{rC} = t_{fC}$ = 20 ns	R_L = 10 kΩ	–	–	–	–	50	–	–	–	–	mV	22	–
Turn "ON" Propagation Delay	t_{pdC}		$V_{is} \leq$ 10V, C_L = 15 pF	–	–	–	–	20	50●	–	–	–	ns	23	2
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1kΩ, C_L = 15pF, V_C = 10V (square wave), $t_r = t_f$ = 20 ns		–	–	–	–	10	–	–	–	–	MHz	24	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is all inputs

TYPICAL "ON" RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS V_{DD} (V)	SUPPLY CONDITIONS V_{SS} (V)	LOAD CONDITIONS R_L = 1kΩ VALUE (Ω)	R_L = 1kΩ V_{is} (V)	R_L = 10kΩ VALUE (Ω)	R_L = 10kΩ V_{is} (V)	R_L = 100kΩ VALUE (Ω)	R_L = 100kΩ V_{is} (V)	TYPICAL CHARACTERISTIC CURVE Fig. No.
R_{ON}	+15	0	200	+15	200	+15	180	+15	2
			200	0	200	0	200	0	
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2	
R_{ON}	+10	0	290	+10	250	+10	240	+10	3
			290	0	250	0	300	0	
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5	
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5	4
			600	0	580	0	800	0	
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7	
R_{ON}	+7.5	–7.5	200	+7.5	200	+7.5	180	+7.5	5
			200	–7.5	200	–7.5	180	–7.5	
R_{ON}(max.)	+7.5	–7.5	290	±0.25	280	±25	400	±0.25	
R_{ON}	+ 5	– 5	260	+ 5	250	+ 5	240	+ 5	6
			310	– 5	250	– 5	240	– 5	
R_{ON}(max.)	+ 5	– 5	600	±0.25	580	±0.25	760	±0.25	
R_{ON}	+2.5	–2.5	590	+2.5	450	+2.5	490	+2.5	7
			720	–2.5	520	–2.5	520	–2.5	
R_{ON}(max.)	+2.5	–2.5	232k	±0.25	300k	±0.25	870k	±0.25	

* Variation from a perfect switch; R_{ON} = 0Ω.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
$(V_{DD} - V_{SS})$	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} < V_I < V_{DD}$
Recommended	
DC Supply-Voltage $(V_{DD} - V_{SS})$	3 to 15 V
Recommended	
Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering)	
At distance 1/16" ± 1/32"	
(1.59 ± 0.79 mm) from case	
for 10 s max.	+265 °C

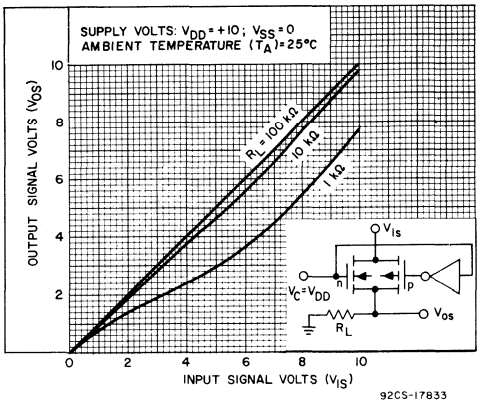


Fig. 3—Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +10V, V_{SS} = 0V.

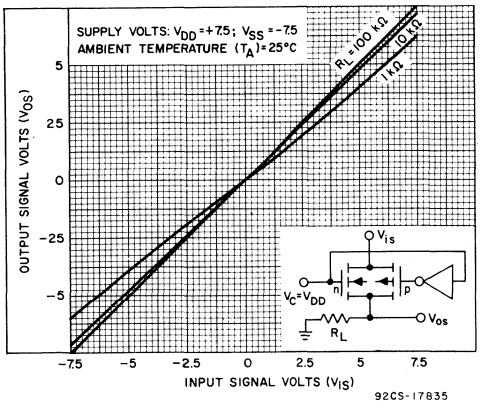


Fig. 5—Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +7.5V, V_{SS} = -7.5V.

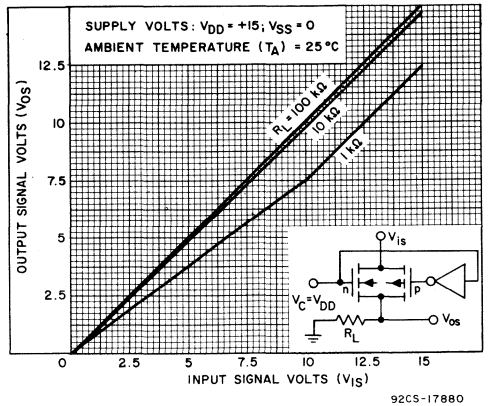


Fig. 2—Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +15V, V_{SS} = 0V.

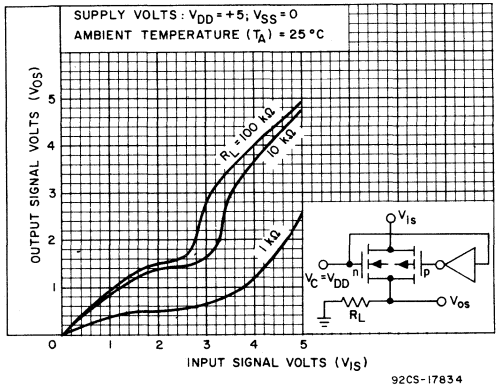


Fig. 4—Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5V, V_{SS} = 0V.

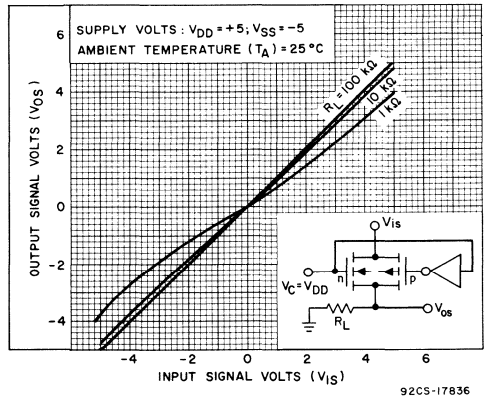


Fig. 6—Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5V, V_{SS} = -5V.

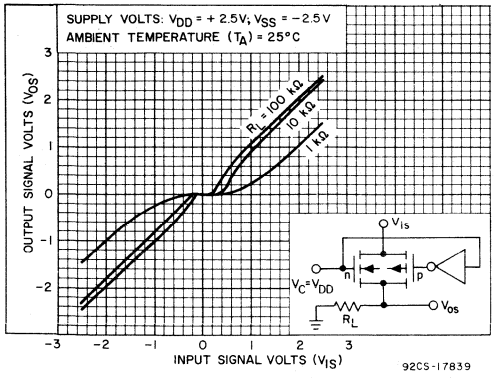


Fig. 7—Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +2.5V, V_{SS} = -2.5V.

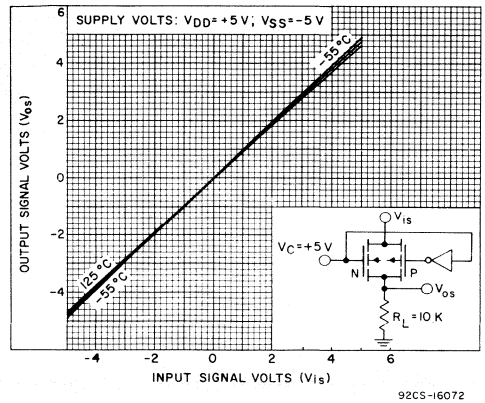


Fig. 8—Typ. "ON" characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5V, V_{SS} = -5V.

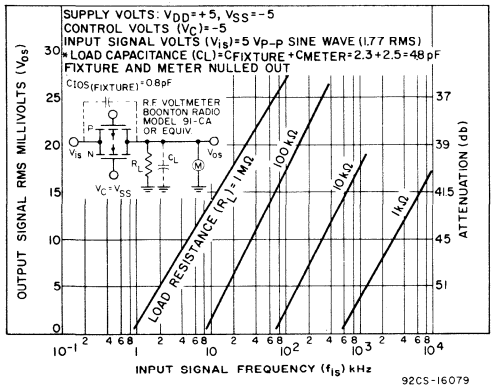


Fig. 9—Typ. feedthru vs. freq. — switch "OFF".

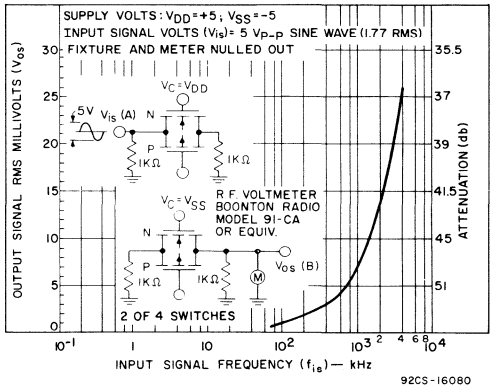


Fig. 10—Typ. crosstalk between switch circuits in the same package.

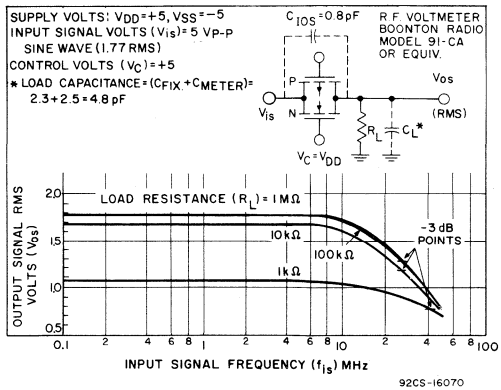
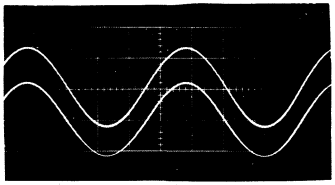
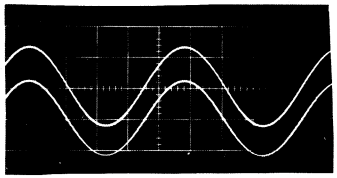


Fig. 11—Typ. switch frequency response —switch "ON".



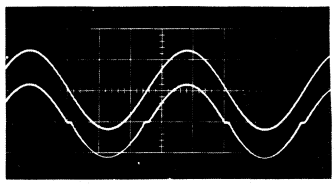
SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD} = V_C = +7.5V$, $V_{SS} = -7.5V$, $R_L = 10K\Omega$
$C_L = 15\ pF$
$f_{IS} = 1\ KHz$ $V_{IS} = 5V\ p\text{-}p$
DISTORTION = 0.2 %

Fig. 12—Typ. sine wave response of V_{DD} = +7.5V, V_{SS} = -7.5V.



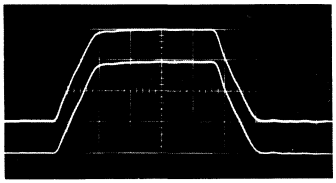
SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD} = V_C = +5\ V$, $V_{SS} = -5\ V$, $R_L = 10K\Omega$
$C_L = 15\ pF$
$f_{IS} = 1\ KHz$ $V_{IS} = 5\ V\ p\text{-}p$
DISTORTION = 0.4 %

Fig. 13—Typ. sine wave response of V_{DD} = +5V, V_{SS} = -5V.



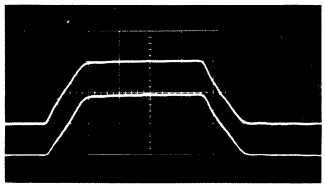
SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD} = V_C = +2.5V$, $V_{SS} = -2.5V$, $R_L = 10K\Omega$
$C_L = 15\ pF$
$f_{IS} = 1\ KHz$ $V_{IS} = 5V\ p\text{-}p$
DISTORTION = 3 %

Fig. 14—Typ. sine wave response of V_{DD} = +2.5V, V_{SS} = -2.5V.



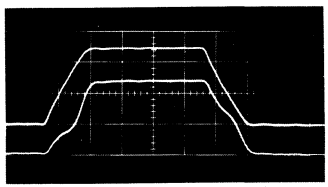
SCALE: X = 100 ns/DIV
Y = 5.0 V/DIV

Fig. 15—Typ. square wave response at $V_{DD} = V_C = +15V$, $V_{SS} = Gnd$.



SCALE: X = 100 ns/DIV
Y = 5.0 V/DIV

Fig. 16—Typ. square wave response at $V_{DD} = V_C = +10V$, $V_{SS} = Gnd$.



SCALE: X = 100 ns/DIV
Y = 2 V/DIV

Fig. 17—Typ. square wave response at $V_{DD} = V_C = +5V$, $V_{SS} = Gnd$.

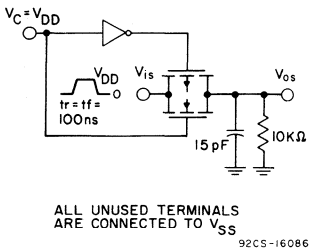


Fig. 18—Test circuit for square wave response.

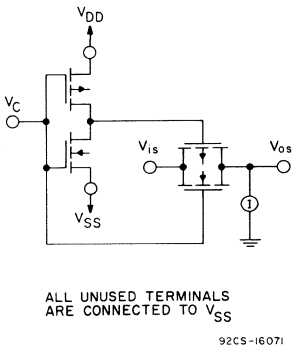


Fig. 19—"OFF" switch input or output leakage test circuit.

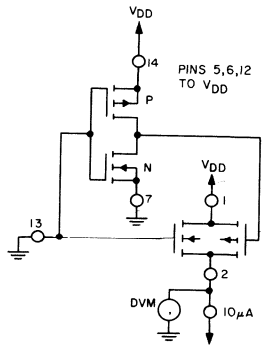


Fig. 20—Switch threshold voltage—n-channel test circuit.

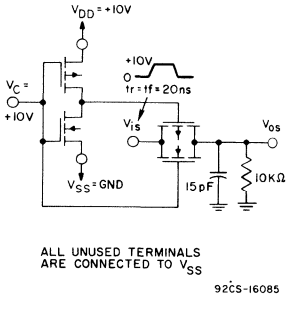
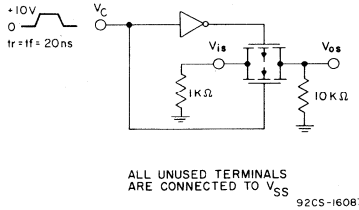


Fig. 21—Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).



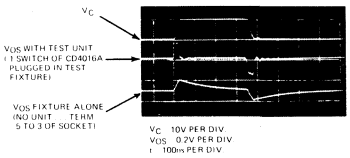


Fig. 22—Crosstalk-control input to signal output.

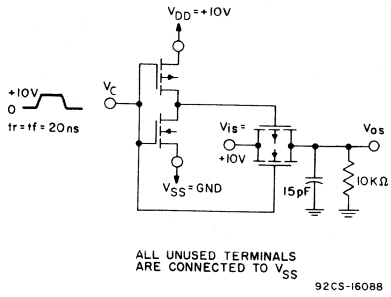


Fig. 23—Turn-on propagation delay control input.

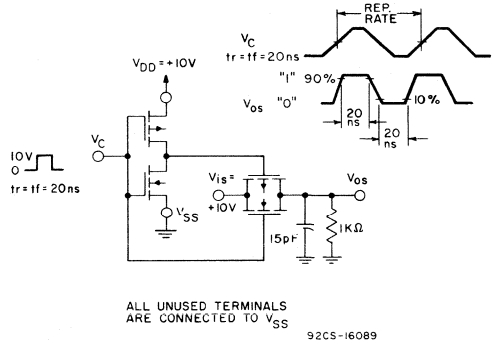


Fig. 24—Max. allowable control-input repetition rate.

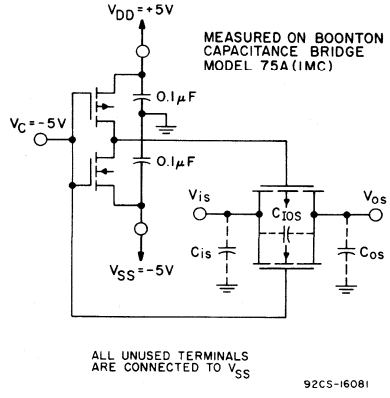
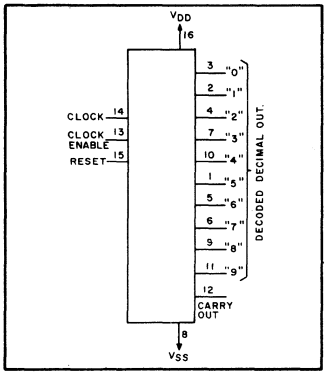


Fig. 25—Capacitance C_{IOS} and C_{OS}.

RCA Solid State Division

Digital Integrated Circuits
Monolithic Silicon

High-Reliability Slash(/) Series CD4017A/...



High-Reliability COS/MOS Decade Counter/Divider

Plus 10 Decoded Decimal Outputs

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation. . . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Fully static operation**
- **MSI complexity on a single chip. . . . . decade counter plus 10 decoded outputs**

Applications:

- **Decade counter/decimal decode display applications**
- **Frequency division**
- **Counter control/timers**
- **Divide by N counting**
  N = 2 – 10 with one CD4017A and one CD4001A
  N> 10 with multiple CD4017A's
- **For further application information, see ICAN6166 "COS/MOS MSI Counter and Register Design & Applications"**

RCA CD4017A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4017A types consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a "Clock", a "Reset", and a "Clock Enable" signal.

The decade counter is advanced one count at the positive clock signal transition if the clock enable signal is "low". Counter advancement via the clock line is inhibited when the clock enable signal is "high". A "high" reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally "low" and go "high" for one full clock cycle. A carry-out (C_{OUT}) signal completes one cycle every 10

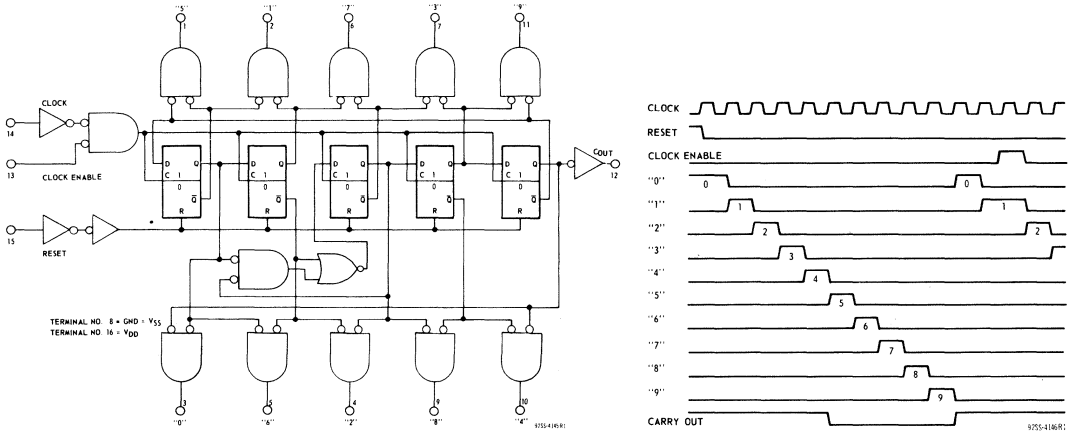


Fig. 1—Logic diagram.

clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

These devices are electrically and mechanically identical with standard COS/MOS CD4017A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4017A	MIL-M-38510/05601

The packaged types in the CD4017A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1, /2, /3, /4 --- which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels --- /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the tables below.

The CD4017A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4017AK, CD4017AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4017AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4017AD/1N

CD4017A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4017AH/N

CD4017A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

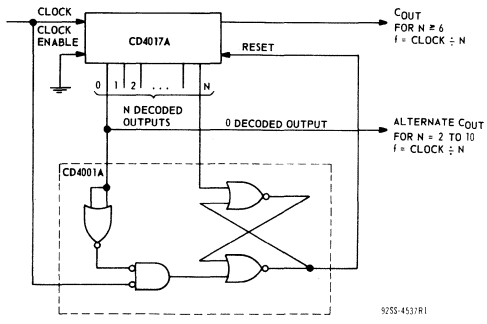


Fig. 2–Divide by N counter (N – 10) with N decoded outputs.

When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001A) generates a reset pulse which clears the CD4017A to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6, the C_{OUT} line goes "high" to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of the clock "low" and decoded "0" output "low" resets the S-R flip flop to enable the CD4017A. If the N^{th} decoded output is less than 6, the C_{OUT} line will not go "high" and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs ... $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4017AD, CD4017AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
		V_O Volts	V_{DD} Volts		−55°C			25°C			125°C					
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I_L		5		–	–	5	–	0.3	5	–	–	300	μA	3	1
			10		–	–	10●	–	0.5	10●	–	–	200●			
Quiescent Device Dissipation/Package	P_D		5		–	–	25	–	1.5	25	–	–	1500	μW	–	–
			10		–	–	100	–	5	100	–	–	2000			
Output Voltage Low-Level	V_{OL}		3		–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5		–	–	0.01	–	0	0.01	–	–	0.05			
			10		–	–	0.01	–	0	0.01	–	–	0.05			
			15		–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3		2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5		4.99	–	–	4.99	5	–	4.95	–	–			
			10		9.99	–	–	9.99	10	–	9.95	–	–			
			15		–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D = -20$ μA			−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	V_{THP}	$I_D = 20$ μA			0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}		0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	4	1
			1	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix SSD-207	V_{NH}		4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
			9	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current N-Channel	I_DN	Decoded Outputs	0.5	5	0.06	–	–	0.05●	0.1	–	0.035	–	–	mA	–	2
			0.5	10	0.12	–	–	0.1●	0.4	–	0.07	–	–			
		Carry Output	0.5	5	0.185			0.15●	0.4		0.105					
			0.5	10	0.45			0.35●	1		0.25					
P-Channel	I_DP	Decoded Outputs	4.5	5	−0.0375	–	–	−0.03●	−0.075	–	−0.021	–	–	mA	–	2
			9.5	10	−0.12	–	–	−0.1●	−0.2	–	−0.07	–	–			
		Carry Output	4.5	5	−0.185			−0.15●	−0.4		−0.105					
			9.5	10	−0.45			−0.35●	−1		−0.25					
Diode Test, 100 μA Test Pin	V_{DF}				–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix,

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range ..... −65 to +150 °C
Operating-Temperature Range ..... −55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) ..... −0.5 to +15 V
Device Dissipation (Per Package) ..... 200 mW
All Inputs ..... $V_{SS} \leq V_I \leq V_{DD}$
Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V
Recommended
Input-Voltage Swing ..... V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32"
(1.59 ± 0.79 mm) from case
for 10 s max. ..... +265 °C

DYNAMIC ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL*

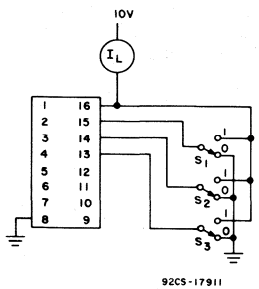
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4017AD, CD4017AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.			
CLOCKED OPERATION									
Propagation Delay Time: Carry Out Line	t_{PHL}, t_{pLH}		5	–	350	1000	ns	6	1
			10	–	125	250●			
Decode Out Lines			5	–	500	1200	ns	5	1
			10	–	200	400●			
Transition Time: Carry Out Line	t_{PHL}, t_{pLH}		5	–	100	300	ns	8	1
			10	–	50	150●			
Decode Out Lines			5	–	300	900	ns	7	1
			10	–	125	350●			
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	500	ns	–	–
			10	–	100	170			
Clock Rise & Fall Time	t_{rCL}, t_{fCL}		5	–	–	15	μs	–	1
			10	–	–	15●			
Clock Enable Set-Up Time			5	–	175	500	ns	–	–
			10	–	75	200			
Maximum Clock Frequency	f_{CL}		5	1	2.5	–	MHz	–	–
			10	3●	5	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–
RESET OPERATION									
Propagation Delay Time: To Carry Out Line	$t_{PHL(R)}$		5	–	350	1000	ns	–	–
			10	–	125	250			
To Decode Out Lines			5	–	450	1200	ns	–	–
			10	–	200	400			
Reset Pulse Width	$t_{WH(R)}$		5	–	200	500	ns	–	–
			10	–	100	165			
Reset Removal Time			5	–	300	750	ns	–	–
			10	–	100	225			

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

*Measured with respect to carry output line



Test performed with the following sequence of "1's and "0's" at each stage.

S_1	S_2	S_3	S_1	S_2	S_3
1	1	1	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
			0	1	0

Fig. 3—Quiescent device current test circuit.

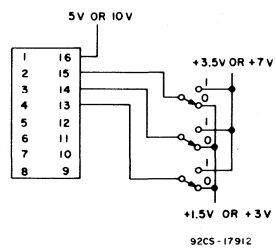


Fig.4—Noise immunity test circuit.

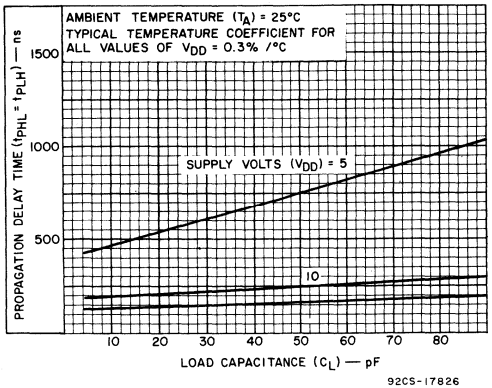


Fig. 5—Typ. propagation delay time vs. C_L for decoded outputs.

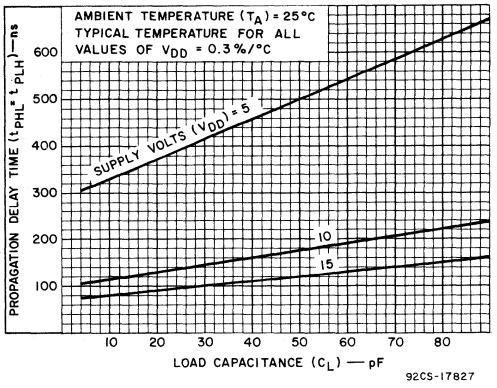


Fig. 6—Typ. propagation delay time vs. C_L for carry output.

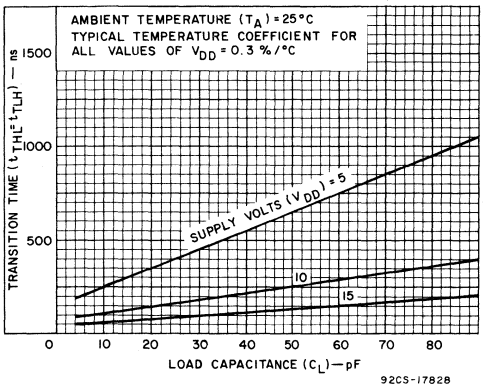


Fig. 7—Typ. transition time vs. C_L for decoded outputs.

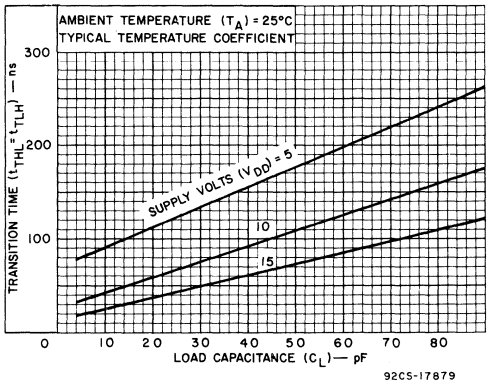


Fig. 8—Typ. transition time vs. C_L for carry output.

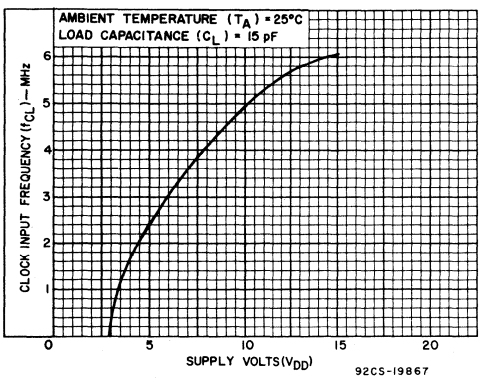


Fig. 9— Typ. clock frequency vs. V_{DD}.

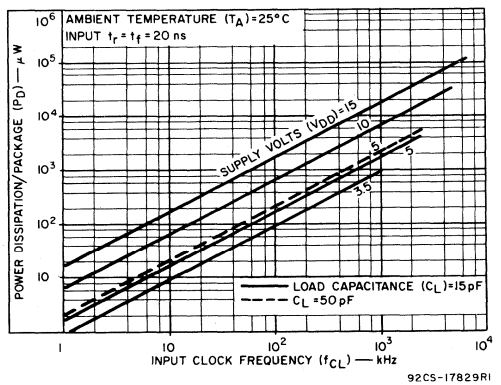
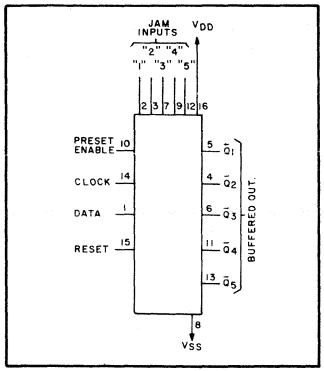


Fig. 10—Typ. dissipation characteristics.

RCA Solid State Division

Digital Integrated Circuits
Monolithic Silicon

High-Reliability Slash(/) Series CD4018A/...



High-Reliabilty COS/MOS Presettable Divide-By-'N' Counter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- **Medium speed operation. . . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Fully static operation**
- **MSI complexity on a single chip**

Applications

- **Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters**
- **Fixed and programmable counters greater than 10**
- **Programmable decade counters**
- **Divide-by-"N" counters/frequency synthesizers**
- **Frequency division**
- **Counter control/timers**

RCA CD4018A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of uses in aerospace, military, and critical industrial equipment. CD4018A types consist of 5 Johnson-Counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. "Clock", "Reset", "Data", "Preset Enable", and 5 individual "jam" inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package to properly gate the feedback connection to the Data input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018A units. The counter is advanced one count at the positive clock-signal transition. A "high" Reset signal clears the counter to an "all-zero" condition. A "high" Preset-Enable signal allows information on the Jam inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

These devices are electrically and mechanically identical with standard CD4018A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

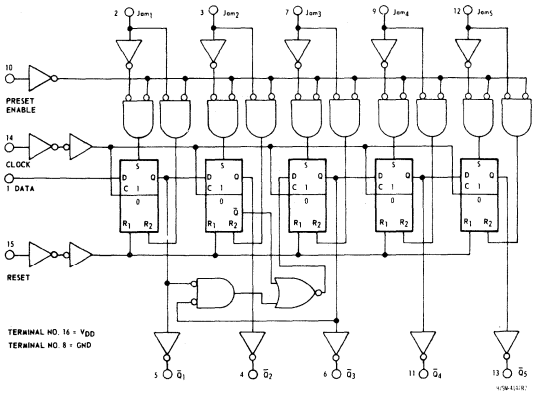


Fig. 1—Logic diagram.

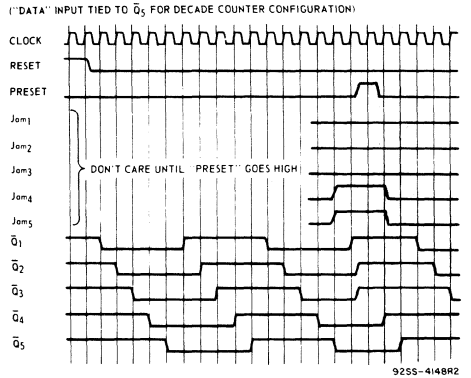


Fig. 2—Timing diagram.

RCA Designation	MIL-M-38510 Designation
CD4018A	MIL-M-38510/05602

The packaged types in the CD4018A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1, /2, /3, /4 --- which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels --- /N, /R, and standard chip. For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see tables below.

CD4018A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4018AK, CD4018AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4018AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4018AD/1N

CD4018A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic	/1N
	K = Ceramic Flat-Pack	/1R
		/1
		/2
		/3
		/4

Chip Version, CD4018AH/N

CD4018A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N
		/R

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended	
DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended	
Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering)	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

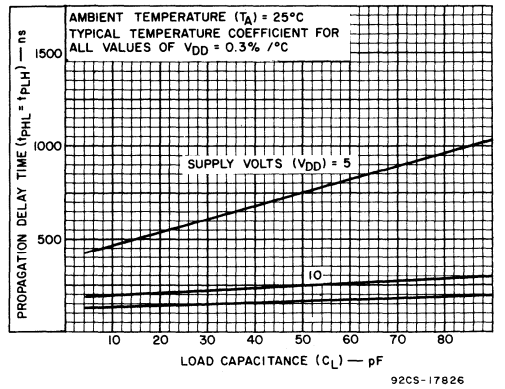


Fig. 3—Typ. propagation delay time vs. C_L for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4018AD, CD4018AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.			
Quiescent Device Current	I_L			5	–	–	5	–	0.3	5	–	–	300	μA	9	1
				10	–	–	10●	–	0.5	10●	–	–	200●			
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	1.5	25	–	–	1500	μW	–	–
				10	–	–	100	–	5	100	–	–	2000			
Output Voltage Low-Level	V_{OL}			3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
				5	–	–	0.01	–	0	0.01	–	–	0.05			
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}			3	2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
				5	4.99	–	–	4.99	5	–	4.95	–	–			
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage N-Channel	V_{THN}	$I_D = -20$ μA			−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	–
P-Channel	V_{THP}	$I_D = 20$ μA			0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}		0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	10	1
			1	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix SSD-207	V_{NH}		4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
			9	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_DN	$\overline{Q}_5$	0.5	5	0.18	–	–	0.15●	0.4	–	0.105	–	–	mA	–	2
			0.5	10	0.45	–	–	0.4●	1	–	0.25	–	–			
		$\overline{Q}_1\,\overline{Q}_2$	0.5	5	0.06	–	–	0.12●	0.1	–	0.035	–	–			
		$\overline{Q}_3\,\overline{Q}_4$	0.5	10	0.25	–	–	0.23●	0.4	–	0.14	–	–			
P-Channel	I_DP	$\overline{Q}_5$	4.5	5	−0.185	–	–	−0.15●	−0.4	–	−0.105	–	–	mA		
			9.5	10	−0.45	–	–	−0.4●	−1	–	−0.25	–	–			
		$\overline{Q}_1\,\overline{Q}_2$	4.5	5	−0.075	–	–	−0.065●	−0.15	–	−0.04	–	–			
		$\overline{Q}_3\,\overline{Q}_4$	9.5	10	−0.25	–	–	−0.2●	−0.4	–	−0.14	–	–			
Diode Test, 1000 μA Test Pin	V_{DF}				–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or a one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix,

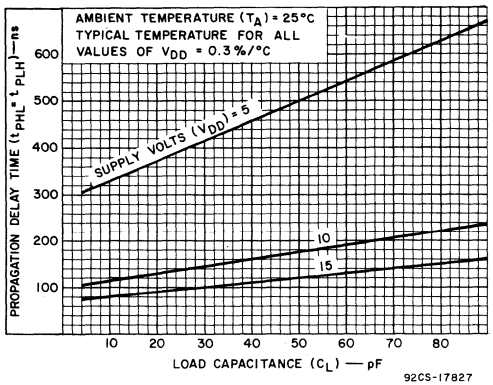


Fig. 4—Typ. propagation delay time vs. C_L for $\overline{Q}_5$ output.

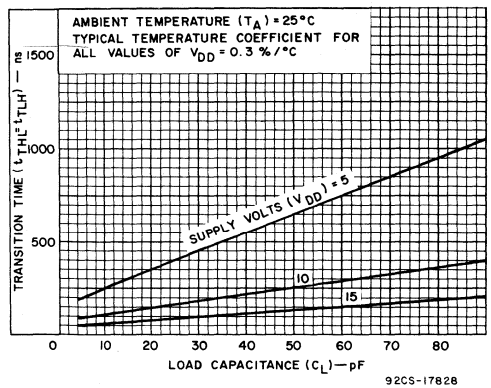


Fig. 5—Typ. transition time vs. C_L for decoded outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS, *at T_A = 25° C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL*

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4018AD, CD4018AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
CLOCKED OPERATION								
Propagation Delay Time: To $\overline{Q}_5$ Output	t_{PHL}, t_{PLH}	5	–	350	1000	ns	4	1
		10	–	125	250●			
Propagation Delay Time: To Other Outputs		5	–	500	1200	ns	3	1
		10	–	200	400●			
Transition Time: To $\overline{Q}_5$ Output	t_{THL}, t_{TLH}	5	–	100	300	ns	6	1
		10	–	50	150●			
Transition Time: To Other Outputs		5	–	300	900	ns	5	1
		10	–	125	350●			
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	200	500	ns	–	–
		10	–	100	170			
Clock Rise & Fall Time	t_{rCL}, t_{fCL}	5	–	–	15	μs	–	1
		10	–	–	15●			
Data Input Set-Up Time		5	–	175	500	ns	–	–
		10	–	75	200			
Maximum Clock Frequency	f_{CL}	5	1	2.5	–	MHz	–	1
		10	3●	5	–			
Input Capacitance	C_I	Any Input	–	5	–	pF	–	–
PRESET* OR RESET OPERATION								
Propagation Delay Time: To $\overline{Q}_5$ Output	$t_{PLH(R)}$,	5	–	350	1000	ns	–	–
		10	–	125	250			
Propagation Delay Time: To Other Outputs	$t_{PHL(PR)}$, $t_{PLH(PR)}$	5	–	500	1200	ns	–	–
		10	–	200	400			
Preset or Reset Pulse Width	$t_{WH(R)}$ $t_{WH(PR)}$	5	–	200	500	ns	–	–
		10	–	100	165			
Preset or Reset Removal Time		5	–	300	750	ns	–	–
		10	–	100	225			

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only

*At Preset Enable or Jam Inputs.

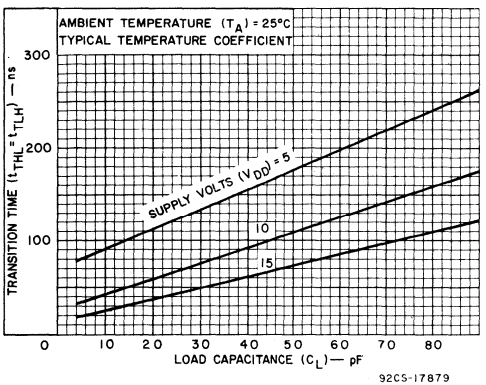


Fig. 6—Typ. transition time vs. C_L for $\overline{Q}_5$ output.

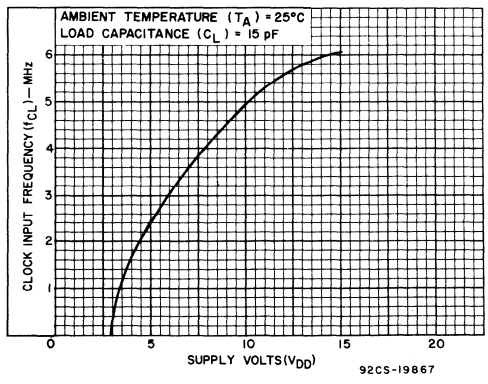


Fig. 7—Typ. clock frequency vs. V_{DD}.

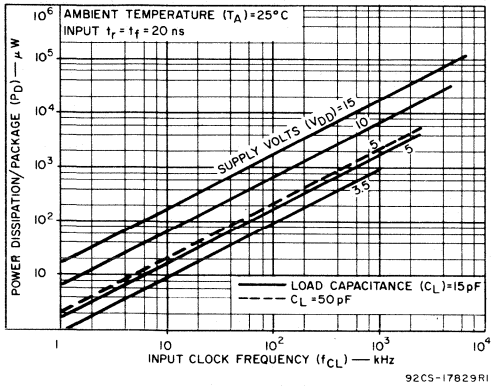
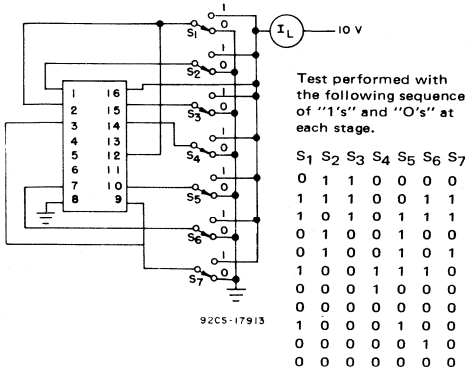


Fig. 8—Typ. dissipation characteristics.



Test performed with the following sequence of "1's" and "0's" at each stage.

S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	1	1	0	0	0	0
1	1	1	0	0	1	1
1	0	1	0	1	1	1
0	1	0	0	1	0	0
0	1	0	0	1	0	1
1	0	0	1	1	1	0
0	0	0	1	0	0	0
0	0	0	0	0	0	0
1	0	0	0	1	0	0
0	0	0	0	0	1	0
0	0	0	0	0	0	0

Fig. 9—Quiescent device current test circuit.

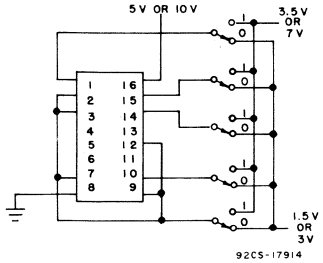


Fig. 10—Noise immunity test circuit.

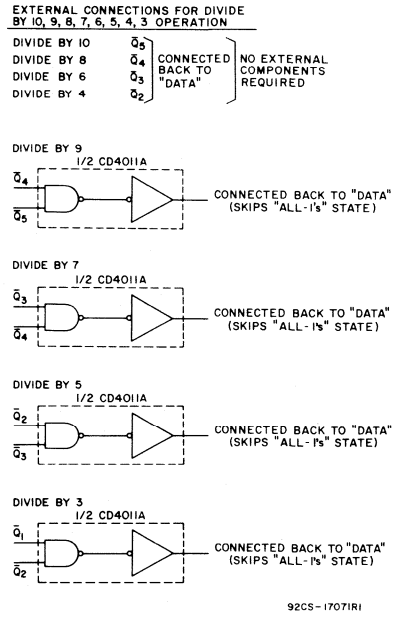


Fig. 11—External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3 operation.

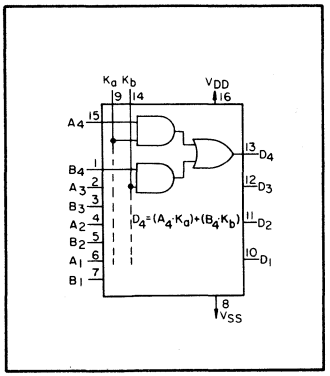
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4019A/...



High-Reliability COS/MOS Quad AND-OR Select Gate

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation . . . $t_{PHL} = t_{PLH}$ = 50 ns (typ.) at C_L = 15 pF**

Applications

- **AND-OR select gating**
- **Shift-right/shift-left registers**
- **True/complement selection**
- **AND/OR/Exclusive-OR selection**

RCA CD4019A "Slash" (/) Series are high-reliability COS/MOS integrated circuit Quad AND-OR Select Gates intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4019A types are comprised of four AND-OR-Select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A+B function.

These devices are electrically and mechanically identical with standard COS/MOS CD4019A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these

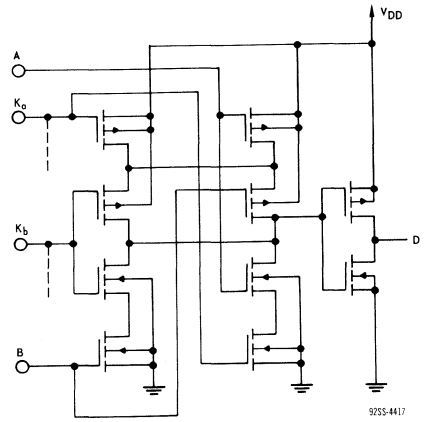


Fig.1 – Schematic diagram for 1 of 4 identical stages.

TYPICAL CD4019A APPLICATIONS

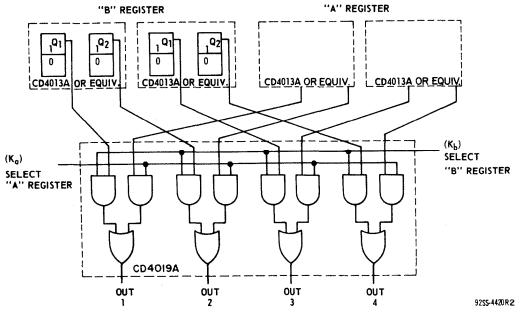


Fig.2 – AND/OR select gating.

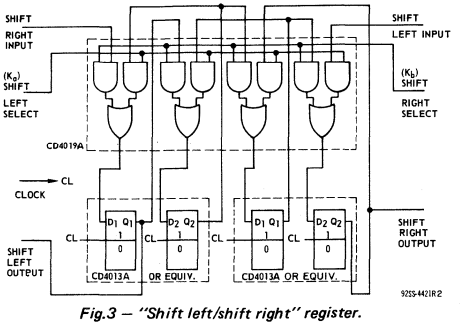


Fig.3 – "Shift left/shift right" register.

circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series Types".

RCA Designation	MIL-M-38510 Designation
CD4019A	MIL-M-38510/05302

The packaged types in the CD4019A "Slash" (/) Series can be supplied to six screening levels ——— /1N, /1R, /1, /2, /3, /4 ——— which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels ——— /N, /R, and standard chip. For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types"

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the tables below.

The CD4019A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4019AK, CD4019AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4019AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

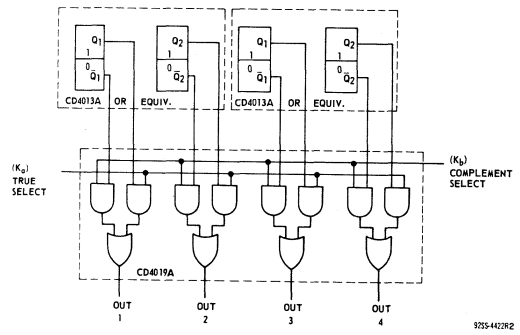


Fig.4—"True complement" selector.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . . $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4019AD, CD4019AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.03	5	–	–	300	μA	10	1
			10	–	–	10●	–	0.05	10●	–	–	200●			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	0.15	25	–	–	1500	μW	–	–
			10	–	–	100	–	0.5	100	–	–	2000			
Output Voltage Low-Level	V_{OL}		3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	4.95	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.45●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D = -20\ \mu A$		−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	V_{THP}	$I_D = 20\ \mu A$		0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Inputs)	V_{NL}	0.95	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	11	1
		2.9	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix SSD-207	V_{NH}	3.6	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		7.2	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_{DN}	0.5	5	0.6	–	–	0.7●	0.9	–	0.3	–	–	mA	–	2
		0.5	10	0.9	–	–	1.2●	1.5	–	0.55	–	–			
P-Channel	I_{DP}	4.5	5	−0.31	–	–	−0.25●	−0.5	–	−0.175	–	–	mA	–	2
		9.5	10	−0.95	–	–	−0.7●	−1.5	–	−0.5	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

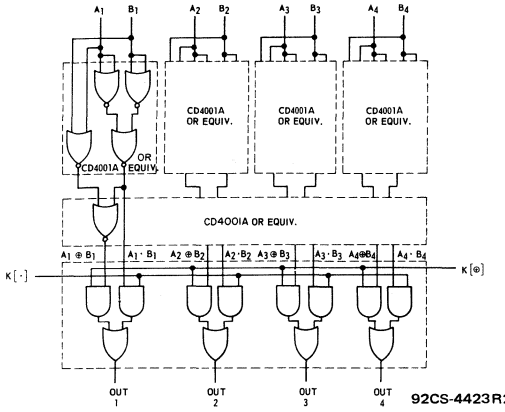


Fig.5—AND/OR Exclusive-OR selector.

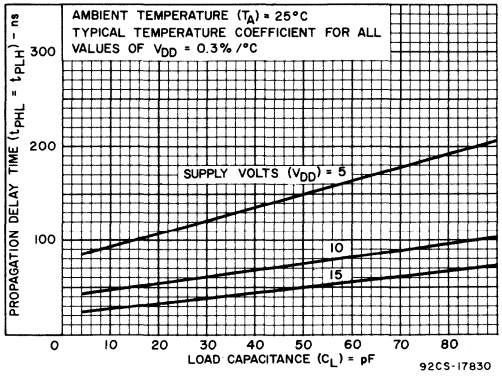


Fig.6—Typ. propagation delay time vs C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3 %/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4019AD, CD4019AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time:	t_{PHL}, t_{PLH}		5	–	100	225	ns	6	1
			10	–	50	100●			
Transition Time	t_{THL}, t_{TLH}		5	–	100	200	ns	7	1
			10	–	40	65●			
Input Capacitance	C_I	All A and B Inputs		–	5	–	pF	–	–
		K_A and K_B Inputs		–	12	–			

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is a one input one output only.

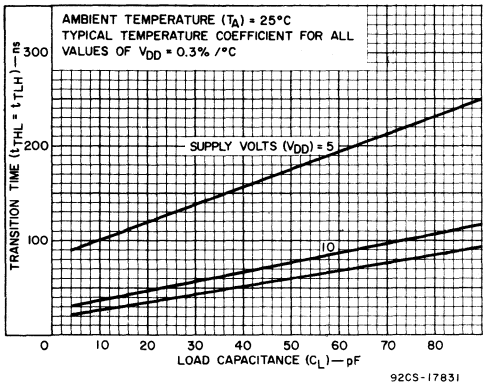


Fig.7—Typ. transition time vs C_L.

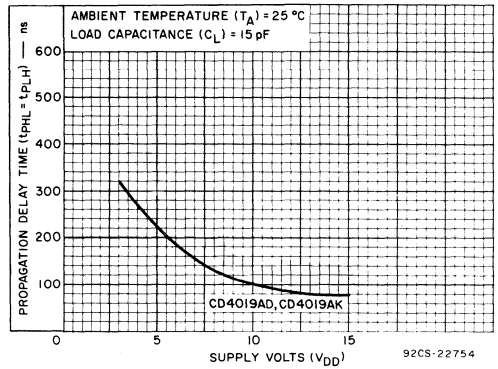


Fig.8—Max. propagation delay time vs V_{DD}.

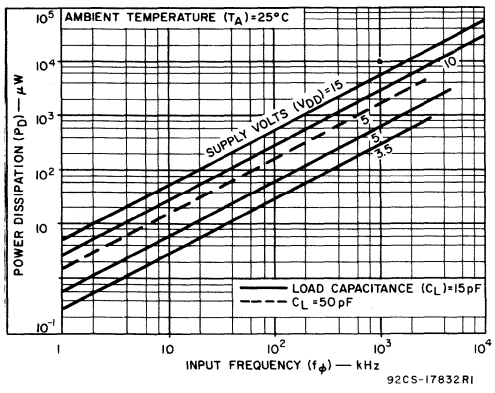


Fig.9—Typ. dissipation characteristics (per output).

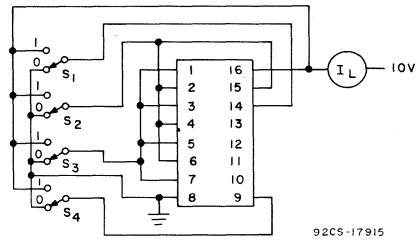


Fig.10—Quiescent device current test circuit.

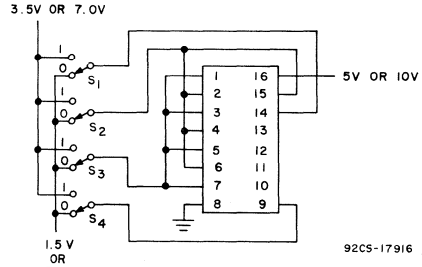


Fig.11—Noise immunity test circuit.

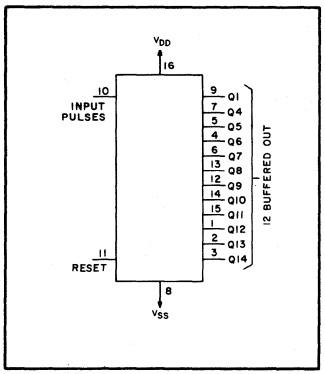
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4020A/...



High-Reliability COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- **Medium speed operation. . . . . 7 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Low "high" - and "low" -level output impedance. . . . . 1000Ω (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **MSI complexity on a single chip. . . . . 14 fully static, master-slave stages**
- **COS/MOS gate-input loading at both Reset and Input-pulse lines**

Applications

- **Frequency-dividing circuits**
- **Time-delay circuits**
- **Counter control**
- **Counting functions**

RCA CD4020A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4020A types consist of a pulse input shaping circuit, reset line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its "all zeroes" state by a high level on the reset inverter input line. Each counter stage is a static master-slave flip-flop.

The counter is advanced one count on the negative-going transition of each input pulse. These devices are electrically and mechanically identical with standard COS/MOS types CD4020A described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

RCA Designation	MIL-M-38510 Designation
CD4020A	MIL-M-38510/05603

The packaged types in the CD4020A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1,/2, /3, /4 ---which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to

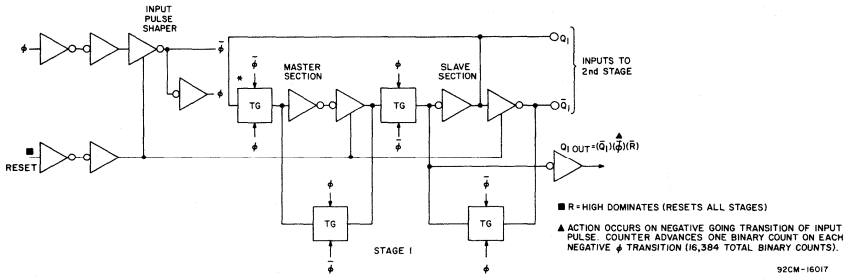


Fig. 1—Logic diagram for 1 of 14 binary stages.

three screening levels --- /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types",*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuits part number, see the following page.

The CD4020A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4020AK, CD4020AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4020AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4020AD/1N

CD4020A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4020AH/N

CD4020A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

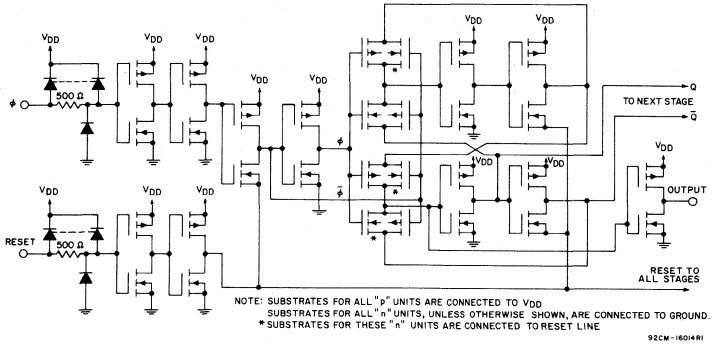


Fig. 2–Schematic diagram of pulse shapers and 1 of 14 binary stages.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} < V_I < V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4020AD, CD4020AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	15	–	0.5	15	–	–	900	μA	11	1
			10	–	–	25●	–	1	25●	–	–	500●			
Quiescent Device Dissipation/Package	P_D		5	–	–	75	–	2.5	75	–	–	4500	μW	10	–
			10	–	–	250	–	10	250	–	–	5000			
Output Voltage Low-Level	V_{OL}		3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$		−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$		0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}	0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	12, 13	1
		1	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix SSD-207	V_{NH}	4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		9	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	$I_D N$	0.5	5	0.9	–	–	0.15●	0.2	–	0.05	–	–	mA	–	2
		0.5	10	0.185	–	–	0.3●	0.4	–	0.105	–	–			
P-Channel	$I_D P$	4.5	5	−0.11	–	–	−0.09●	−0.25	–	−0.065	–	–	mA	–	2
		9.5	10	−0.25	–	–	−0.2●	−0.5	–	−0.14	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

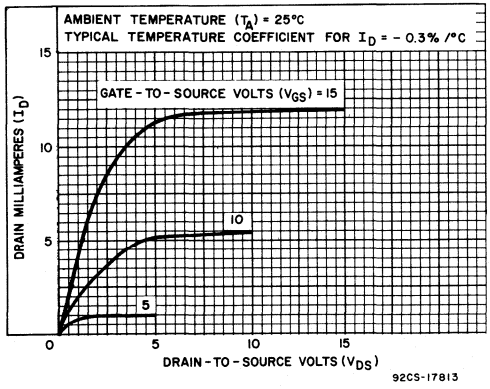


Fig. 3—Typ. n-channel drain characteristics.

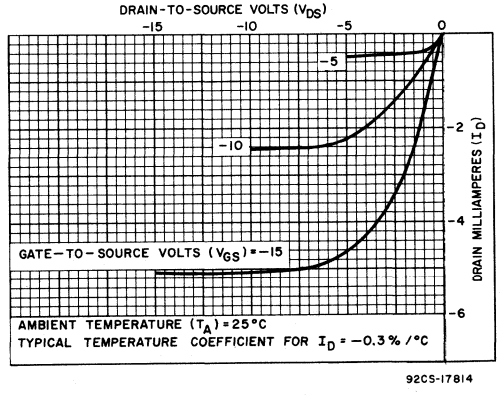


Fig. 4—Typ. p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_rCL, t_fCL*

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4020AD, CD4020AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
CLOCKED OPERATION									
Propagation Delay Time	t_{PHL}, t_{PLH}	*	5	–	450	600	ns	7	1
			10	–	150	225●			
Transition Time	t_{THL}, t_{TLH}		5	–	450	600	ns	8	1
			10	–	200	300●			
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	335	ns	–	–
			10	–	70	125			
Clock Rise & Fall Time	t_rCL, t_fCL		5	–	–	15	μs	–	1
			10	–	–	15●			
Maximum Clock Frequency	f_{CL}		5	1.5	2.5	–	MHz	9	1
			10	4●	7	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–
RESET OPERATION									
Propagation Delay Time:	$t_{PHL(R)}$		5	–	2000	3000	ns	7	–
			10	–	500	775			
Minimum Reset Pulse Width	$t_{WH(R)}$		5	–	1800	2500	ns	–	–
			10	–	300	475			

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

*Propagation Delay is from clock input to Q_1 output.

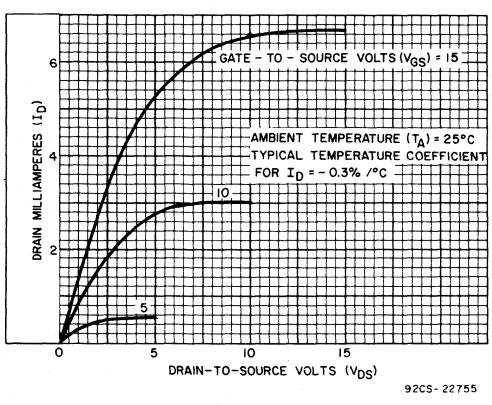


Fig. 5—Min. n-channel drain characteristics.

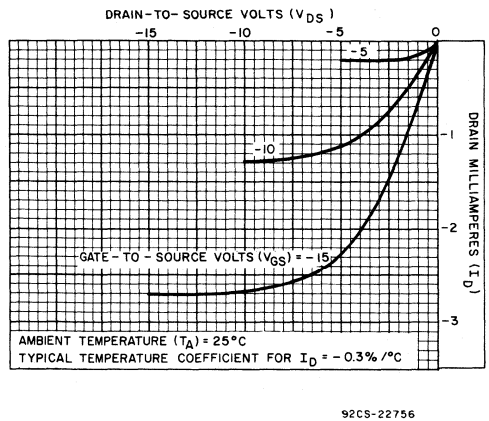


Fig. 6—Min. p-channel drain characteristics.

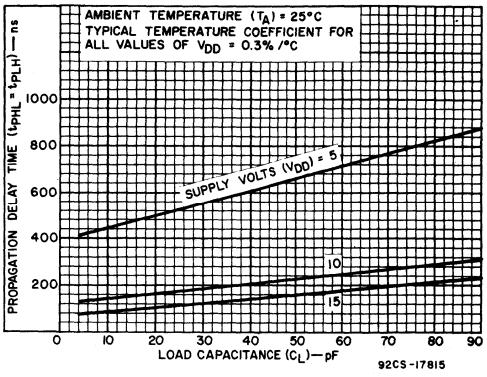


Fig. 7—Typ. propagation delay time vs. C_L.

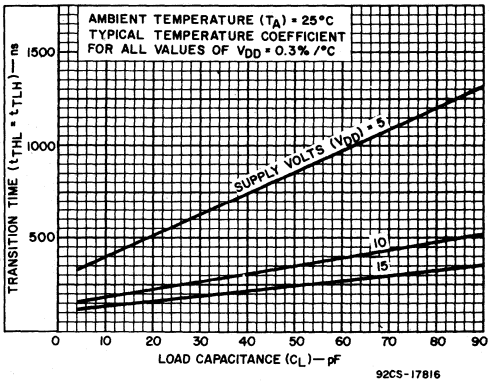


Fig. 8—Typ. transition time vs. C_L.

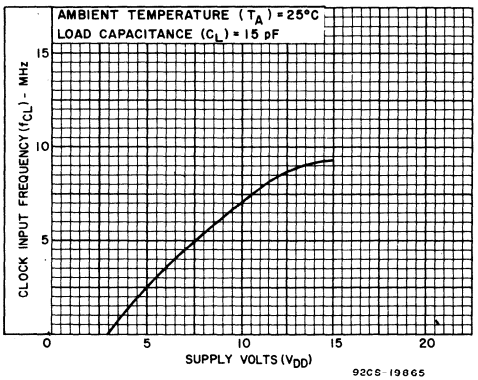


Fig. 9—Typ. clock frequency vs. V_{DD}.

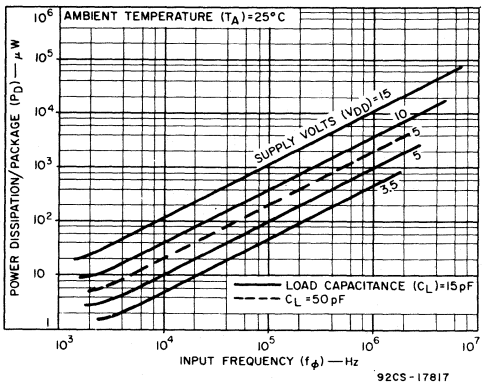


Fig. 10—Typ. dissipation characteristics.

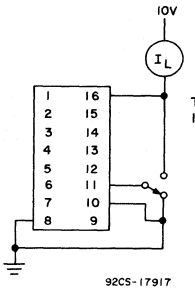


Fig. 11—Quiescent device dissipation test circuit.

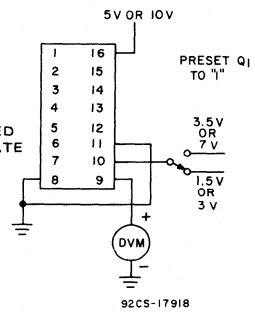


Fig. 12—Noise immunity test circuit.

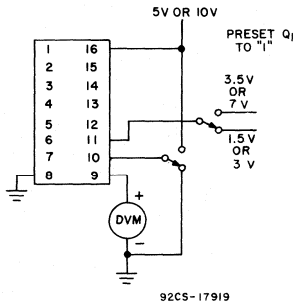


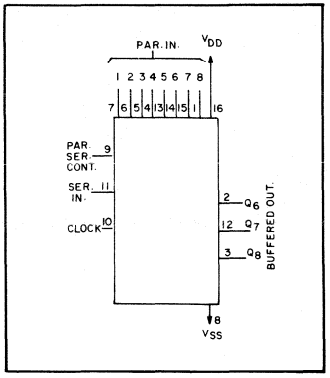
Fig. 13—Reset noise immunity test circuit.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4021A/...



High-Reliability COS/MOS 8-Stage Static Shift Register

Asynchronous Parallel Input/Serial Output, Synchronous Serial Input/Serial Output For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

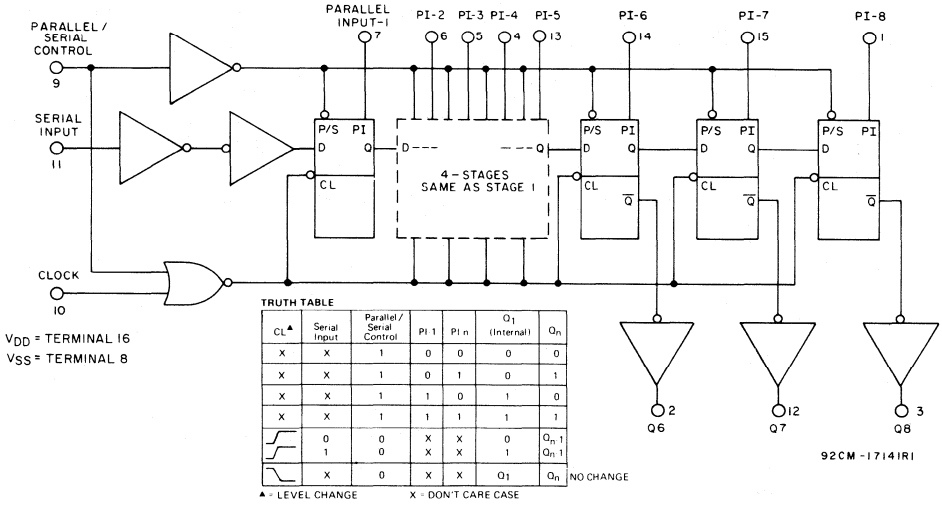
- **Asynchronous parallel or synchronous serial operation under control of parallel/serial control-input**
- **Individual "jam" inputs to each register stage**
- **Master-slave flip-flop register stages**
- **Fully static operation. . . . . .DC to 5 MHz**

RCA CD4021A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4021A types are 8-stage parallel or serial-input/serial-output shift registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. "Q" outputs are available from the sixth, seventh, and eighth stages.

Applications:

- **Asynchronous parallel input/serial output data queueing**
- **Parallel to serial data conversion**
- **General purpose register**

When the parallel/Serial Control input is "low", data is serially shifted into the 8-stage register synchronously with the positive-going transition of the Clock pulse. When the Parallel/Serial Control input is "high", data is Jammed into the 8-stage register via the parallel input lines asychronously with the clock line. Register expansion is possible using additional CD4021A packages.



V_{DD} = TERMINAL 16
V_{SS} = TERMINAL 8

TRUTH TABLE

CL▲	Serial Input	Parallel/Serial Control	PI 1	PI n	Q_1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⌐⌐	0	0	X	X	0	Q_{n-1}	
⌐⌐	1	0	X	X	1	Q_{n-1}	
⌐	X	0	X	X	Q_1	Q_n	NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

Fig. 1—Logic diagram and truth table.

These devices are electrically and mechanically identical with standard COS/MOS CD4021A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510 as shown in RIC-104, "MIL-M-38510/COS/MOS CD4000A Series types."

RCA Designation	MIL-M-38510 Designation
CD4021A	MIL-M-38510/05704

The packaged types in the CD4021A "Slash" (/) can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /N, /R, and standard chip.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102B, "High-Reliability COS/CD4000A "Slash" (/) Series Types".

The CD4021A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4021AD, CD4021AK,	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4021AH,	Custom	/N	√	
		/R	√	
	Standard Chip		√	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

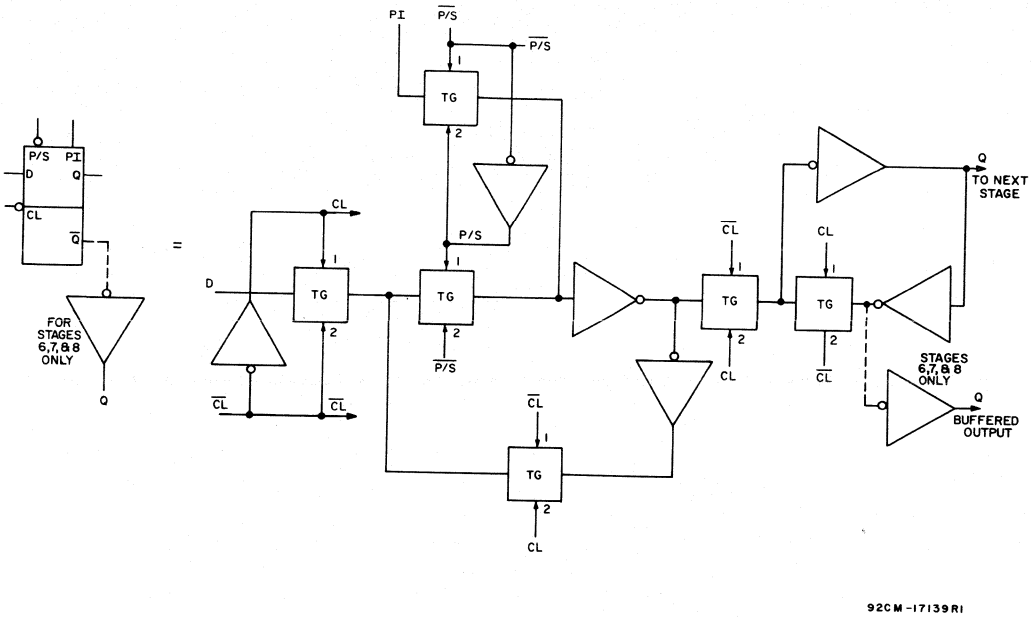


Fig. 2—One typical stage and its equivalent detailed circuit.

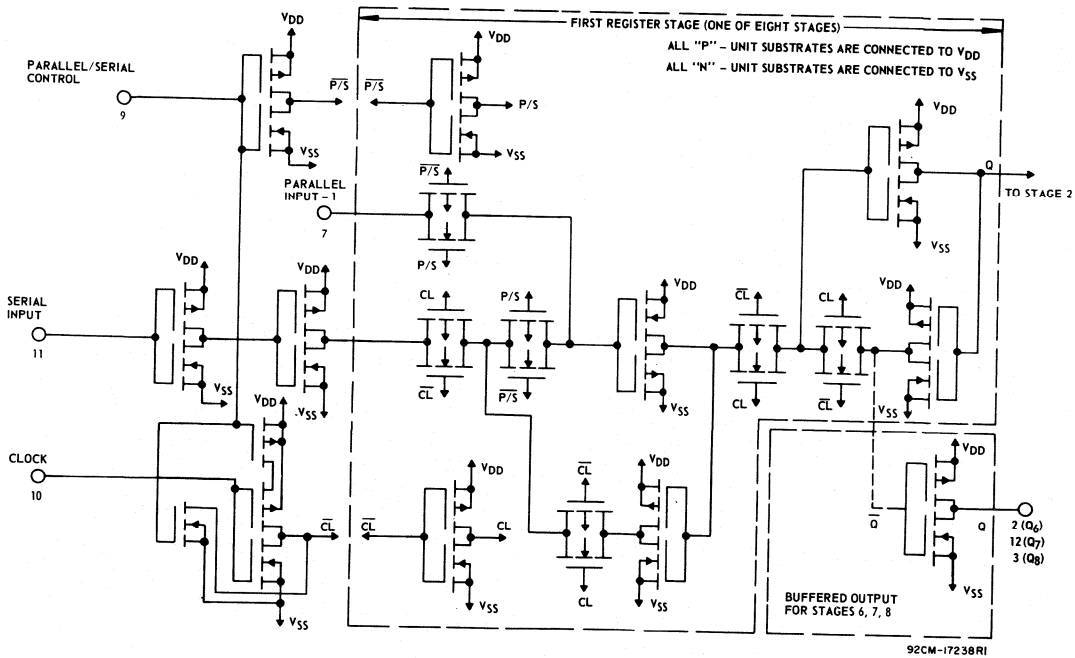


Fig. 3—Schematic diagram—CD4021A.

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4021AD, CD4021AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.5	5	–	–	300	μA	8	1
			10	–	–	10•	–	1	10•	–	–	200•			
Quiescent Deivce Dissipation/Package	P_D		5	–	–	25	–	2.5	25	–	–	1500	μW	–	–
			10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}		3	–	–	0.55•	–	–	0.5•	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5•	–	–	0.55•			
High-Level	V_{OH}		3	2.25•	–	–	2.3•	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5•	–	–	14.45•	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = -20 μA		-0.7•	-1.7	-3•	-0.7•	-1.5	-3•	-0.3•	-1.3	-3•	V	–	2
P-Channel	V_{THP}	I_D = 20 μA		0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•	V		
Noise Immunity (All Inputs) *For Definition, See Appendix in SSD-207*	V_{NL}	0.8	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	9	1
		1.0	10	3•	–	–	3•	4.5	–	2.9•	–	–			
	V_{NH}	4.2	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V		
		9.0	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: N-Channel	I_{DN}	0.5	5	0.15	–	–	0.15•	0.3	–	0.085	–	–	mA	–	2
		0.5	10	0.31	–	–	0.25•	0.5	–	0.175	–	–			
P-Channel	I_{DP}	4.5	5	-0.1	–	–	-0.08•	-0.16	–	-0.055	–	–	mA		
		9.5	10	-0.25	–	–	-0.20•	-0.44	–	-0.14	–	–			
Diode Test 100 μA Test Pin	V_{DF}		–	–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

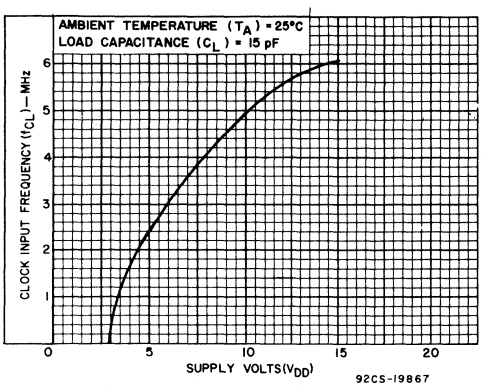


Fig. 4—Typ. clock frequency vs. V_{DD}.

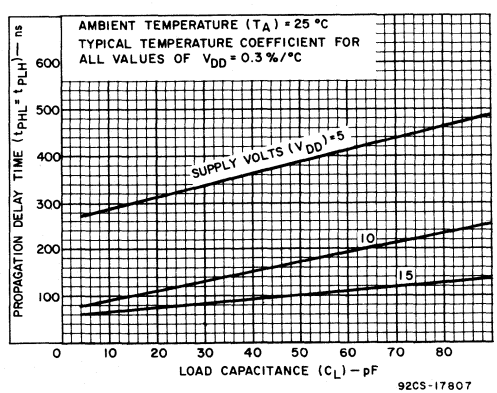


Fig. 5—Typ. propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF and input rise and fall times = 20 ns except t_rCL, t_fCL Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
				CD4021AD, CD4021AK					
			V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time**	t_{PHL}, t_{PLH}		5	–	300	750	ns	5	1
			10	–	100	225•			
Transition Time	t_{THL}, t_{TLH}		5	–	150	300	ns	6	–
			10	–	75	125•			
Minimum Clock Pulse Width	t_{WL} = t_{WH}		5	–	200	500	ns	–	–
			10	–	100	175			
Minimum High-Level Parallel/Serial Control Pulse Width	$t_{WH(P/S)}$		5	–	200	500		–	–
			10	–	100	175			
Clock Rise & Fall Time	*t_rCL = t_fCL		5	–	–	15	μs	–	1
			10	–	–	15•			
Set-Up Time			5	–	100	350	ns	–	–
			10	–	50	80			
Maximum Clock Frequency	f_{CL}		5	1	2.5	–	MHz	–	1
			10	3•	5	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

**From Clock or Parallel/Serial Control Input

NOTE 1: Test is a one input one output only

* If more than one unit is cascaded in a parallel clocked operation t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

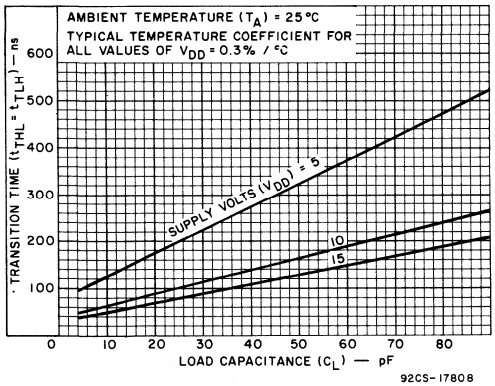


Fig. 6—Typ. transition time vs. C_L.

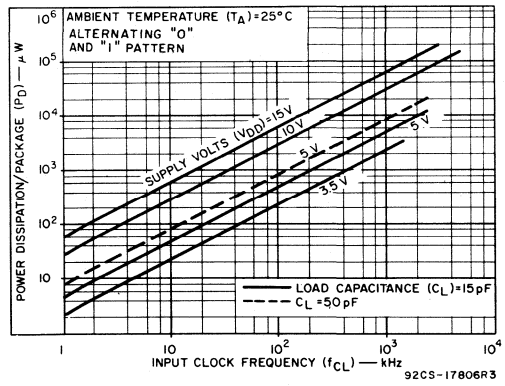


Fig. 7—Typ. dissipation characteristics.

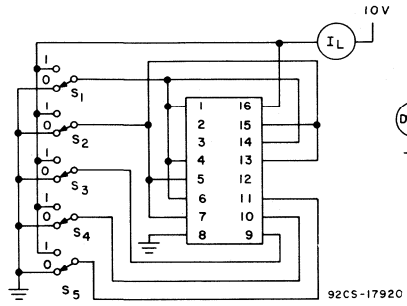
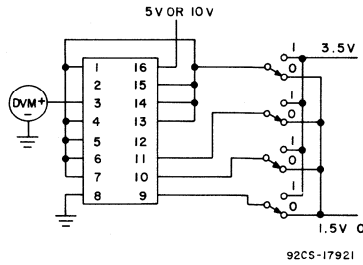


Fig. 8—Quiescent device current test circuit.



Test performed with the following sequence of "One's" and "Zero's".

S_1	S_2	S_3	S_4	S_5
0	0	1	0	0
1	0	1	1	1
1	0	1	0	1
0	1	1	1	1
0	1	0	0	0

Fig. 9—Noise immunity test circuit.

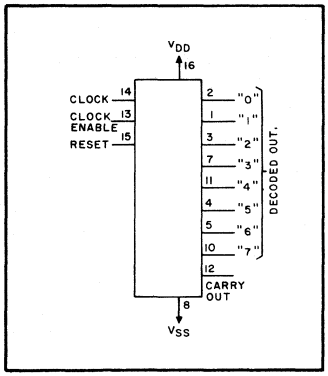
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4022A/...



High Reliability COS/MOS Divide-By-8 Counter/Divider with 8 Decoded Outputs

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation. . . . . .5 MHz (typ.) at $V_{DD}-V_{SS}$ = 10 V**
- **MSI complexity on a single chip**
- **Divide by N counting; N = 2 to 8 with one CD4022A plus one CD4001A, package**

Applications:

- **Binary counting/decoding**
- **Binary frequency division**
- **Binary counter control/timers**

RCA CD4022A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. CD4022A types consist of a 4-stage divide-by-8 Johnson counter, associated decode output gating, and a carry-out bit. The counter is cleared to its zero count by a "high" reset signal. The counter is advanced on the positive clock-signal transition provided the clock enable signal is "low".

Use of the Johnson divide-by-8 counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoder outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decode gating outputs are normally "low" and go "high" only at their respective decoded time slot. Each decode gate output remains "high" for one full clock cycle. The carry-out signal completes one cycle every 8 clock-input cycles and is used as a ripple-carry signal to directly clock a succeeding counter package in a multi-package counting system. These devices are electrically and mechanically identical to standard COS/MOS CD4022A types described in data bulletin 479 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

RCA Designation	MIL-M-38510 Designation
CD4022A	MIL-M-38510/05604

The packaged types in the CD4022A "Slash" (/) Series can

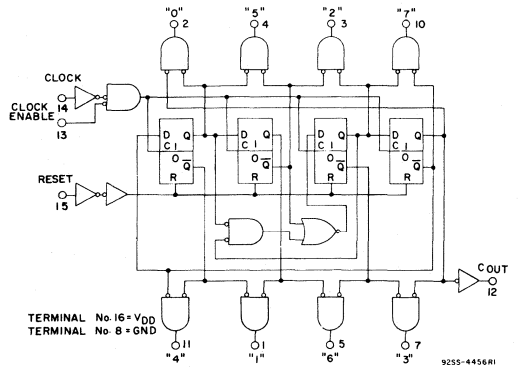


Fig. 1—Logic diagram.

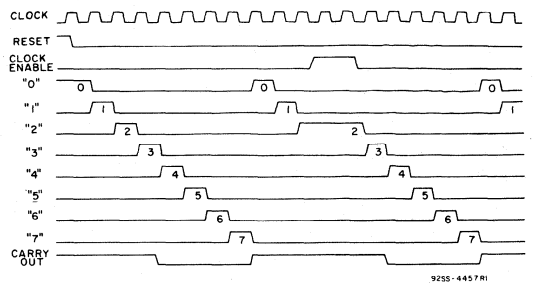


Fig. 2—Timing diagram.

be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 - which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to screening levels – /N, /R, and standard chip.

For a description of the screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Series Types".

The CD4022A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended	
DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended	
Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering)	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4022AD, CD4022AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4022AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

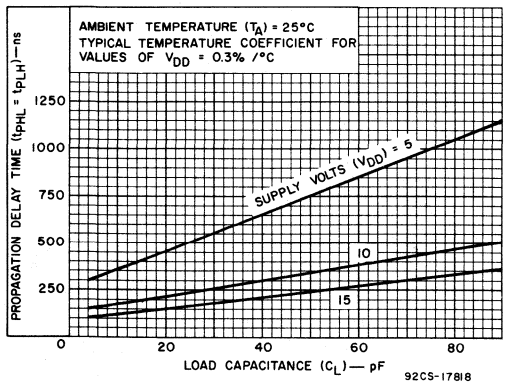


Fig. 3–Typ. propagation delay time vs. C_L for decoded outputs.

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

	CD4000A	D	/1N
		Package Suffix Letter	Screening Level
Type Designation		D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

	CD4000A	H	/N
		Package Suffix Letter	Screening Level
Type Designation		H = Chip Version	/N /R

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
					CD4022AD, CD4022AK											
		V_O Volts		V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.			
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	μA	9	2
				10	–	–	10.	–	1	10.	–	–	200.			
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	μW	–	
				10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55.	–	–	0.5.	–	–	–	V		1
				5	–	–	0.01	–	0	0.01	–	–	0.05			
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.5	–	–	0.55.			
High-Level	V_{OH}			3	2.25.	–	–	2.3.	–	–	–	–	–	V		1
				5	4.99	–	–	4.99	5	–	4.95	–	–			
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.5.	–	–	14.45.	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = -20 μA			-0.7.	-1.7	-3.	-0.7.	-1.5	-3.	-0.3.	-1.3	-3.	V		2
P-Channel	V_{THP}	I_D = 20 μA			0.7.	1.7	3.	0.7.	1.5	3.	0.3.	1.3	3.			
Noise Immunity (All Inputs) *For Definition, See Appendix in SSD-207*	V_{NL}		0.8	5	1.5	–	–	1.5.	2.25	–	1.4	–	–	V	10	1
			1.0	10	3.	–	–	3	4.5	–	2.9	–	–			
	V_{NH}		4.2	5	1.4	–	–	1.5.	2.25	–	1.5	–	–	V		
			9.0	10	2.9.	–	–	3.	4.5	–	3.	–	–			
Output Drive Current N-Channel	I_{DN}	Decoded Outputs	0.5	5	0.062	–	–	0.05.	0.15	–	0.035	–	–	mA		2
			0.5	10	0.12	–	–	0.1.	0.3	–	0.07	–	–			
		Carry Outputs	0.5	5	0.185	–	–	0.15.	0.5	–	0.105	–	–			
			0.5	10	0.375	–	–	0.3.	1	–	0.21	–	–			
P-Channel	I_{DP}	Decoded Outputs	4.5	5	-0.038	–	–	-0.03	-0.075	–	-0.021	–	–	mA		
			9.5	10	-0.062	–	–	-0.1.	-0.15	–	-0.035	–	–			
		Carry Outputs	4.5	5	-0.185	–	–	-0.15.	-0.4	–	-0.105	–	–			
			9.5	10	-0.375	–	–	-0.3.	-0.8	–	-0.21	–	–			
Diode Test 100 μA Test Pin	–			–	–	–	1.5.	–	–	1.5.	–	–	1.5.	V		3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

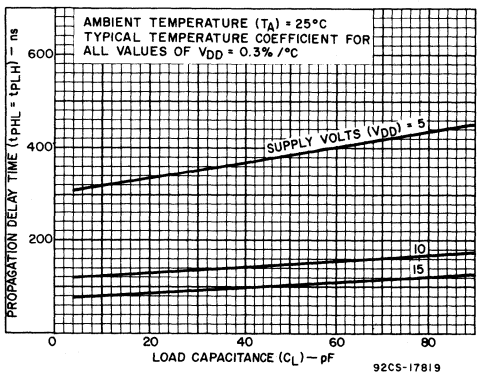


Fig. 4—Typ. propagation delay time vs. C_L for carry output.

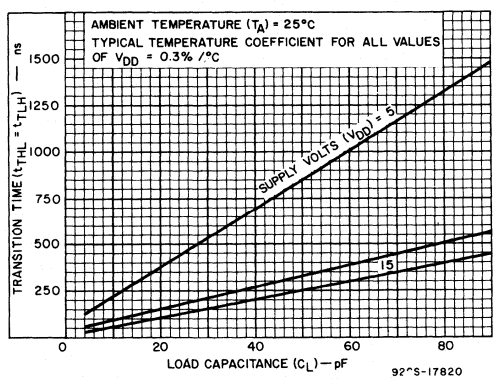


Fig. 5—Typ. transition time vs. C_L for decoded outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times 20 ns except t_rCL, t_fCL

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4022AD, CD4022AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
CLOCKED OPERATION									
Propagation Delay Time: Carry-Out Line	t_{PHL} = t_{PLH}		5	–	325	1000	ns	4	1
			10	–	125	250•			
Decode Out Lines			5	–	400	1200	ns	3	
			10	–	200	400			
Transition Time: Carry-Out Line	t_{THL} = t_{TLH}		5	–	85	300	ns	6	
			10	–	50	100			
Decode-Out Lines			5	–	300	900	ns	5	
			10	–	125	250			
Minimum Clock Pulse Width	t_{WL} = t_{WH}		5	–	250	500	ns	11	
			10	–	85	170			
Clock Rise & Fall Time	t_rCL = t_fCL		5	–	–	15	μs	11	1
			10	–	–	15•			
Clock Enable Set-Up Time			5	350	175	–	ns	12	
			10	150	75	–			
Maximum Clock Frequency	f_{CL}		5	1	2.5	–	MHz	7	1
			10	3•	5	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	
RESET OPERATION									
Propagation Delay Time: Carry-Out Line	t_{PHL} = t_{PLH}		5	–	300	900	ns	–	1
			10	–	125	250			
Decade-Out Line			5	–	500	1250	ns	–	
			10	–	200	400			
Minimum Reset Pulse Width	t_{WL} = t_{WH}		5	–	150	300	ns	13	
			10	–	75	150			

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is a one-input, one-output only.

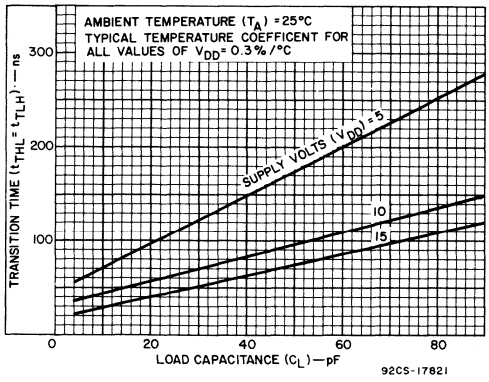


Fig. 6—Typ. transition time vs. C_L for carry output.

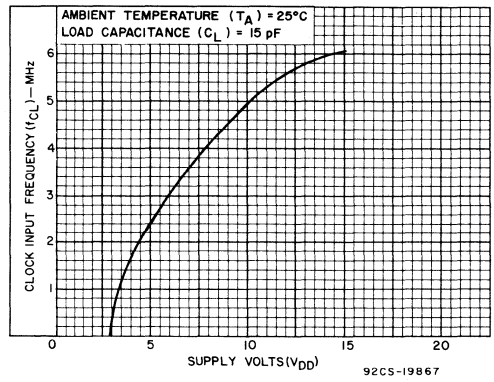


Fig. 7—Typical clock frequency vs. V_{DD}.

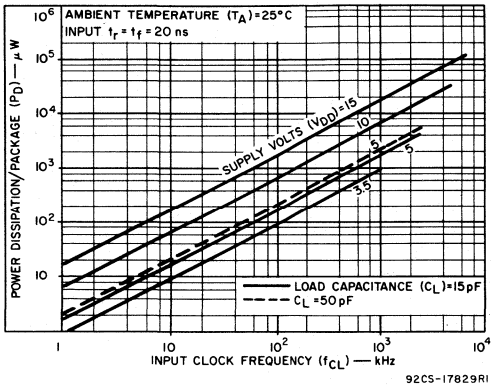


Fig. 8—Typical dissipation characteristics.

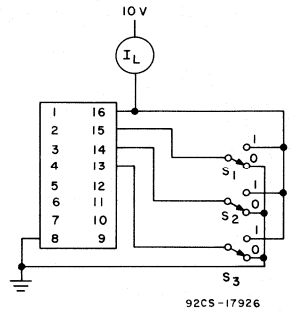


Fig. 9—Quiescent device current test circuit.

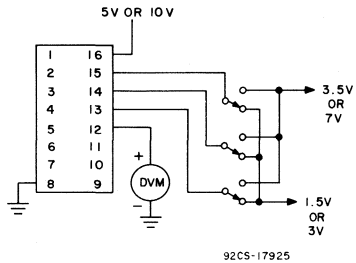


Fig. 10—Noise immunity test circuit.

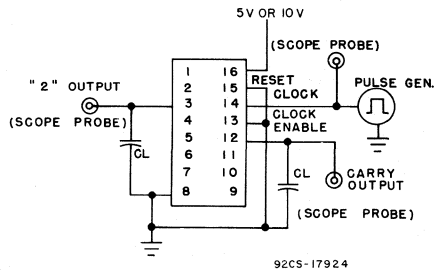


Fig. 11—Clock line test set-up.

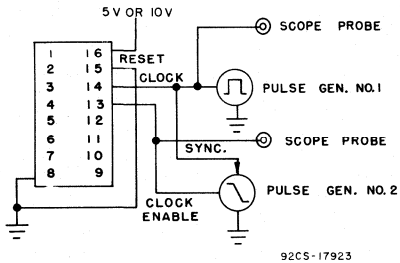


Fig. 12—Clock enable and set-up time test circuit.

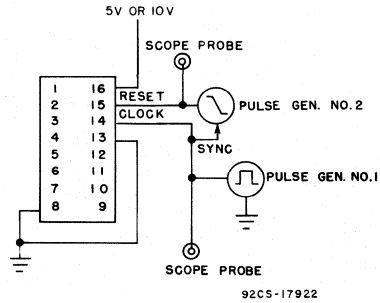


Fig. 13—Reset propagation delay time and minimum reset pulse duration.

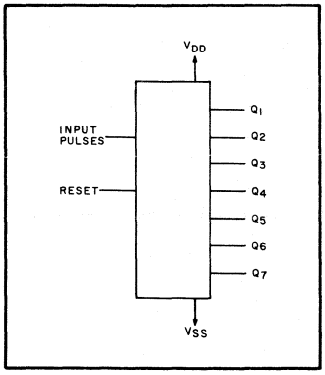
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4024A/...



High-Reliability COS/MOS 7-Stage Binary Counter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation.....7MHz (typ.) input pulse rate at $V_{DD}-V_{SS}$ = 10 V**
- **Low "high" and "low" level output impedance.....700Ω and 500Ω (typ.), respectively at $V_{DD}-V_{SS}$ = 10 V**
- **Logic block complexity on a single chip.....each output accessible and resettable**
- **Static counter operation—counter retains state indefinitely with input pulse level "low" or "high"**
- **COS/MOS gate input loading on both reset and input-pulse lines**

RCA CD4024A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4024A types consist of an input-pulse-shaping circuit, reset-line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse. These devices are electrically and mechanically identical to standard COS/MOS CD4024A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

RCA Designation	MIL-M-38510 Designation
CD4024A	MIL-M-38510/05605

Applications:

- **Frequency-dividing circuits.**
- **Time-delay circuits**
- **Counter control**
- **D/A counter and switch on one chip**

The packaged types in the CD4024A "Slash" (/) Series can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /N, /R, and standard chip.

For a description of the screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Series Types".

The CD4024A "Slash (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

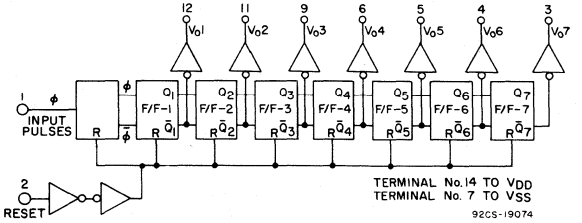


Fig. 1—Functional diagram for CD4024AD, AK.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DC}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4024AD, CD4024AK,	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4024AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

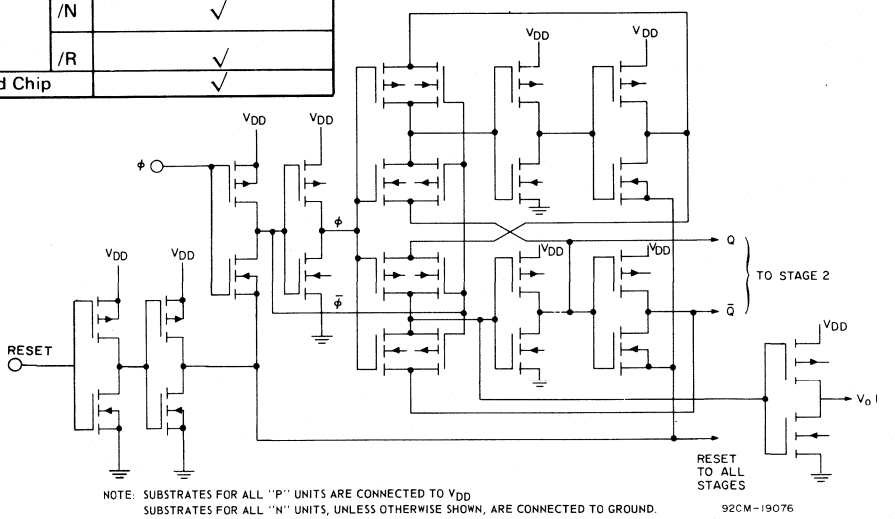


Fig. 2—Schematic diagram (pulse shaper and 1 binary stage).

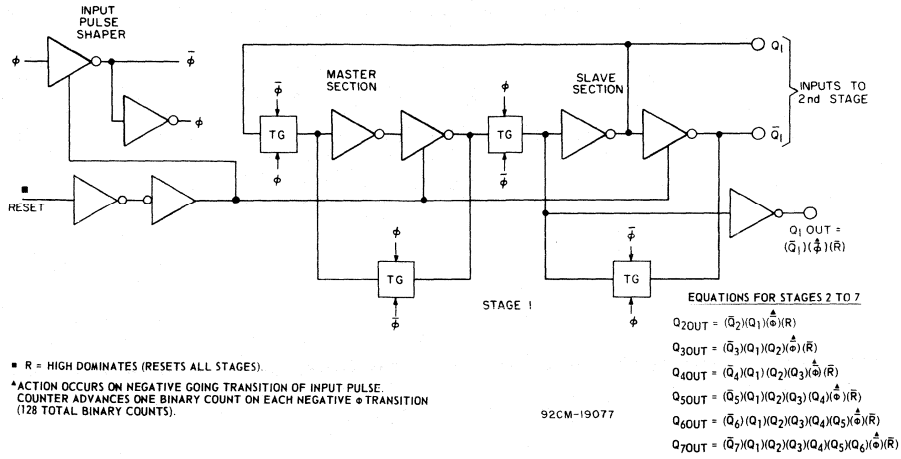


Fig. 3—Logic block diagram (pulse shaper and 1 binary stage).

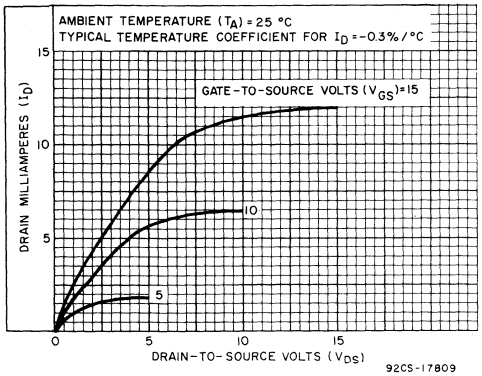


Fig. 4—Typ. N-channel drain characteristics.

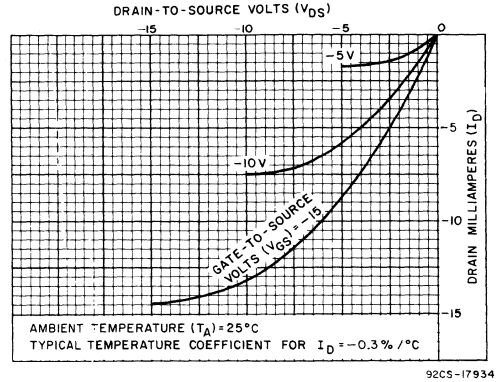


Fig. 5—Typ. P-channel drain characteristics.

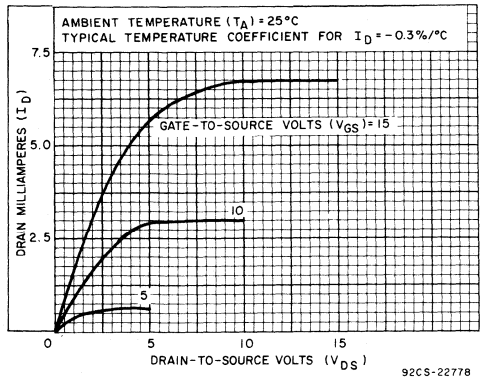


Fig. 6—Min. N-channel drain characteristics.

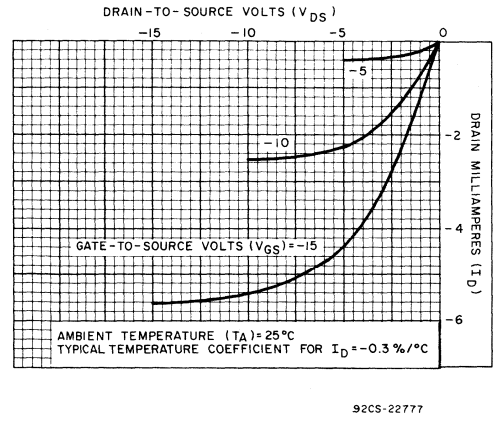


Fig. 7—Min. P-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4024AD, CD4024AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.5	5	–	–	300	μA	12	2
			10	–	–	10.	–	1	10.	–	–	200.			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	2.5	25	–	–	1500	μW	–	
			10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}	0	3	–	–	0.55.	–	–	0.5.	–	–	–	V		1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
		0	15	–	–	–	–	–	–	–	–	0.55.			
High-Level	V_{OH}	3	3	2.25.	–	–	2.3.	–	–	–	–	–	V		1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
		15	15	–	–	–	14.5.	–	–	14.45.	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = -20 μA		-0.7 •	-1.7	-3 •	-0.7 •	-1.5	-3 •	-0.3 •	-1.3	-3 •	V		2
P-Channel	V_{THP}	I_D = 20 μA		0.7 •	1.7	3•	0.7 •	1.5	3•	0.3 •	1.3	3 •	V		
Noise Immunity (All Inputs) *For Definition, See Appendix*	V_{NL}	0.8	5	1.5	–	–	1.5.	2.25	–	1.4.	–	–	V	13	1
		1.0	10	3.	–	–	3.	4.5	–	2.9.	–	–			
	V_{NH}	4.2	5	1.4	–	–	1.5.	2.25	–	1.5.	–	–	V	14	
		9.0	10	2.9.	–	–	3.	4.5	–	3.	–	–			
Output Drive Current: N-Channel	I_DN	0.5	5	0.31	–	–	0.25.	0.5	–	0.175	–	–	mA		2
		0.5	10	0.02	–	–	0.5.	1	–	0.35	–	–			
P-Channel	I_DP	4.5	5	-0.19	–	–	-0.15.	0.3	–	-0.105	–	–	mA		
		9.5	10	-0.45	–	–	-0.35.	-0.7	–	-0.25	–	–			
Diode Test 100 μA Test Pin	–			–	–	1.5.	–	–	1.5.	–	–	1.5.	V		3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or a one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

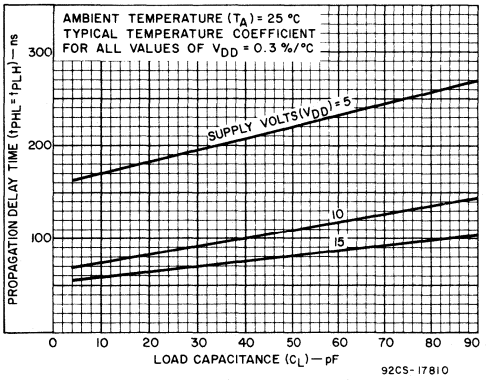


Fig. 8—Typ. propagation delay time vs. C_L.

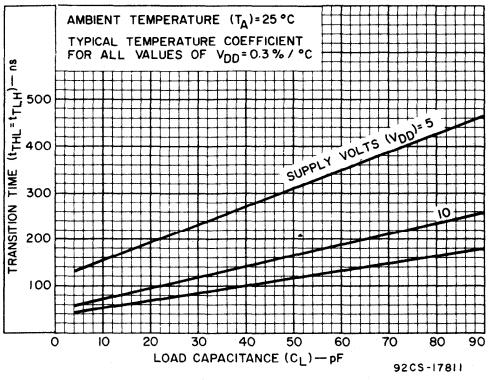


Fig. 9—Typ. transition time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = OV, C_L = 15pF, and input rise and fall times = 20ns, except $t_r\phi$ and $t_f\phi$. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4024AD, CD4024AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.			
ϕ INPUT OPERATION									
Propagation Delay Time*	t_{PHL}, t_{PLH}		5	–	175	350	ns	8	1
			10	–	80	125.			
Transition Time	t_{THL}, t_{TLH}		5	–	175	225	ns	9	1
			10	–	80	125.			
Minimum Input-Pulse Width	t_{WL}, t_{WH}		5	–	200	330	ns	–	
			10	–	140	125			
Input Pulse Rise & Fall Time	$t_r\phi$		5	–	–	15	µs	–	1
	$t_f\phi$		10	–	–	10.			
Maximum Input Pulse Frequency	$f\phi$		5	1.5	2.5	–	MHz	11	1
			10	4.	7	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	
RESET OPERATION									
Propagation Delay Time	$t_{PHL(R)}$		5	–	500	700	ns	–	
			10	–	250	350			
Minimum Reset Pulse Width	$t_{WH(R)}$		5	–	375	500	ns	–	
			10	–	200	300			

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is a one-input, one-output only. *Propagation delay time is from clock input to Q_1 output.

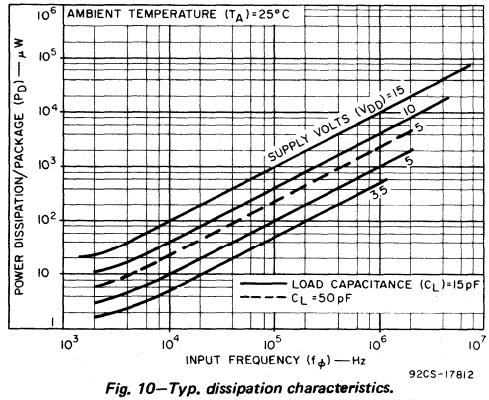


Fig. 10—Typ. dissipation characteristics.

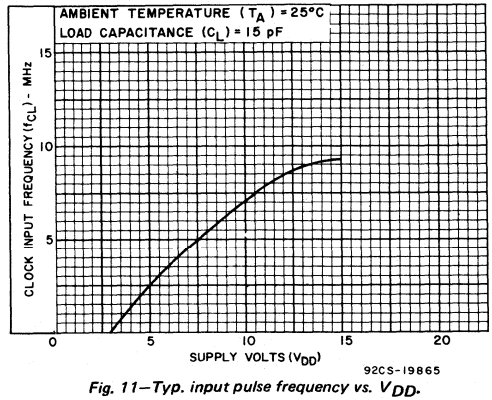


Fig. 11—Typ. input pulse frequency vs. V_{DD}.

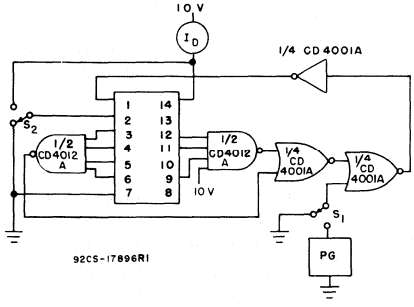


Fig. 12—Quiescent device current test circuit.

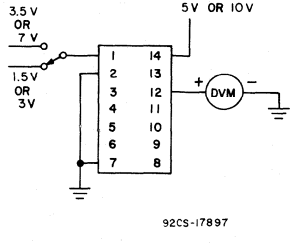


Fig. 13—Noise Immunity test circuit.

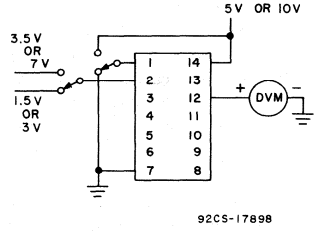


Fig. 14—Reset noise immunity test circuit.

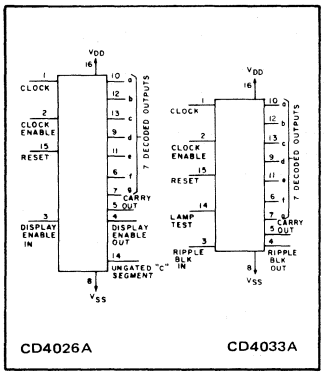
RCA Solid State Division

Digitial Integrated Circuits

Monolithic Silicon

High-Reliability 'Slash' (/) Series

CD4026A/... CD4033A/...



CD4026A CD4033A

High-Reliability COS/MOS Decade Counters/Dividers

With Decoded 7-Segment Display Outputs and:

Display Enable – CD4026A
Ripple Blanking – CD4033A

Special Features:

- **Counter and 7-segment decoding in one package**
- **Ideal for low-power displays**
- **Easily interfaced with 7-segment display types**
- **Fully static counter operation: DC to 2.5 MHz (typ.)**
- **Display Enable Output (CD4026A)**
- **"Ripple Blanking" and Lamp Test (CD4033A)**

RCA CD4026A and CD4033A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4026A and CD4033A each consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package counter are important.

Inputs common to both types are Clock, Reset, and Clock Enable; common outputs are carry out and seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026A include Display Enable input and Display Enable and Ungated "C-segment" outputs. Signals peculiar to the CD4033A are Ripple-Blanking and Lamp Test inputs and a Ripple-Blanking output.

A "high" Reset signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the Clock Enable signal is "low". Counter advancement via the clock line is inhibited when the Clock Enable signal is "high". Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (C_{out}) Signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multidecade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for

Applications:

- **Decade counting/7-segment decimal display**
- **Frequency division/7-segment decimal displays**
- **Clock/watches/timers (e.g. ÷ 60, ÷ 60, ÷ 12 counter/display)**
- **Counter/display driver for meter applications**

representing the decimal number 0 to 9. The 7-segment outputs go "high" on selection in the CD4033A; in the CD4026A these outputs go "high" only when the Display Enable IN is "high".

CD4026A

When the Display Enable IN is "low" the seven decoded outputs are forced "low" regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033A

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display, consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero

suppression on the integer side is obtained by connecting the RB1 terminal of the CD4033A associated with the most significant digit in the display to a "low-level" voltage and connecting the RB0 terminal of that stage to the RB1 of the CD4033A in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

On the fraction side of the display the RB1 of the CD4033A associated with the least significant bit is connected to a "low level" voltage and the RB0 of the CD4033A is connected to the RB1 terminal of the CD4033A in the next more-significant-bit position. Again, this procedure is continued for all CD4033A's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RB1 of that stage to a "high level" voltage (instead of the RB0 of the next more-significant-stage). For Example: optional zero → 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RB1 of the CD4033A associated with it to a "high level" voltage.

Ripple blanking of non-significant zeroes provides an appreciable savings in display power.

The CD4033A has a "Lamp Test" input which, when connected to a "high level" voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the "high" state.

These devices are electrically and mechanically identical with standard COS/MOS CD4026A and CD4033A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4026A and CD4033A "Slash" (/) Series can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /N, /R, and standard chip.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to high-reliability report RIC-102B, "High-Reliability COS/MOS CD4000A Series Types".

The CD4026A and CD4033A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4022AD, CD4022AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4022AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

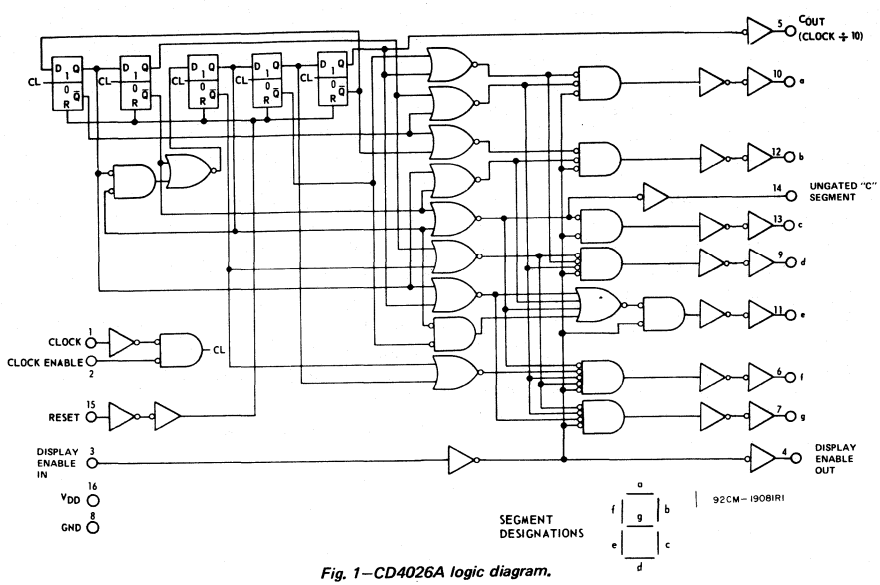


Fig. 1–CD4026A logic diagram.

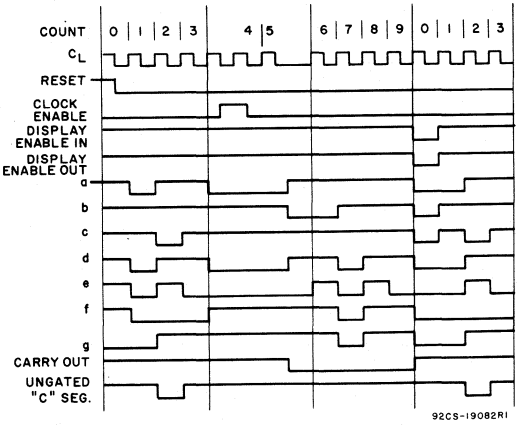


Fig. 2–CD4026A timing diagram.

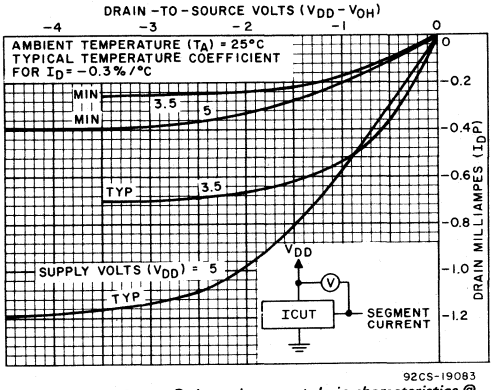


Fig. 3–Min. & typ. P-channel segment drain characteristics @ V_{DD} = 3.5 & 5 V.

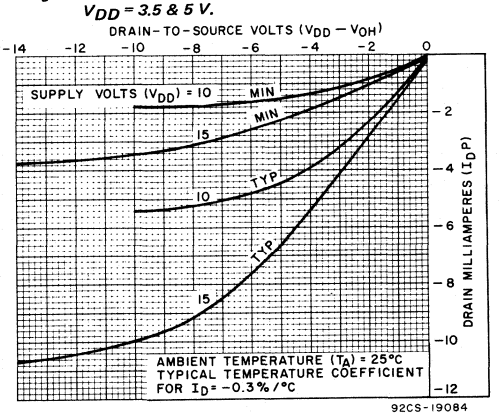


Fig. 4–Min. & typ. P-channel segment drain characteristics @ V_{DD} = 10 & 15 V.

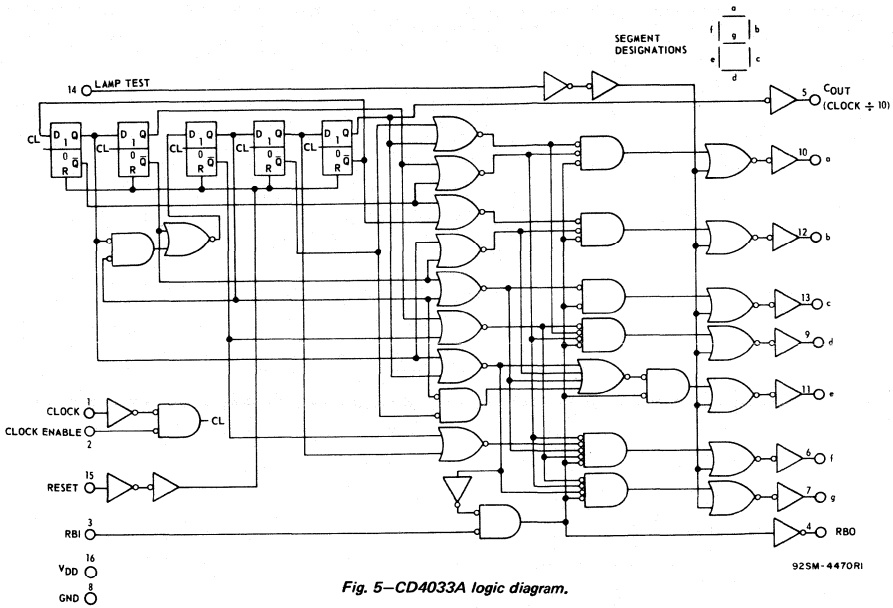


Fig. 5—CD4033A logic diagram.

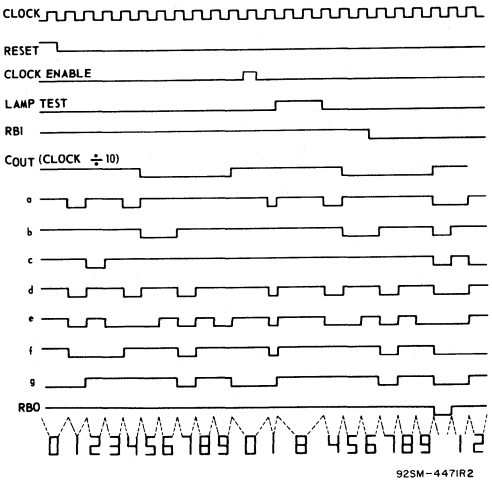


Fig. 6—CD4033A timing diagram.

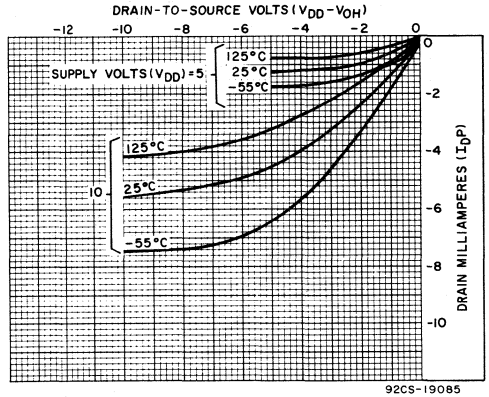


Fig. 7—Typ. P-channel drain characteristics at a function of temp.

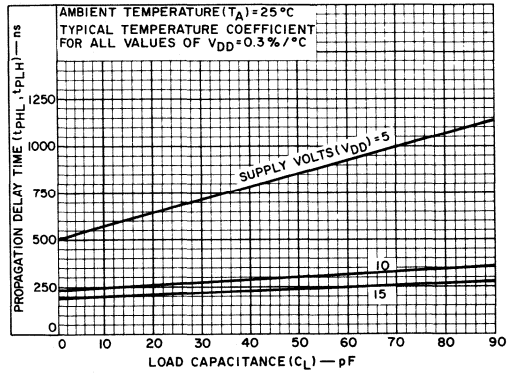


Fig. 8—Typ. propagation delay time vs. C_L for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
					CD4026AD, CD4026AK CD4033AD, CD4033AK											
			V_O Volts	V_{DD} Volts	−55°C			25°C			125°C					
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig. No.	
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	μA	14	1
				10	–	–	10.	–	1	10.	–	–	200.			
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	μW	–	
				10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55.	–	–	0.5.	–	–	–	V		1
				5	–	–	0.01	–	0	0.01	–	–	0.05			
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.5.	–	–	0.55.			
High-Level	V_{OH}			3	2.25.	–	–	2.3.	–	–	–	–	–	V		1
				5	4.99	–	–	4.99	5	–	4.95	–	–			
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.5.	–	–	14.45.	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = -10 μA			-0.7.	-1.7	-3.	-0.7.	-1.5	-3.	-0.3.	-1.3	-3.	V		2
P-Channel	V_{THP}	I_D = 10 μA			0.7.	1.7	3.	0.7.	1.5	3.	0.3.	1.3	3.	V		
Noise Immunity (All Inputs) *For Definition, See Appendix in SSD-207*	V_{NL}		0.8	5	1.5	–	–	1.5.	2.25	–	1.4	–	–	V		
			1.0	10	3.	–	–	3.	4.5	–	2.9.	–	–			
	V_{NH}		4.2	5	1.4	–	–	1.5.	2.25	–	1.5	–	–	V	15	1
			9.0	10	2.9.	–	–	3.	4.5	–	3.	–	–			
Output Drive Current - N-Channel	I_DN	Decoded Outputs	0.5	5	0.15	–	–	0.12.	0.24	–	0.09	–	–	mA		2
			0.5	10	0.32	–	–	0.25.	0.5	–	0.18	–	–			
		Carry Output	0.5	5	0.12	–	–	0.15	0.4	–	0.1	–	–			
			0.5	10	0.45	–	–	0.35	1	–	0.25	–	–			
P-Channel	I_DP	Decoded Outputs	4.5	5	-0.21	–	–	-0.14.	0.28	–	-0.1	–	–	mA	3, 4, 7	2
			9.5	10	-0.45	–	–	-0.3.	-0.6	–	-0.22	–	–			
		Carry Output	4.5	5	-0.12	–	–	-0.15	-0.4	–	-0.1	–	–			
			9.5	10	-0.45	–	–	-0.35	-1	–	-0.25	–	–			
Diode Test 100 μA	–	–			–	–	1.5.	–	–	1.5.	–	–	1.5.	V		3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.
For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V_{SS} = OV, C_L = 15pF, and input rise and fall times - 20 ns, except t_rCL and t_fCL. Typical Temperatuer Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4026AD, CD4025AK CD4033AD, CE4033AK			UNITS	CHARACTERISTIC CURVE & TEST CIRCUITS Fi. No.	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.			
CLOCKED OPERATION									
Propagation Delay Time: Carry Out Line	t_{PHL}		5	–	350	1000	ns	9	1
			10	–	125	250•			
Decode Out Lines	t_{PLH}		5	–	600	1700	ns	8	
			10	–	250	500			
Transition Time: Carry Out Line	t_{THL}		5	–	100	300	ns	11	
			10	–	50	150			
Decode Out Lines	t_{TLH}		5	–	300	900	ns	10	
			10	–	125	350			
Minimum Clock Pulse Width	t_{WL} t_{WH}		5	–	200	300	ns	–	
			10	–	100	170			
Clock Rise & Fall Time	t_rCL* t_fCL		5	–	–	15	μs	–	1
			10	–	–	15•			
Clock Enable Set-Up Time			5	–	175	500	ns	–	
			10	–	75	200			
Maximum Clock Frequency	f_{CL}	Measured with Respect to Carry Out Line	5	1.5	2.5	–	MHz	12	1
			10	3•	5	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	
RESET OPERATION									
Propagation Delay Time: To Carry Out Line	$t_{PHL(R)}$		5	–	350	1000	ns	–	1
			10	–	125	125			
To Decode Out Lines			5	–	550	1400	ns	–	
			10	–	240	500			
Reset Pulse Width	$t_{WH(R)}$		5	–	200	330	ns	–	
			10	–	100	165			
Reset Removal Time			5	–	300	750	ns	–	
			10	–	100	225			

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

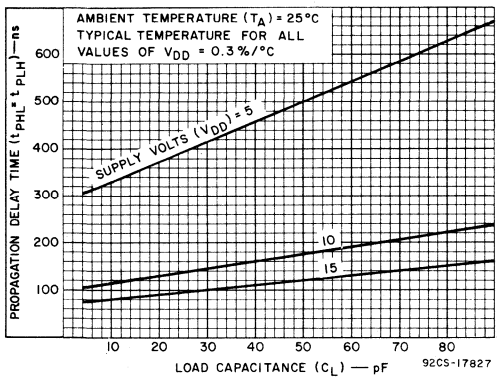


Fig. 9—Typ. propagation delay time vs. C_L for carry outputs.

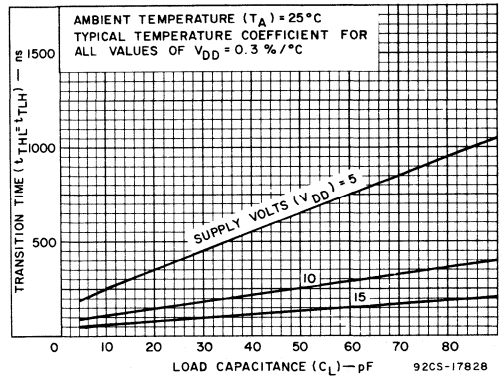


Fig. 10—Typ. transition time vs. C_L for decoded outputs.

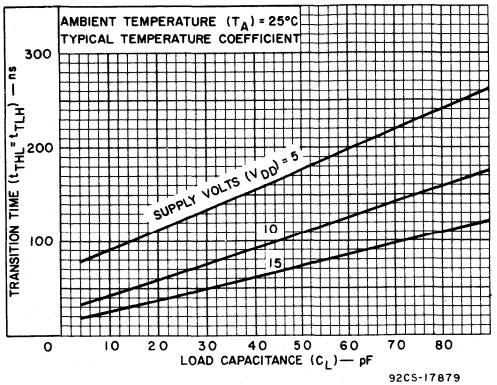


Fig. 11—Typ. transition time vs. C_L for carry output

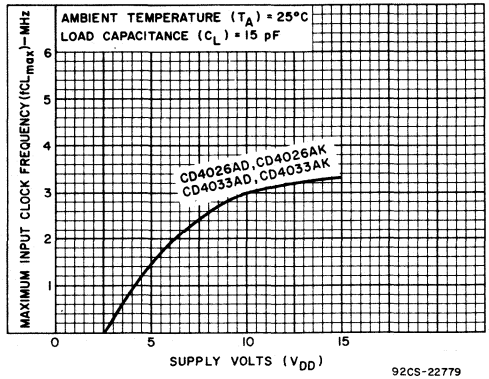


Fig. 12—Max. input clock frequency vs. V_{DD}.

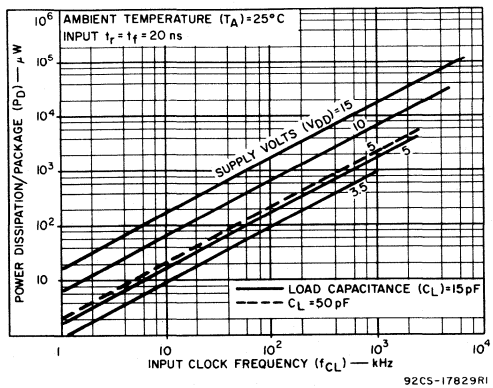


Fig. 13—Typ. dissipation characteristics.

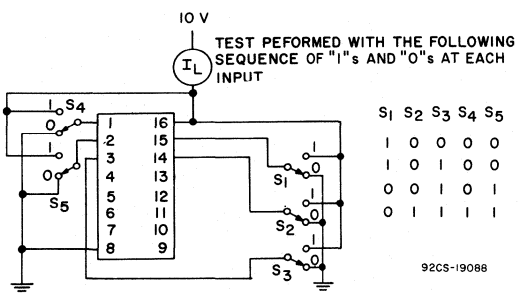


Fig. 14—Quiescent device current test circuit.

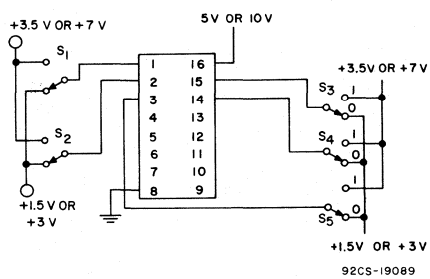


Fig. 15—Noise immunity test circuit.

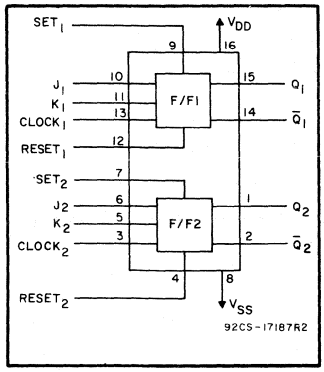
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4027A/...



High-Reliability COS/MOS Dual J-K Master-Slave Flip Flop

With Set/Reset Capability
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

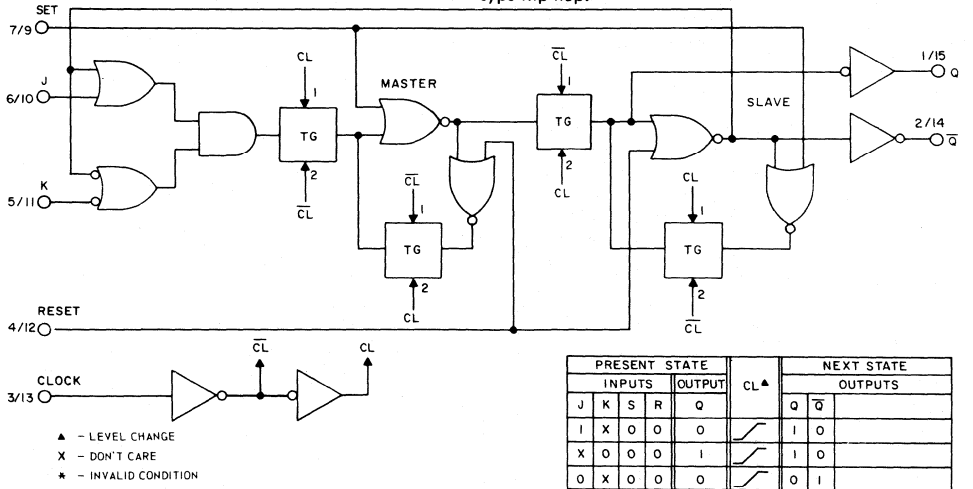
Special Features:

- **Static flip-flop operation.....retains state indefinitely with clock level either "high" or low"**
- **Medium speed operation.....8 MHz (typ.) clock toggle rate at $V_{DD}-V_{SS}$ = 10 V**
- **Low "high"-and "low" output impedance.....700Ω and 300Ω, respectively, at $V_{DD}-V_{SS}$ = 10 V**

Applications:

- **Registers, counters, control circuits**

RCA CD4027A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4027A is a single monolithic chip integrated circuit containing two identical complementary-symmetry "J-K" master-slave flip-flops. Each flip-flop has provisions for individual "J" "K", "Set", "Reset", and "Clock" input signals. Buffered "Q" and "Q" signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA CD4013A dual "D" type flip-flop.



PRESENT STATE						NEXT STATE	
INPUTS				OUTPUT	CL▲	OUTPUTS	
J	K	S	R	Q		Q	Q̄
1	X	0	0	0	⌐	1	0
X	0	0	0	1	⌐	1	0
0	X	0	0	0	⌐	0	1
X	1	0	0	1	⌐	0	1
X	X	0	0	X	⌐		← NO CHANGE
X	X	1	0	X	X	1	0
X	X	0	1	X	X	0	1
X	X	1	1	X	X	*	*

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

92CM-17188R2

Fig. 1—Logic diagram & truth table for one of two identical J-K flip flops.

The CD4027A is useful in performing control, register, and toggle functions. Logic levels present at the "J" and "K" inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the "clock" pulse. Set and reset functions are independent of the clock and are initiated when a "high"-level signal is present at either the "Set" or "Reset" input.

These devices are electrically and mechanically identical to standard COS/MOS CD4027A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA High-Reliability "Slash" (/) series, RCA will offer these circuits screened to MIL-M-38510 as described in RIC-104, "MIL-M-38510 COS/MOS CD4000A Series types."

RCA Designation	MIL-M-38510 Designation
CD4027A	MIL-M-38510/05102

The packaged types in the CD4027A "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /N, /R, and standard chip.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to high-reliability report RIC-102B, "High-Reliability COS/MOS CD4000A Series Types".

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4027AD, CD4027AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4027AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

The CD4027A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended	
DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended	
Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering)	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A, D, /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A, H, /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... **3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4027AD, CD4027AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	1	–	0.005	1	–	–	60	μA	12	1
			10	–	–	2●	–	0.005	2●	–	–	40●			
Quiescent Device Dissipation/Package	P_D		5	–	–	5	–	0.025	5	–	–	300	μW	–	–
			10	–	–	20	–	0.05	20	–	–	400			
Output Voltage Low-Level	V_{OL}		3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	1445●	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = -10 μA		-0.7●	-1.7	-3●	-0.7●	-1.5	-3●	-0.3●	-1.3	-3●	V	–	2
P-Channel	V_{THP}	I_D = 10 μA		0.7●	1.7	3●	0.7●	1.5	3●	0.3	1.3	3●	V		
Noise Immunity (All Inputs) *For Definition, See Appendix*	V_{NL}	0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	13	1
		1.0	10	3●	–	–	3●	4.5	–	2.9●	–	–			
	V_{NH}	4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		9.0	10	2.9●	—	—	3●	—	—	3●	—	—			
Output Drive Current: N-Channel	I_{DN}	0.5	5	0.63	–	–	0.5●	1	–	0.33	–	–	mA	2, 4	2
		0.5	10	1.25	–	–	0.25●	2.5	–	0.7	–	–			
P-Channel	I_{DP}	4.5	5	-0.31	–	–	-0.25●	-0.5	–	-0.175	–	–	mA	3, 5	
		9.5	10	-0.8	–	–	-0.3●	-1.3	–	-0.45	–	–			
Diode Test 100 μA Test Pin	–			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

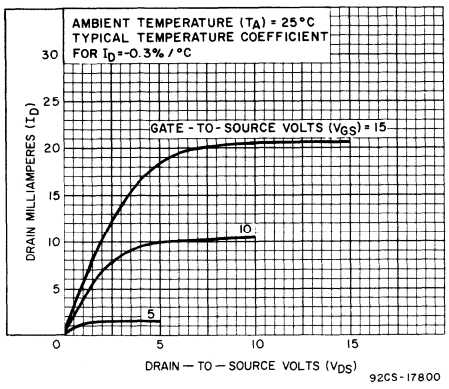


Fig. 2—Typ. N-channel drain characteristics.

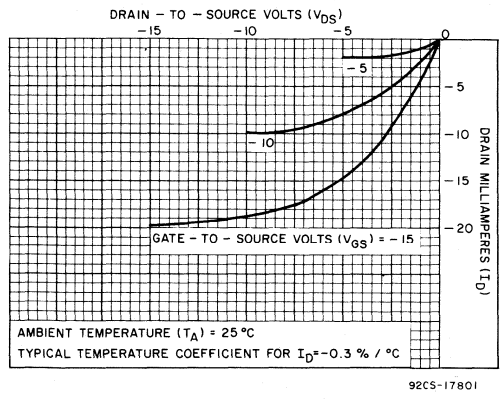


Fig. 3—Typ. P-channel drain characteristics.

Dynamic Electrical Characteristics at T_A = 25°C, V_{SS} = OV, C_L = 15pF, and input rise and fall times = 20 ns, except t_rCL and t_fCL. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
			CD4027AD, CD4027AK					
		V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	150	300	ns	7	1
		10	–	75	110•			
Transition Time	t_{THL}, t_{TLH}	5	–	75	125	ns	8	–
		10	–	50	70			
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	165	330	ns	–	
		10	–	65	110			
Clock Rise & Fall Time	*t_rCL, t_fCL	5	–	–	15	μs	–	1
		10	–	–	5•			
Set-Up Time		5	–	70	150	ns	–	–
		10	–	25	50			
Maximum Clock Frequency (toggle mode)	fCL	5	1.5	3	–	MHz	9	1
		10	4.5•	8	–			
Input Capacitance	C_I	–	–	5	–	pF	–	–
SET & RESET OPERATION								
Propagation Delay Time	$t_{PHL(R)}$, $t_{PLH(S)}$	5	–	175	225	ns	–	–
		10	–	75	110			
Minimum Set and Reset Pulse Widths	$t_{WH(S)}$, $t_{WL(R)}$	5	–	125	200	ns	–	
		10	–	50	80			

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
NOTE 1: Test is a one input one output only.

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

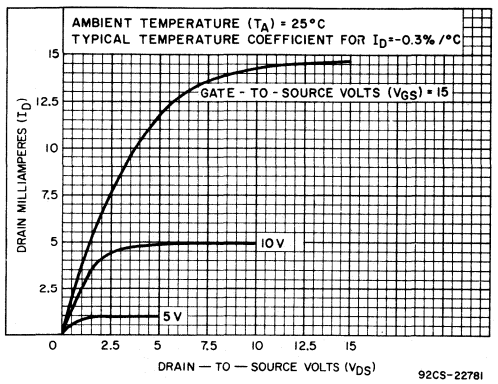


Fig. 4—Min. N-channel drain characteristics.

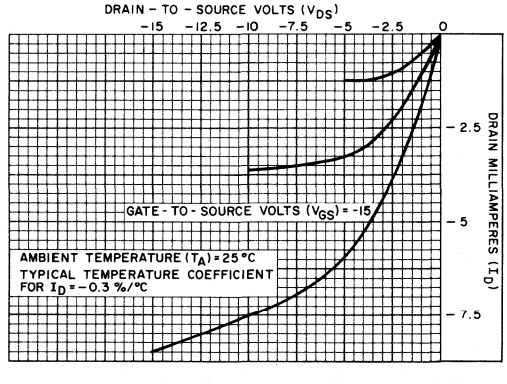


Fig. 5—Min. P-channel drain characteristics.

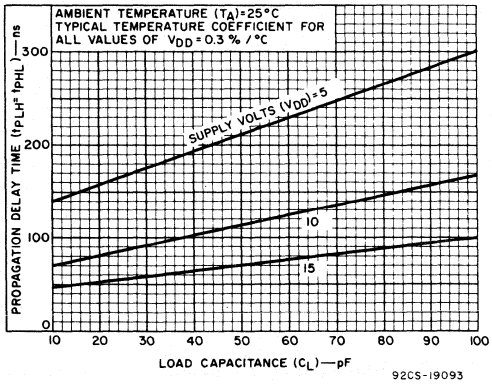


Fig. 6—Typ. propagation delay time vs. C_L.

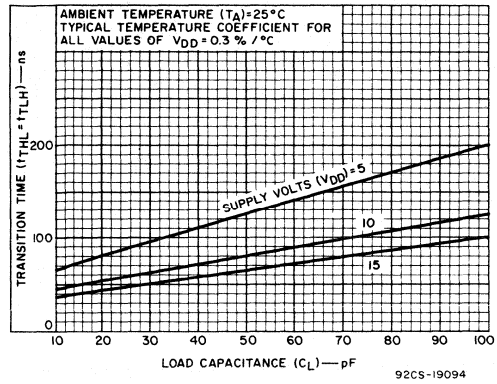


Fig. 7—Typ. transition time vs. C_L.

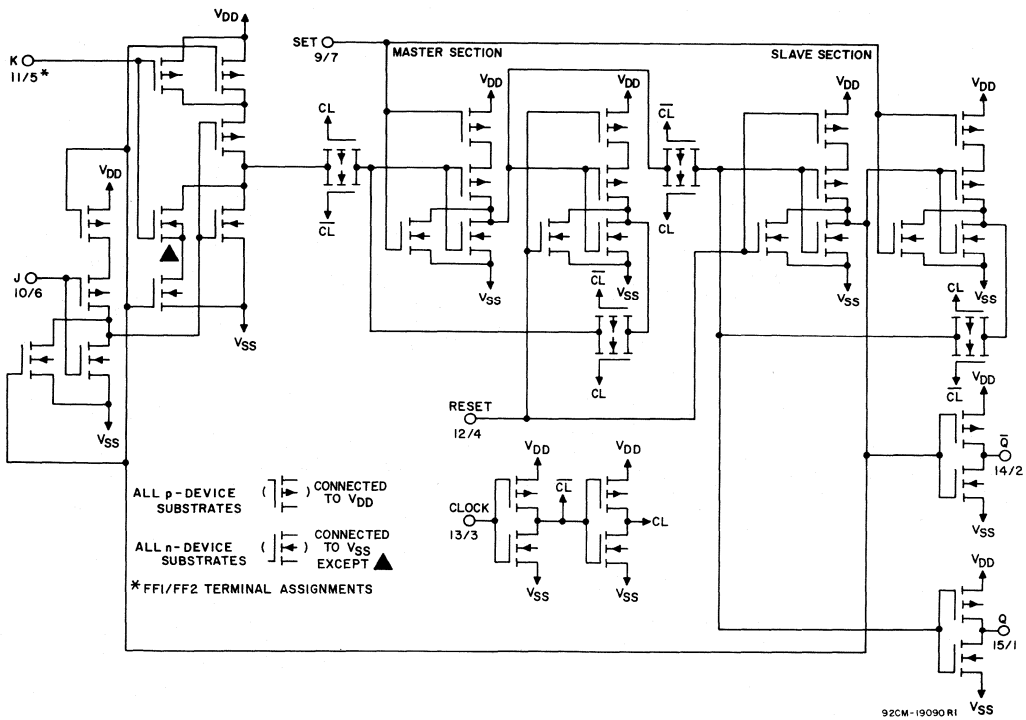


Fig. 8—Schematic diagram for one of two identical J-K flip flops.

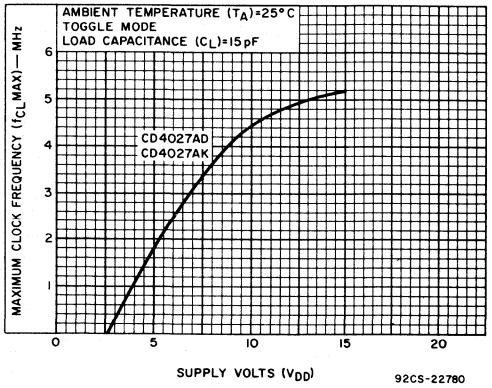


Fig. 9—Max. clock frequency vs. supply voltage.

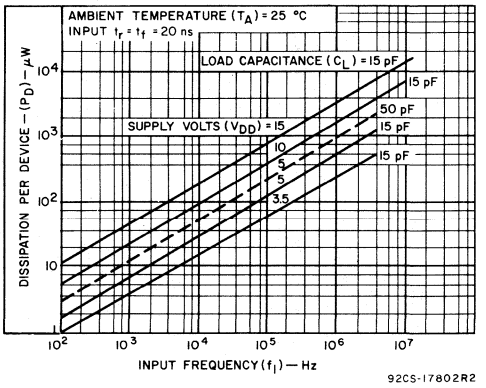


Fig. 10—Typ. dissipation characteristics.

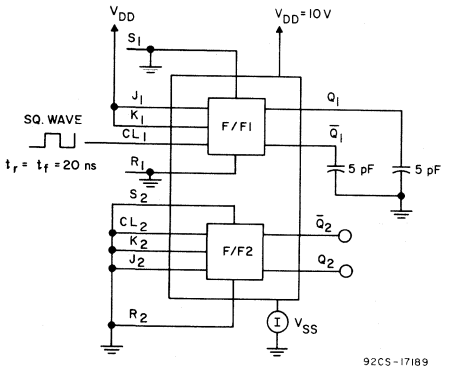
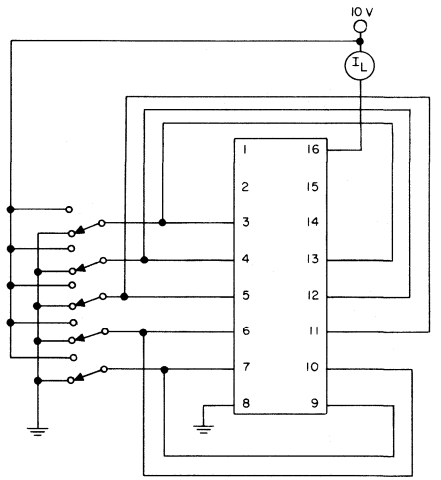


Fig. 11—Dissipation test circuit.



TEST PERFORMED WITH THE FOLLOWING LOGIC LEVELS PRESENT

CL	J	K	S	R
0	1	1	0	1
0	0	0	1	1
0	0	0	1	0
1	0	0	1	0

92CS-19096

Fig. 12—Quiescent device current test circuit.

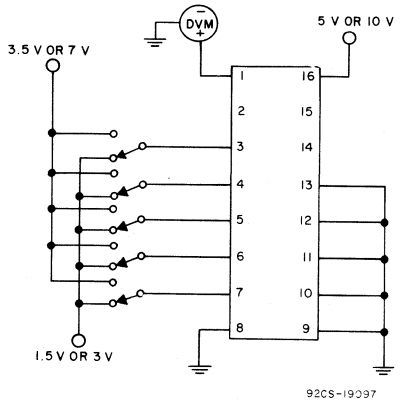


Fig. 13—Noise-immunity test circuit.

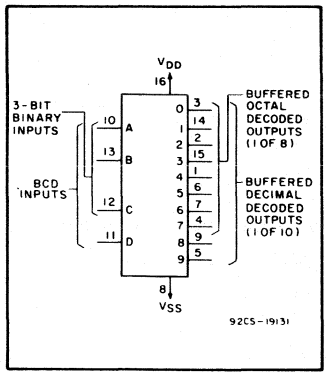
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4028A/...



High-Reliability

COS/MOS BCD-to-Decimal Decoder

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **BCD to decimal decoding or binary to octal decoding**
- **High decoded output drive capability. . . . . .8 mA (typ.) sink or source**
- **"Positive Logic" inputs and outputs. . . . . .decoded outputs go "high" on selection**
- **Medium speed operation. . . . . .t_{THL}, t_{TLH} = 30 ns (typ.) @ V_{DD} = 10 V**

Applications:

- **Code conversion**
- **Indicator-tube decoder**
- **Address decoding—memory selection control**

RCA CD4028A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a "high" level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A "high"-level signal at the D input inhibits octal decoding and causes inputs 0 through 7 to go "low". If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications. All inputs and outputs are protected against electrostatic effects.

These devices are electrically and mechanically identical with standard COS/MOS CD4028A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical,

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

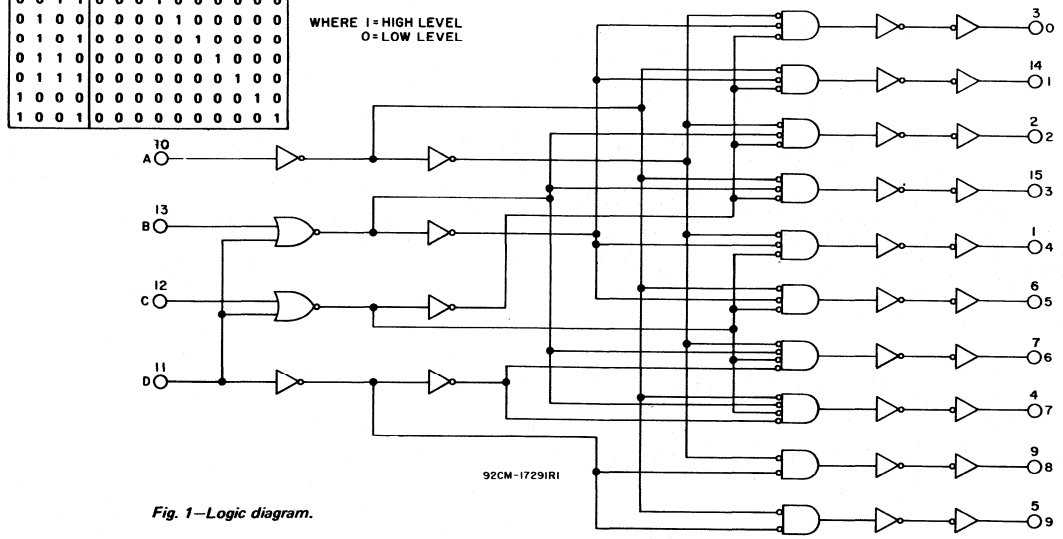


Fig. 1—Logic diagram.

mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4028A "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /N, /R, and standard chip.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to high-reliability report RIC-102B, "High-Reliability COS/MOS CD4000A Series Types".

The CD4028A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4028AD, CD4028AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4028AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

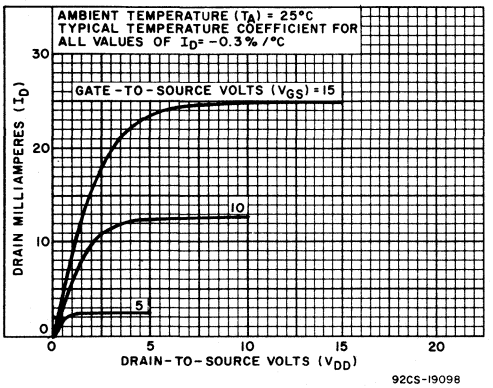


Fig. 2–Typ. N-channel drain characteristics.

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

	CD4000A	D	/1N
		Package Suffix Letter	Screening Level
Type Designation		D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

	CD4000A	H	/N
		Package Suffix Letter	Screening Level
Type Designation		H = Chip Version	/N /R

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4028AD, CD4028AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.5	5	–	–	300	μA	8	1
			10	–	–	10.	–	1	10.	–	–	200.			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	2.5	25	–	–	1500	μW	–	
			10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}		3	–	–	0.55.	–	–	0.5.	–	–	–	V		1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5.	–	–	0.55.			
High-Level	V_{OH}		3	2.25.	–	–	2.3.	–	–	–	–	–	V		1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5.	–	–	14.45.	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = -20 μA		-0.7.	-1.7	-3.	-0.7.	-1.5	-3.	-0.3.	-1.3	-3.	V		2
P-Channel	V_{THP}	I_D = 20 μA		0.7.	1.7	3.	0.7.	1.5	3.	0.3.	-1.3	3.	V		
Noise Immunity (All Inputs) *For Definition, See Appendix*	V_{NL}	0.8	5	1.5	–	–	1.5.	2.25	–	1.4	–	–	V		
		1.0	10	3.	–	–	3.	4.5	–	2.9.	–	–			
	V_{NH}	4.2	5	1.4	–	–	1.5.	2.25	–	1.5	–	–	V	9	1
		9.0	10	2.9.	–	–	3.	4.5	–	3.	–	–			
Output Drive Current N-Channel	I_DN	0.5	5	0.75	–	–	0.6.	1.2	–	0.45	–	–	mA	2	2
		0.5	10	1.5	–	–	1.2.	2.4	–	0.9	–	–			
P-Channel	I_DP	4.5	5	-0.7	–	–	-0.37.	-0.9	–	-0.32	–	–	mA	3	
		9.5	10	-1.4	–	–	-0.9.	-1.9	–	-0.65	–	–			
Diode Test 100 μA Test Pin	–		–	–	–	1.5.	–	–	1.5.	–	–	1.5.	V		3
Input Current	I_I		–	–	–	–	–	10	–	–	–	–	pA		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

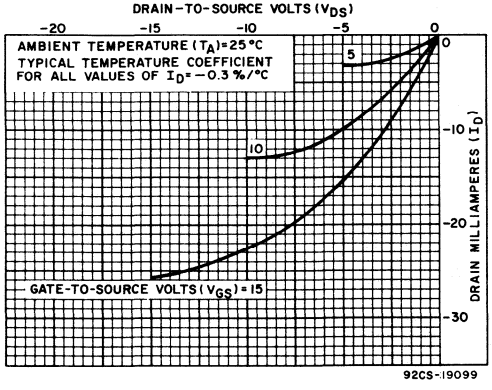


Fig. 3—Typ. P-channel drain characteristics.

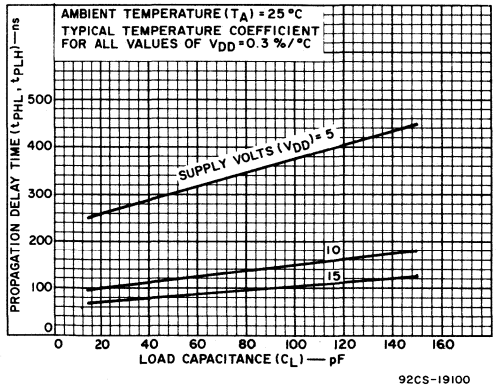


Fig.4—Typ. propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = OV, C_I = 15pF, and all input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
				CD4028AD, CD4028AK					
			V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	250	480	ns	6	1
			10	–	100	180.			
Transition Time	t_{THL}, t_{TLH}		5	–	60	150	ns	5	1
			10	–	30	75.			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
NOTE 1: Test is a one-input, one output only.

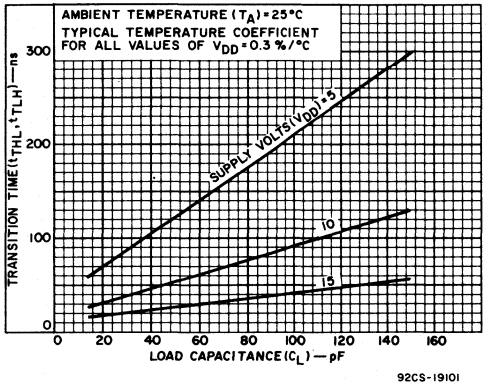


Fig. 5—Typ. transition time vs. C_L.

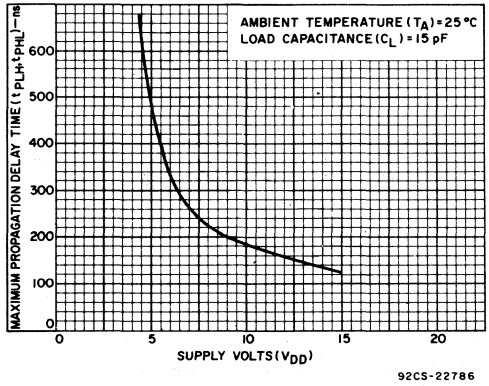


Fig. 6—Max. propagation delay time vs. V_{DD}.

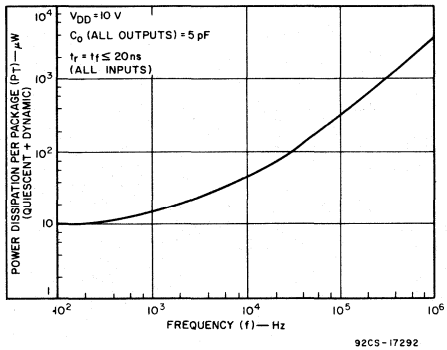


Fig. 7—Dissipation vs. input frequency.

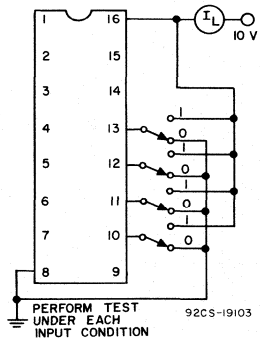


Fig. 8—Quiescent device current test circuit.

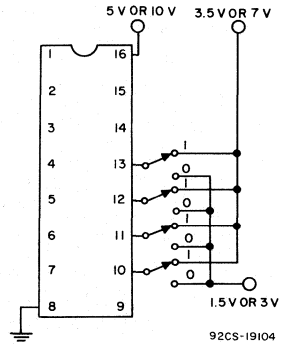


Fig.9 – Noise-immunity test circuit.

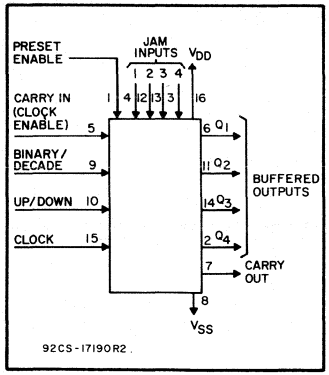
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4029A/...



High-Reliability COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Medium speed operation. . . . 5 MHz (typ.) @ C_L = 15 pF and $V_{DD}-V_{SS}$ = 10 V**
- **Multi-package parallel clocking for synchronous high speed output response of ripple clocking for slow clock input rise and fall times**
- **"Preset Enable" and individual "Jam" inputs provided**
- **Binary or decade up/down counting**
- **BCD outputs in decade mode**

Applications:

- **Programmable binary and decade counting/frequency synthesizers-BCD output**
- **Analog to digital and digital to analog conversion**
- **Up/Down binary counting**
- **Up/Down decade counting**
- **Magnitude and sign generation**
- **Difference counting**

RCA CD4029A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4029A types consist of a four-stage binary or BCD decade up/down counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Binary/Decade, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-Out signal are provided as outputs.

A "high" Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the clock. A "low" on each Jam line, when the Preset-Enable signal is "high", resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the Carry-In and Preset-Enable signals are "low". Advancement is inhibited when the Carry-In or Preset-Enable signals are "high". The Carry-Out signal is normally "high" and goes "low" when the counter reaches its maximum count in the "Up" mode or the minimum count in the "Down" mode provided the Carry-In signal is "low". The Carry-In signal in the "low" state can thus be considered a Clock Enable. The Carry-In terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the Binary/Decade input is "high"; the counter counts in the Decade mode when the Binary/Decade input is "low". The counter counts "Up" when the Up/Down input is "high", and "Down" when the Up/Down input is "low". Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 10. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

These devices are electrically and mechanically identical with standard COS/MOS CD4029A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4029A "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to Three screening levels – /N, /R, and standard chip.

For a description of the screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".

The CD4029A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4029AD, CD4029AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4029AH,	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

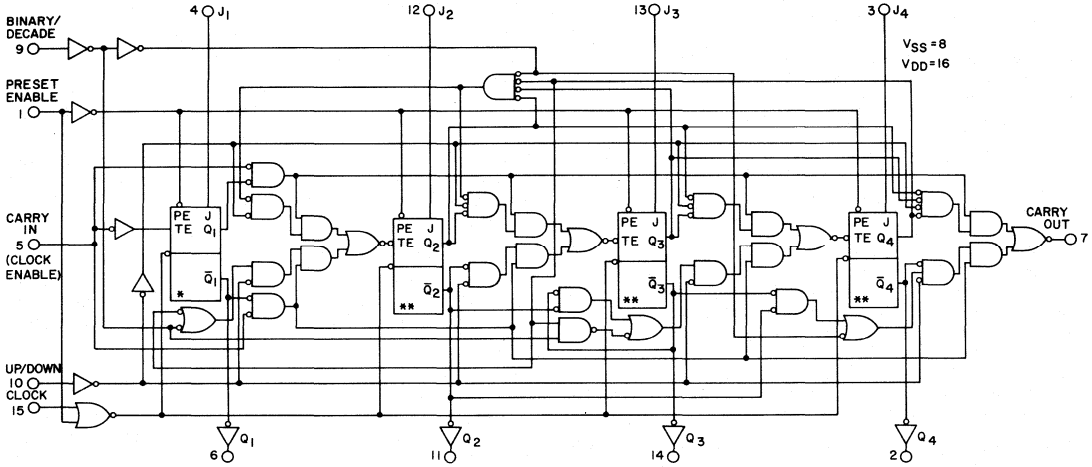
CD4000A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

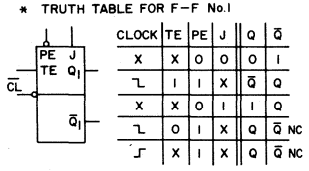
Chip Version, CD4000AH/N

CD4000A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

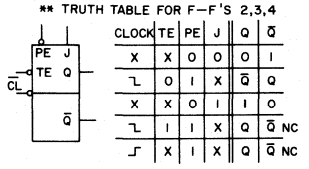


* TRUTH TABLE FOR F–F No.1



CLOCK	TE	PE	J	Q	Q̄
X	X	0	0	0	1
⌞	1	1	X	Q̄	Q
X	X	0	1	1	Q
⌞	0	1	X	Q	Q̄ NC
⌜	X	1	X	Q	Q̄ NC

** TRUTH TABLE FOR F–F'S 2,3,4



CLOCK	TE	PE	J	Q	Q̄
X	X	0	0	0	1
⌞	0	1	X	Q̄	Q
X	X	0	1	1	0
⌞	1	1	X	Q	Q̄ NC
⌜	X	1	X	Q	Q̄ NC

NC–NO CHANGE TE–TOGGLE ENABLE X–DON'T CARE

92CL-17191R1

Fig. 1–Logic diagram.

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
CARRY IN (CI) (CLOCK ENABLE)	1	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION
	0	ADVANCE COUNTER AT POS. CLOCK TRANSITION

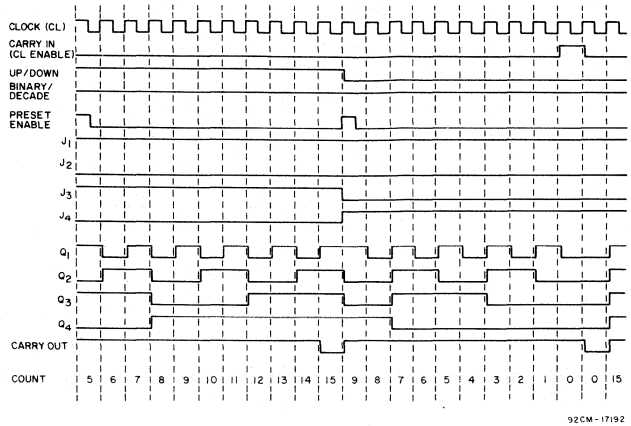


Fig. 2—Timing diagram-binary mode.

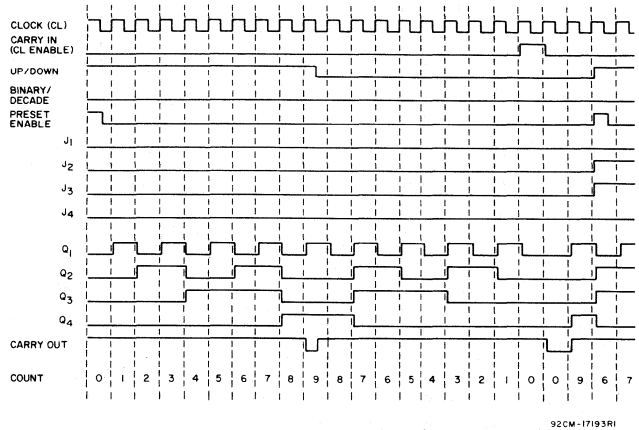


Fig. 3—Timing diagram-decade mode.

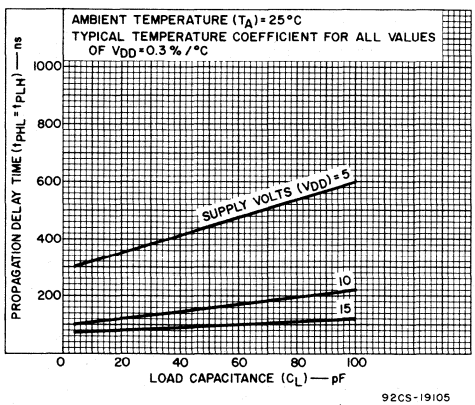


Fig. 4—Typ. propagation delay time vs. C_L for Q outputs.

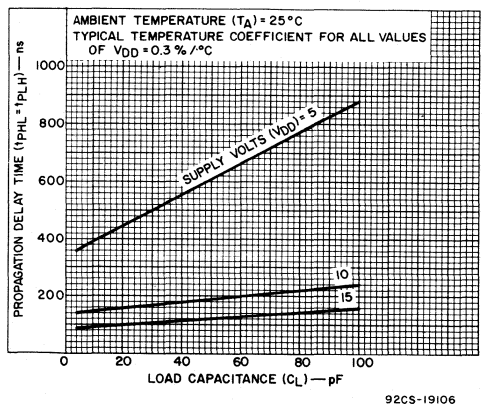


Fig. 5—Typ. propagation delay time vs. C_L for carry output.

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
					CD4029AD, CD4029AK											
					−55°C			25°C			125°C					
		V_O Volts		V_{DD} Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	μA	13	1
				10	–	–	10.	–	1	10.	–	–	200.			
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	μW		
				10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55.	–	–	0.5.	–	–	–	V		1
				5	–	–	0.01	–	0	0.01	–	–	0.05			
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.5.	–	–	0.55.			
High-Level	V_{OH}			3	2.25.	–	–	2.3.	–	–	–	–	–	V		1
				5	4.99	–	–	4.99	5	–	4.95	–	–			
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.5.	–	–	14.45.	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = -20 μA			-0.7.	-1.7	-3.	-0.7.	-1.5	-3.	-0.3.	-1.3	-3.	V		2
P-Channel	V_{THP}	I_D = 20 μA			0.7.	1.7	3.	0.7.	1.5	3.	0.3.	1.3	3.	V		
Noise Immunity (All Inputs) *For Definition, See Appendix*	V_{NL}		0.8	5	1.5	–	–	1.5.	2.25	–	1.4	–	–	V	14	1
			1.0	10	3.	–	–	3.	4.5	–	2.9.	–	–			
	V_{NH}		4.2	5	1.4	–	–	1.5.	2.25	–	1.5	–	–	V		
			9.0	10	2.9.	–	–	3.	4.5	–	3.	–	–			
Output Drive Current N-Channel	I_DN	Q Out-puts	0.5	5	0.5	–	–	0.4.	0.15	–	0.28	–	–	mA		1
			0.5	10	0.74	–	–	0.6.	0.3	–	0.42	–	–			
		Carry Out-puts	0.5	5	0.1	–	–	0.08.	0.5	–	0.06	–	–			
			0.5	10	0.4	–	–	0.32.	1	–	0.22	–	–			
P-Channel	I_DP	Q Out-put	4.5	5	-0.18	–	–	-0.12.	-0.075	–	-0.08	–	–	mA		
			9.5	10	-0.3	–	–	-0.2.	-0.15	–	-0.14	–	–			
		Carry Out-put	4.5	5	-0.09	–	–	-0.06.	-0.4	–	-0.04	–	–			
			9.5	10	-0.15	–	–	-0.1.	-0.8	–	-0.01	–	–			
Diode Test 100 μA Test Pin	–				–	–	1.5.	–	–	1.5.	–	–	1.5.	V	–	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–	

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or a one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

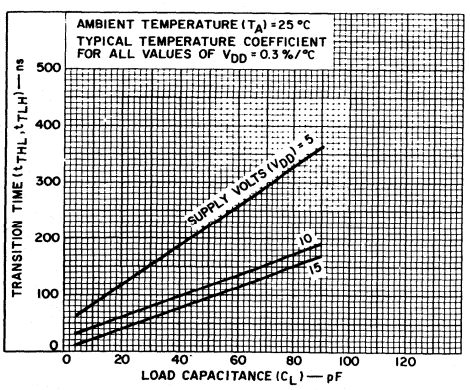


Fig. 6—Typ. transition time vs. C_L for Q outputs.

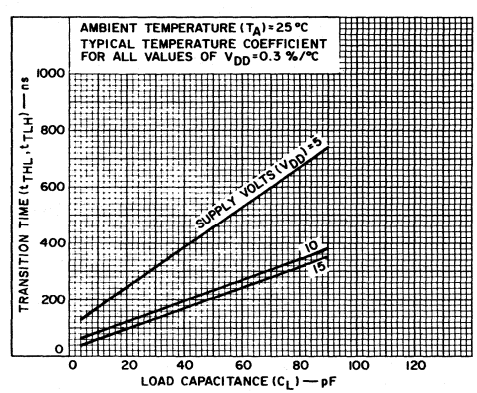


Fig. 7—Typ. transition time vs. C_L for carry output.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = OV, C_L = 15 pF, and input rise and fall times = 20 ns, except t_rCL and t_fCL Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS CD4029AD, CD4029AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.			
CLOCKED OPERATION									
Propagation Delay Time: Q Outputs	t_{PHL}, t_{PLH}		5	–	325	650	ns	4	1
			10	–	115	230●			
Carry Output			5	–	425	850	ns	5	1
			10	–	150	300●			
Transition Time: Q Outputs	t_{THL}, t_{TLH}		5	–	100	200	ns	6	–
			10	–	50	100			
Carry Output			5	–	200	400	ns	7	–
			10	–	100	200			
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	340	ns	–	–
			10	–	100	170			
Clock Rise & Fall Time	t_rCL, ▲ t_fCL		5	–	–	15	μs	–	–
			10	–	–	15●			
Set-Up Times*	t_{SHL}, t_{SLH}		5	–	325	650	ns	–	–
			10	–	115	230			
Maximum Clock Frequency	f_{CL}		5	1.5	2.5	–	MHz	8	–
			10	3●	5	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–
PRESET ENABLE									
Propagation Delay Time: Q Outputs	t_{PHL}, t_{PLH}		5	–	325	650	ns	–	–
			10	–	115	230			
Carry Output			5	–	425	850	ns	–	–
			10	–	150	300			
Reset Enable Pulse Width	t_{WH}		5	–	115	330	ns	–	–
			10	–	80	160			
Preset Enable Removal Time	t_{rem}		5	–	325	650	ns	–	–
			10	–	115	230			
CARRY INPUT									
Propagation Delay Time: Carry Output	t_{PHL}, t_{PLH}		5	–	175	350	ns	–	–
			10	–	50	100			

*From Up/Down, Binary/Decade or Carry Input Control Inputs to Clock Input.
▲ If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimate capacitive load.
NOTE 1: Test is a one-input, one-output only.

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

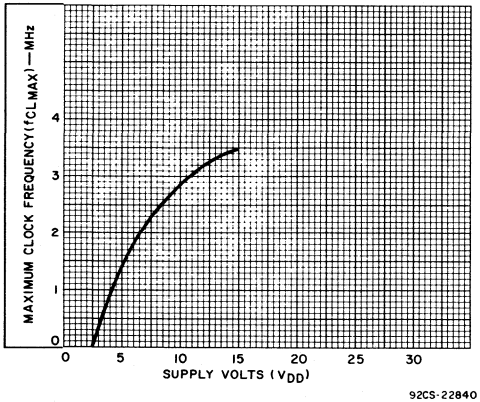


Fig. 8—Max. clock frequency vs. V_{DD}.

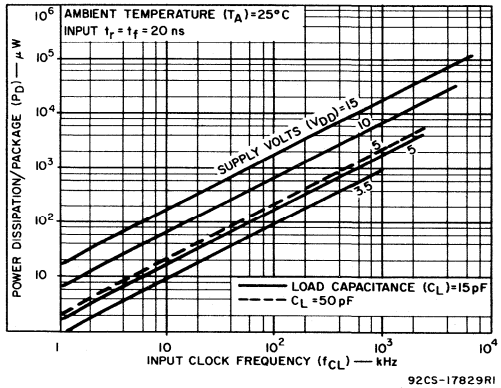


Fig. 9—Typ. dissipation characteristics.

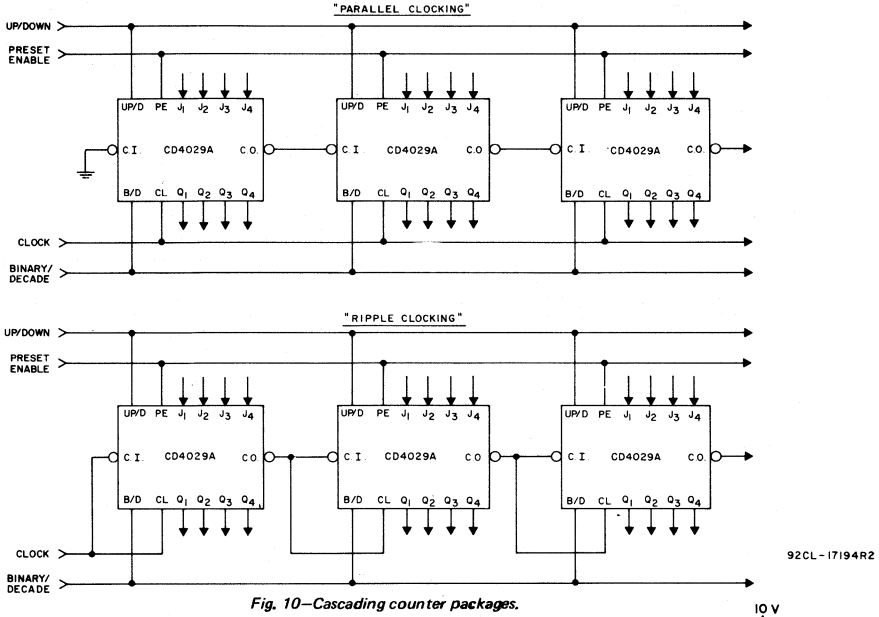


Fig. 10—Cascading counter packages.

The CD4029A "Clock" and "Up/Down" inputs are used directly in most applications. In applications where "Clock Up" and "Clock Down" inputs are provided, conversion to the CD4029A "Clock" and "Up/Down" inputs can easily be realized by use of the circuit shown below.

CD4029A changes count on positive transitions of "Clock Up" or "Clock Down" inputs. For the gate configuration shown below, when counting "up" the "Clock Down" input must be maintained "high" and conversely when counting "down" the "Clock Up" input must be maintained "high".

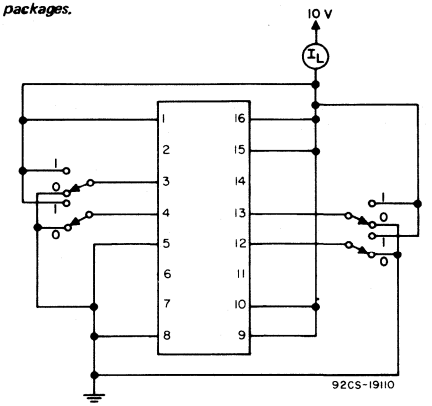


Fig. 12—Quiescent device current test circuit.

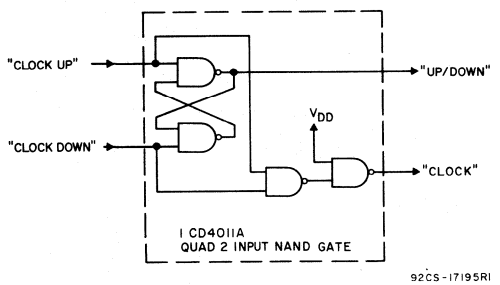


Fig. 11—Conversion of "clock up", "clock down" input signals to "clock" and "up/down" signals.

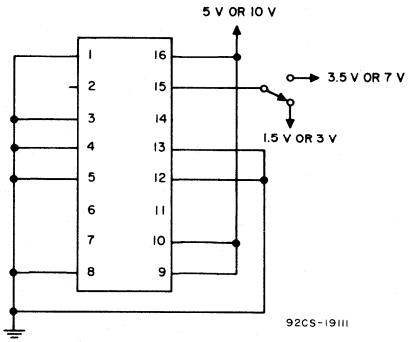


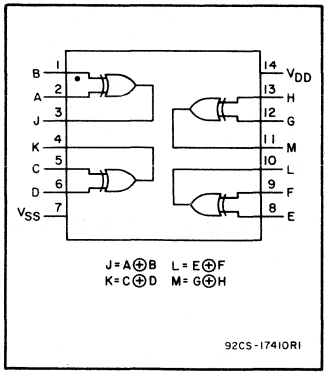
Fig. 13—Noise-immunity test circuit.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4030A/...



High-Reliability COS/MOS Quad Exclusive-OR Gate

(Positive Logic)

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- Medium speed operation ..... $t_{PHL} = t_{PLH}$ = 40 ns (typ.) @ C_L = 15 pF and $V_{DD}-V_{SS}$ = 10 V
- Low output impedance ..... 500Ω (typ.) @ $V_{DD}-V_{SS}$ = 10 V

Applications:

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/subtractors
- General logic functions

RCA CD4030A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4030A types each contain four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four N-channel and four P-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

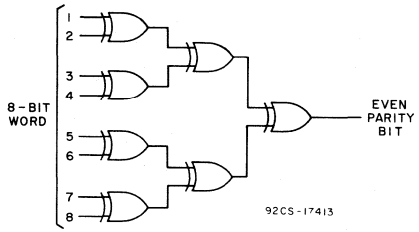


Fig. 2a—Even-parity-bit generator (1-3/4 x CD4030A).

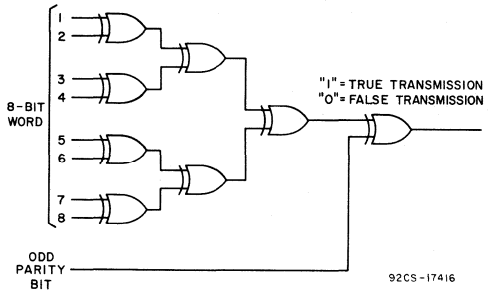


Fig. 2b—Even-parity checker (2 x CD4030A).

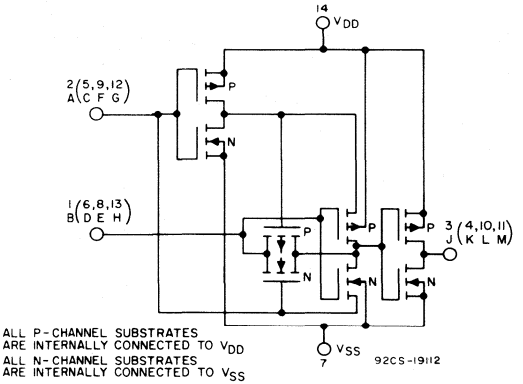


Fig. 1—Schematic diagram for 1 of 4 identical exclusive-OR gates.

TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

WHERE "1" = HIGH LEVEL
"0" = LOW LEVEL

These devices are electrically and mechanically identical with standard COS/MOS CD4030A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4030A "Slash" (/) Series can be supplied in six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to screening levels – /N, /R, and standard chip.

For a description of the screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".

The CD4030A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14 lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4030AD, CD4030AK,	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4030AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

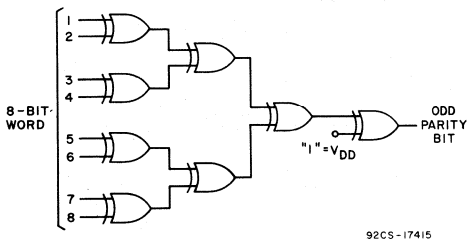


Fig. 2c—Odd-parity-bit generator (2 x CD4030A).

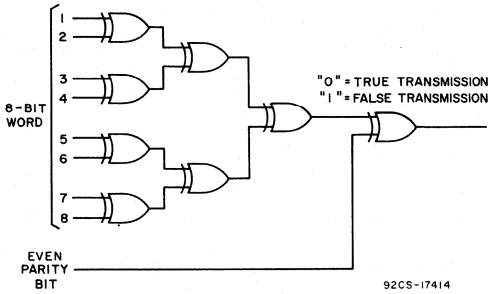


Fig. 2d—Odd-parity checker (2 x CD4030A).

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \geq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	V_{DD} Volts	LIMITS CD4030AD, CD4030AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	0.5	–	0.005	0.5	–	–	30	μA	11	1
			10	–	–	1•	–	0.01	1•	–	–	10•			
Quiescent Device Dissipation/Package	P_D		5	–	–	2.5	–	0.025	1.5	–	–	150	μW	–	
			10	–	–	10	–	0.1	10	–	–	100			
Output Voltage: Low-Level	V_{OL}		3	–	–	0.55•	–	–	0.5•	–	–	–	V		1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5•	–	–	0.55•			
High-Level	V_{OH}		3	2.25•	–	–	2.3•	–	–	–	–	–	V		1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5•	–	–	14.45•	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -10\mu A$		-0.7•	-1.7	-3•	-0.7•	-1.5	-3•	-0.3•	-1.3	-3•	V		2
P-Channel	$V_{TH}P$	$I_D = 10\mu A$		0.7•	1.7	3•	-0.7•	1.5	3•	0.3•	1.3	3•	V		
Noise Immunity (All inputs) *For Definition, See Appendix in SSD-207*	V_{NL}		5	1.5	–	–	1.5•	2.25	–	1.4•	–	–	V	12	1
			10	3•	–	–	3.	4.5	–	2.9	–	–			
	V_{NH}		5	1.4	–	–	1.5•	2.25	–	1.5•	–	–	V		
			10	2.9•	–	–	3•	4.5	–	3	–	–			
Output Drive Current: N-Channel	$I_D N$	0.5	5	0.75	–	–	0.6•	1.2	–	0.45	–	–	mA	3	2
		0.5	10	1.5	–	–	1.2•	2.4	–	0.9	–	–			
P-Channel	$I_D P$	4.5	5	-0.45	–	–	-0.25•	-0.6	–	-0.21	–	–	mA	4	
		9.5	10	-0.95	–	–	-0.6•	-1.3	–	-0.45	–	–			
Diode Test 100μA Test Pin	–			–	–	1.5•	–	–	1.5•	–	–	1.5•	V		3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

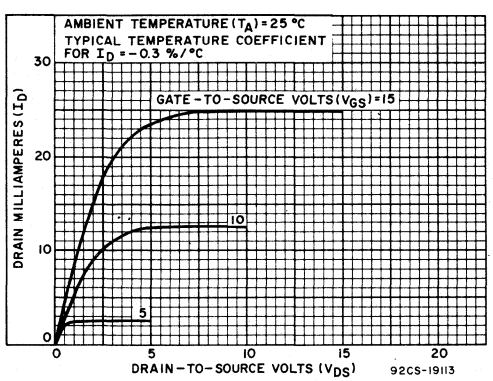


Fig. 3—Typ. N-channel drain characteristics.

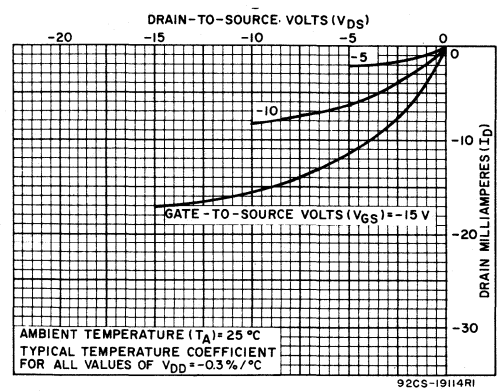


Fig. 4—Typ. P-channel drain chacteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = OV, C_L = 15pF, and all input rise and fall times = 20ns
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
			CD4030AD, CD4030AK					
		V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	100	200	ns	7, 9	1
		10	–	40	100.			
Transition Time: High-to-Low Level	t_{THL}	5	–	70	150	ns	8	1
		10	–	25	75.			
Low-to-High Level	t_{TLH}	5	–	80	150	ns		
		10	–	30	75.			
Input Capacitance	C_I	Any Input	–	5	–	pF	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
NOTE 1: Test is a one input one output only.

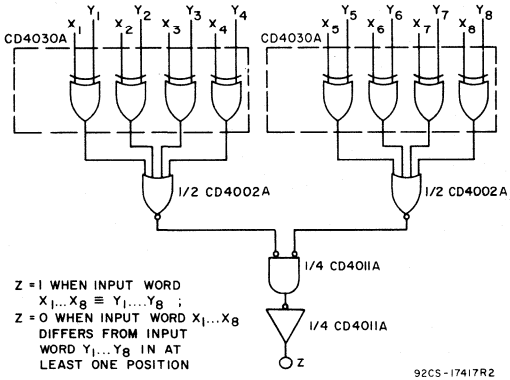


Fig. 5—8-bit comparator.

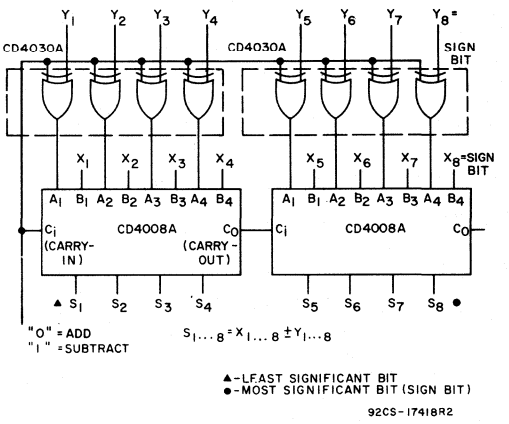


Fig. 6—8-bit two's complement adder-substractor.

TABLE I — TWO'S COMPLEMENT NUMBERS AND THEIR EQUIVALENT DECIMAL VALUES.

X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1		X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	
0	0	0	0	0	0	0	0	= 0	1	1	1	1	1	1	1	1	= −1
0	0	0	0	0	0	0	1	= 1	1	1	1	1	1	1	1	0	= −2
0	0	0	0	0	0	1	0	= 2	1	1	1	1	1	1	0	1	= −3
0	0	0	0	0	0	1	1	= 3	1	1	1	1	1	1	0	0	= −4
.	.	.	.	.	.	.	.	.	1	1	1	1	1	0	1	1	= −5
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	0	= 126	1	0	0	0	0	0	0	1	= −127
0	1	1	1	1	1	1	1	= 127	1	0	0	0	0	0	0	0	= −128

The Two's complement adder - subtractor can add or subtract any two of the numbers in Table I. For example:

a) $\begin{array}{r} 2 \\ +\underline{-5} \\ = \end{array}$

	SIGN BIT								
X	0	0	0	0	0	0	1	0	2 +
X	1	1	1	1	1	0	1	1	−5 +
C_i							0	+	+
S	0	1	1	1	1	1	1	0	1 = −3
	C_o								

b) $\begin{array}{r} -2 \\ -\underline{-5} \\ = \end{array}$

	SIGN BIT								
X	1	1	1	1	1	1	1	0	−2 +
y	1	1	1	1	1	0	1	1	−5
$\bar{y}$	0	0	0	0	0	1	0	0	+
C_i							1		+
S	1	0	0	0	0	0	1	1	= 3
	C_o								

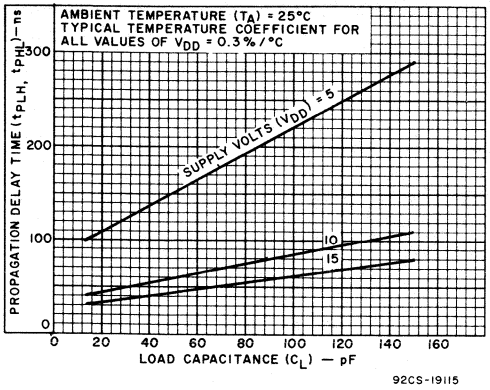


Fig. 7—Typ. propagation delay time vs. C_L.

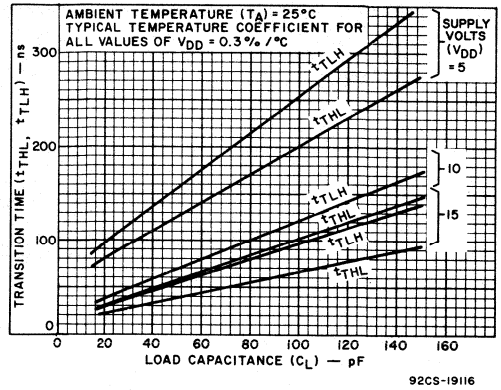


Fig. 8—Typ. transition time vs. C_L.

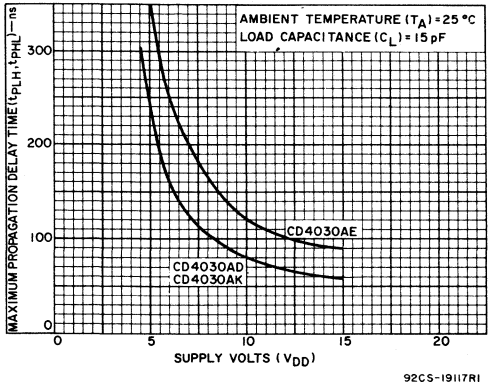


Fig. 9—Max. propagation delay time vs. V_{DD}.

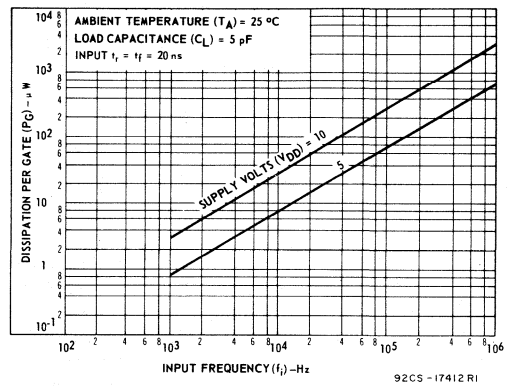


Fig. 10—Dissipation vs. input frequency.

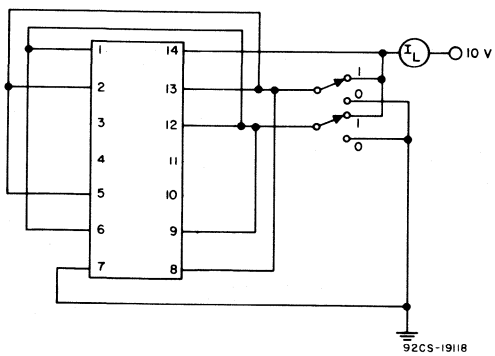


Fig. 11—Quiescent device current test circuit.

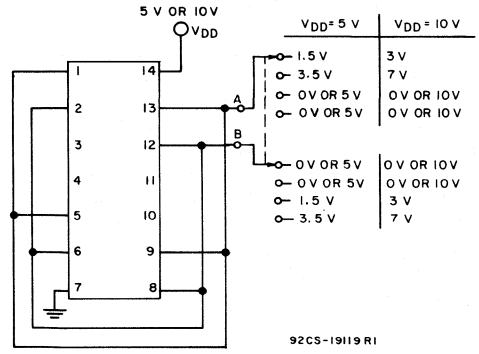


Fig. 12—Noise-immunity test circuit.

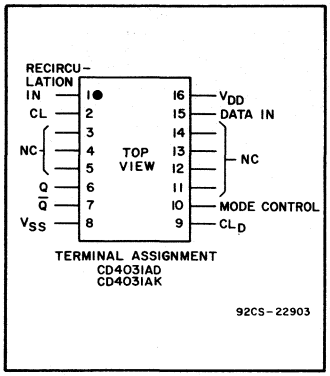
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4031A/...



TERMINAL ASSIGNMENT
CD4031AD
CD4031AK

92CS-22903

High-Reliability COS/MOS 64-stage Static Shift Register

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Applications:

For use in digital equipment where low-power dissipation, low package count, and/or high noise immunity are primary design requirements.

- **Serial shift registers**
- **Time delay circuits**

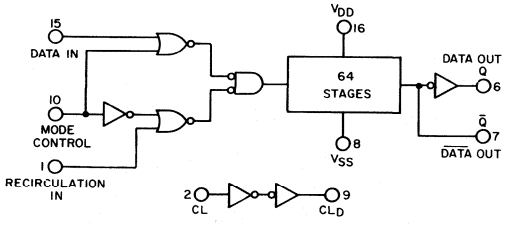
RCA CD4031A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4031A is a 64-stage static shift register in which each stage is a D-type, master-slave flip-flop.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 2 Megahertz can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the "low" or "high" state. the CD4031A has a mode control input that, when in the "high" state, allows operation in the recirculating mode. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements.

Data (Q) and $\overline{\text{Data}}$ ($\bar{Q}$) outputs are provided from the 64th register stage. The Data (Q) output is capable of driving one TTL or DTL load. These devices are electrically and mechanically identical with standard COS/MOS CD4031A types described in data bulletin 569 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA High-Reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

Features:

- **Fully static operation: DC to 4 MHz @ $V_{DD}-V_{SS}$ = 10V**
- **Operation from a single 3 to 15 V positive or negative power supply**
- **High noise immunity**
- **Microwatt quiescent power dissipation: 10 μW (typ.)**
- **Full military operating temperature range: −55°C to +125°C**
- **Single-phase clocking requirements**
- **Protection against electrostatic effects on all inputs**
- **Data compatible with TTL-DTL**
- **Recirculation capability**
- **Two cascading modes:**
  Direct clocking for high-speed operation
  Delayed clocking for reduced clock drive requirements



92CS-19745R1

Fig. 1—Functional diagram.

RCA Designation	MIL-M-38510 Designation
CD4031A	MIL-M-38510/05705

The packaged types in the CD4022A "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels –/N, /R, and standard chip.

For a description of the screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4031A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended	
DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended	
Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering)	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4031AD, CD4031AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4031AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A, D, /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A, H, /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

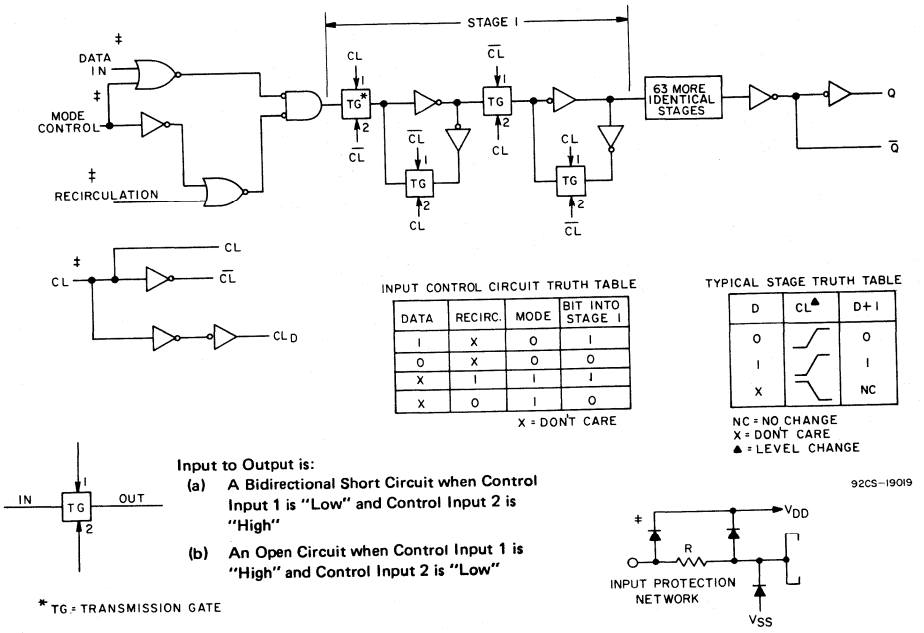


Fig. 2—CD4031A logic diagram and truth tables.

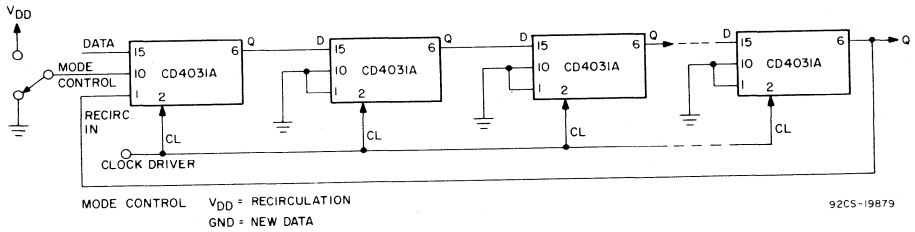


Fig. 3—Cascading using direct clocking for high speed operation (see clock rise & fall time requirement).

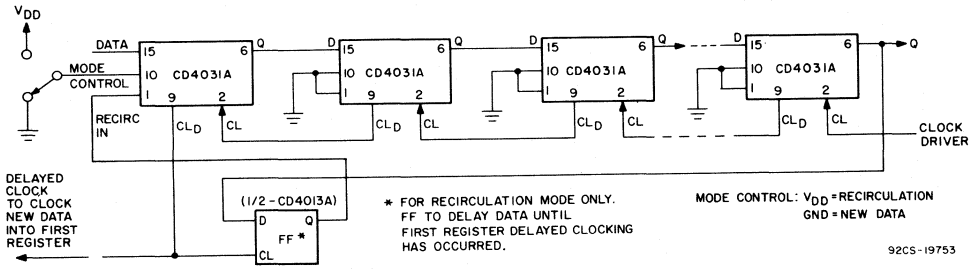


Fig. 4—Cascading using delayed clocking for reduced clock drive requirements.

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
					CD4031AD, CD4031AK											
			V_O	V_{DD}	−55°C			25°C			125°C					
			Volts	Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I_L			5	–	–	10	–	0.5	10	–	–	600	μA	13	1
				10	–	–	25•	–	1	25•	–	–	500•			
Quiescent Device Dissipation/Package	P_D			5	–	–	50	–	2.5	50	–	–	3000	μW	–	–
				10	–	–	250	–	10	250	–	–	5000			
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55•	–	–	0.5•	–	–	–	V	—	1
				5	–	–	0.01	–	0	0.01	–	–	0.05			
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.5•	–	–	0.55•			
High-Level	V_{OH}			3	2.25•	–	–	2.3•	–	–	–	–	–	V	—	1
				5	4.99	–	–	4.99	5	–	4.95	–	–			
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.5•	–	–	14.45•	–	–			
Threshold Voltage: N-Channel	V_{THN}	I_D = -20 μA			-0.7•	-1.7	-3•	-0.7•	-1.5	-3•	-0.3•	-1.3	-3•	V	—	2
P-Channel	V_{THP}	I_D = 20μA			0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•	V		
Noise Immunity (All Inputs) *For Definition, See Appendix in SSD-207*	V_{NL}		0.8	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	14	1
			1.0	10	3•	–	–	3•	4.5	–	2.9•	–	–			
	V_{NH}		4.2	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V		
			9.0	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: N-Channel	I_{DN}	Q	0.4	4.5	1.6	–	–	1.3•	2.6	–	0.91	–	–	mA	—	2
			0.5	10	–	9.6	–	–	8	–	–	5.6	–			
		$\bar{Q}$	0.5	5	0.11	–	–	0.09•	0.18	–	0.06	–	–			
			0.5	10	0.24	–	–	0.2•	0.4	–	0.14	–	–			
		CL_D	0.5	5	0.48	–	–	0.4•	0.8	–	0.28	–	–			
			0.5	10	1.5	–	–	1.2•	2.4	–	0.84	–	–			
P-Channel	I_{DP}	Q	4.5	5	-0.4	–	–	-0.32•	-0.64	–	-0.22	–	–	mA	—	2
			9.5	10	-0.85•	–	–	-0.70•	-1.4	–	-0.49	–	–			
		$\bar{Q}$	4.5	5	-0.11	–	–	-0.09•	-0.18	–	-0.06	–	–			
			9.5	10	-0.24	–	–	-0.20•	-0.4	–	-0.14	–	–			
		CL_D	4.5	5	-0.48	–	–	-0.40•	-0.8	–	-0.28	–	–			
			9.5	10	-1.0	–	–	-0.80•	-1.6	–	-0.56	–	–			
Diode Test 100 μA Test Pin	–				–	–	1.5•	–	–	1.5•	–	–	1.5•	V	—	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.
For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = OV, C_L = 15pF (unless otherwise specified), and input rise and fall times = 20 ns, except t_rCL and t_fCL.

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4031AD, CD4031AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
Propagation Delay Clock to Data Output Q & $\overline{Q}$*	t_{PHL}	C_L = 60pF	5	–	400	800	ns	7	1
			10	–	200	400			
Clock to CL_D	t_{PLH}		5	–	400	800		8	
			10	–	200	400			
Transition Time: Q Output	t_{THL}, t_{TLH}	C_L = 60pF	5	–	75	150	ns	9	–
			10	–	30	60			
$\overline{Q}$ Output			5	–	300	600			
			10	–	150	300			
CL_D Output			5	–	200	400		10	
			10	–	100	200			
Clock Rise & Fall Time**	t_rCL, t_fCL		5	–	–	2	μs	—	1
			10	–	–	1			
Set-Up Time	t_{SHL}, t_{SLH}		5	–	200	400	ns	—	—
			10	–	50	100			
Data Overhang Time	t_{DO}		5	–	0		ns	—	—
			10	–	20	50			
Maximum Clock*** Frequency	f_{CL}		5	0.8	2	–	MHz	11	1
			10	2●	4	–			
Input Capacitance Clock	C_I			–	60	–	pF	—	—
All Others				–	5	–			

*Capacitive loading on $\overline{Q}$ output affects propagation delay of Q output. These limits apply for $\overline{Q}$ load $C_L \leq 15pF$.

**If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15pF and the transition time of the output driving stage.

***Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature – $f_{max} = \frac{1}{(n-1)\ CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$ where n = number of packages

b) Not Using Delayed Clock – $f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

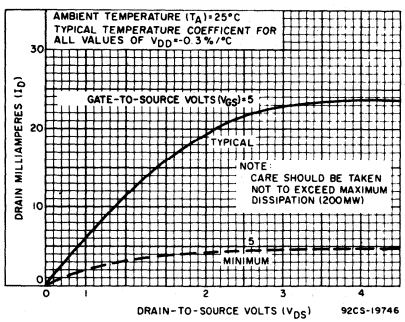


Fig. 5—Typical & minimum N-channel drain characteristics for Q output.

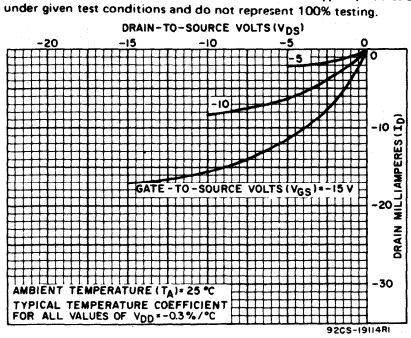


Fig. 6—Typical P-channel drain characteristics for Q output.

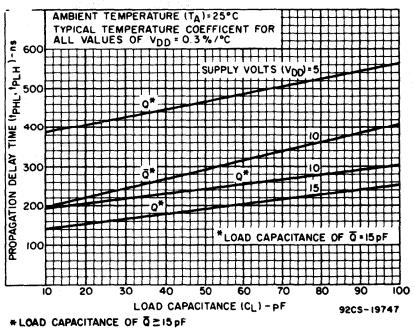


Fig. 7—Typical propagation delay time vs. C_L for data outputs.

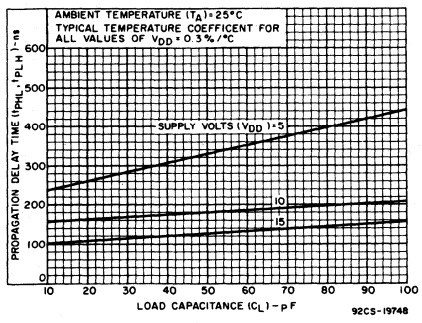


Fig. 8—Typical propagation delay vs. C_L for delayed clock output.

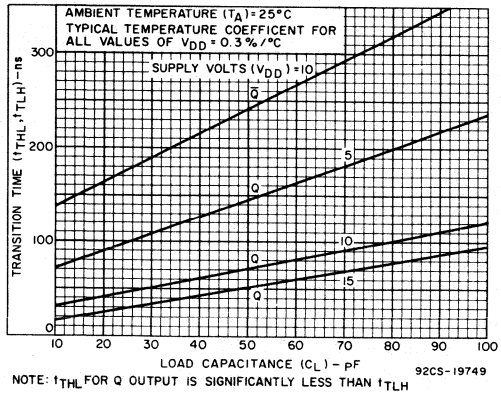


Fig. 9—Typical transition time vs. C_L for data outputs.

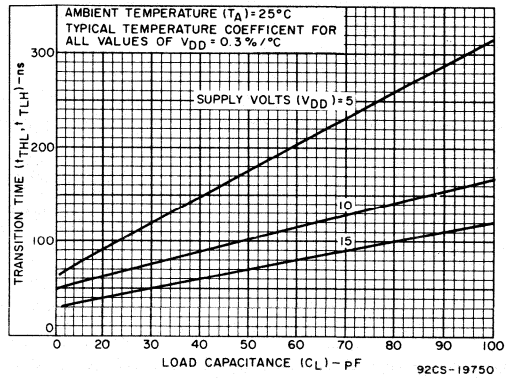


Fig. 10—Typical transition time vs. C_L for delayed clock output.

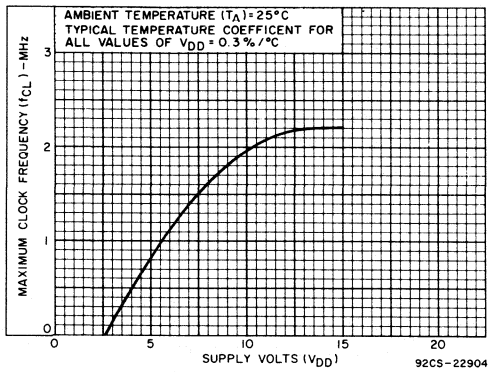


Fig. 11—Maximum clock frequency vs. V_{DD}.

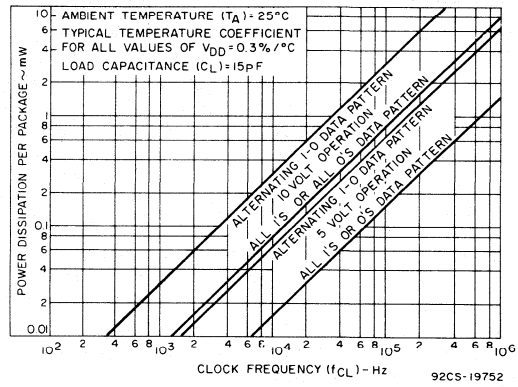


Fig. 12—Typical power dissipation vs. frequency.

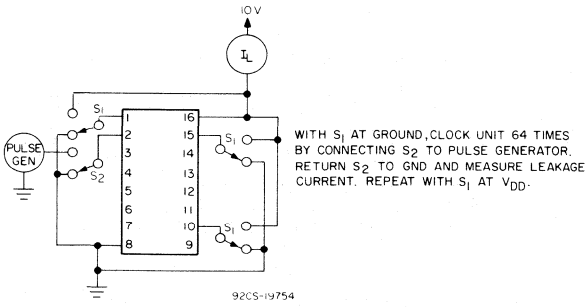


Fig. 13—Quiescent device current.

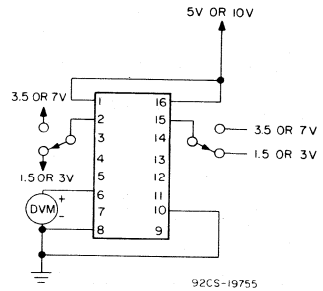


Fig. 14—Noise immunity.

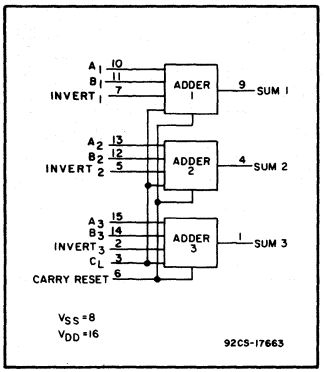
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4032A/... CD4038A/...



High-Reliability COS/MOS Triple Serial Adder

Positive Logic Adder – CD4032A

Negative Logic Adder – CD4038A

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Invert inputs on all adders for sum complementing applications**
- **Fully static operation. . . . .dc to 5 MHz (typ.)**
- **Buffered outputs**
- **Single-phase clocking**
- **Microwatt quiescent power dissipation. . . . . 5 μW (typ.)**

RCA CD4032A and CD4038A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4032A and CD4038A types consist of three serial-adder circuits with common clock and carry-reset inputs. Each adder has provisions for two serial-data input signals and an invert command signal which (when a logical "1") complements the sum. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032A or at the negative-going clock for the CD4038A. For spike-free operation the input data transitions should occur as soon as possible after the triggering edge.

The carry is reset to a logical "0" at the end of each word by applying a logical "1" signal to a carry-reset input one bit-position before the application of the first bit of the next word. Figs.2 and 4 show definitive waveforms for all input and output signals.

Applications:

- **Serial arithmetic units**
- **Digital correlators**
- **Digital datalink computers**
- **Flight control computers**
- **Digital servo control systems**

These devices are electrically and mechanically identical with standard COS/MOS CD4032A and CD4038A types described in data bulletin 503 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

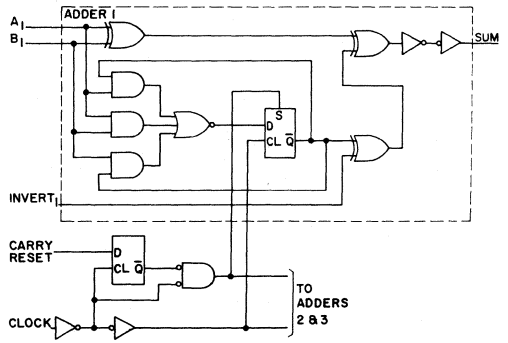


Fig.1 – CD4032A logic diagram of one of three serial adders.

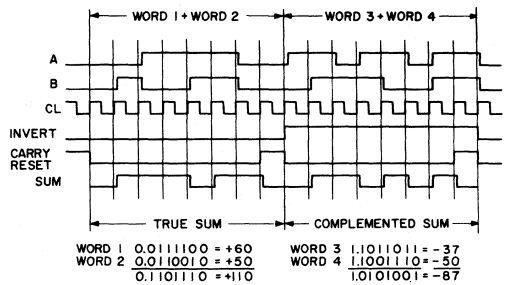


Fig.2 – CD4032A timing diagram.

The packaged types in the CD4032A & CD4038A "Slash" (/) Series can be supplied to six screening levels—1N, /1R, /1, /2, /3, /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to screening levels—1N, /R, and standard chip.

For a description of the screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to High-Reliability Report RIC-102, "High-Reliability COS/MOS CD4000A Series Types.

The CD4032A and CD4038A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4032AD, CD4032AK, CD4038AD, CD4038AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4032AH, CD4038AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

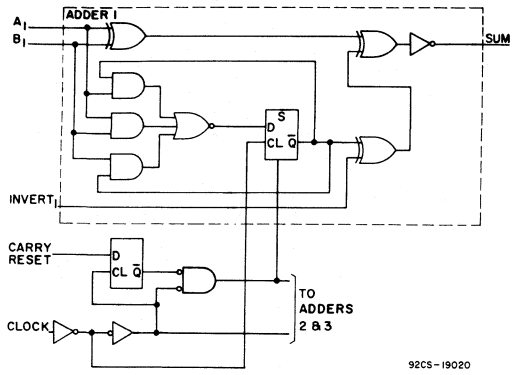


Fig.3 – CD4038A logic diagram of one of three serial adders.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

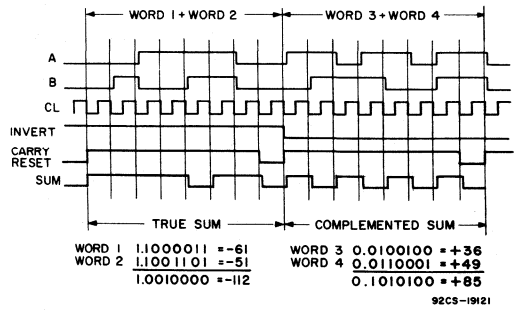


Fig.4 – CD4038A timing diagram.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4032AD, CD4032AK CD4038AD, CD4038AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.5	5	–	–	300	μA	8,10	1
			10	–	–	10●	–	1	10●	–	–	200●			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	2.5	25	–	–	1500	μW	–	
			10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low Level	V_{OL}		3	–	–	0.55●	–	–	0.5●	–	–	–	V		1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V		1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	V_{THP}	$I_D = -20$ μA		−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V		2
P-Channel	V_{THP}	$I_D = 20$ μA		0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●	V		
Noise Immunity (All Inputs) *For Definition, See Appendix in SSD-207*	V_{NL}	0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	9,11	1
		1.0	10	3●	–	–	3●	4.5	–	2.9●	–	–			
	V_{NH}	4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		9.0	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_{DN}	0.5	5	0.6	–	–	0.5●	0.9	–	0.3	–	–	mA		2
		0.5	10	0.75	–	–	0.7●	2.4	–	0.6	–	–			
P-Channel	I_DP	4.5	5	−0.21	–	–	−0.23●	−0.4	–	−0.075	–	–	mA		
		9.5	10	−0.7	–	–	−0.55●	−1.2	–	−0.35	–	–			
Diode Test 100 μA test pin	V_{DF}					1.5●			1.5●			1.5●	V		3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix

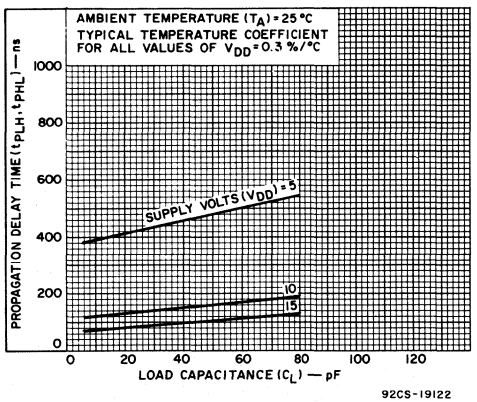


Fig.5 – Typ. propagation delay time vs. C_L for A, B, or invert inputs to sum outputs.

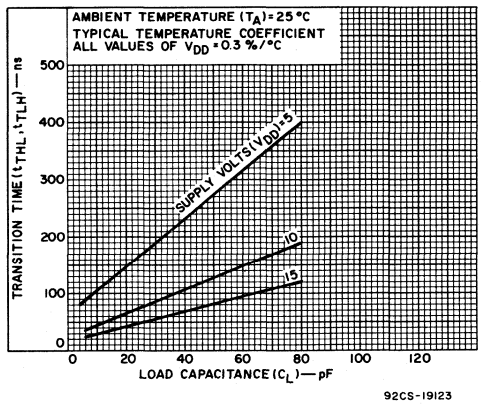


Fig.6 – Typ. transition time vs. C_L for sum outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = OV, C_L = 15pF, and input rise and fall times = 20ns, except Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. (See Appendix for Waveforms) **t_rCL and t_fCL.**

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4032AD, CD4032AK CD4038AD, CD4038AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time: A, B, or Invert Inputs to Sum Outputs	t_{PHL}, t_{PLH}		5	–	400	1100	ns	5	1
			10	–	125	250●			
Clock Input to Sum Outputs			5	–	800	2200	ns	–	1
			10	–	250	500●			
Transition Time (Sum Outputs)	t_{THL}, t_{TLH}		5	–	125	375	ns	6	1
			10	–	50	150●			
Clock Rise & Fall Time	**t_rCL, t_fCL		5	–	–	15	μs	–	1
			10	–	–	15●			
Input Set-Up Times*			5	t_rCL	–	–	–	–	
			10						
Maximum Clock Frequency	f_{CL}		5	1.5	2.5	–	MHz	–	1
			10	3●	5	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	

*This characteristic refers to the minimum time required for the A, B, or Reset Inputs to change state following a positive clock transition (CD4032A) or negative transition (CD4038A).

**If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Limits with black dot (●) designate 100% testing. Refer to RIC-1028 "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one-input, one-output only.

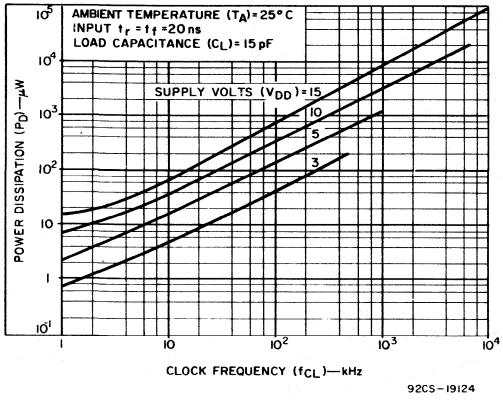


Fig.7 – Typ. dissipation characteristics.

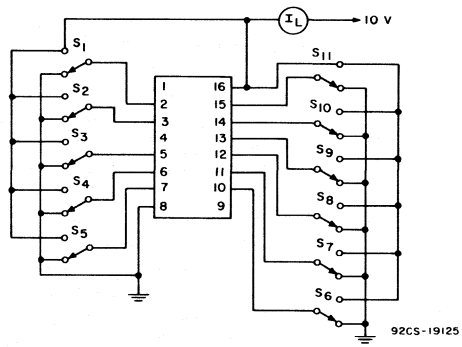


Fig.8 – Quiescent device current test circuit CD4032A.

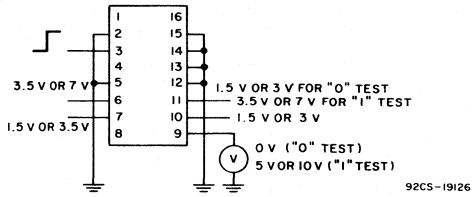


Fig.9 – Noise-immunity test circuit CD4032A.

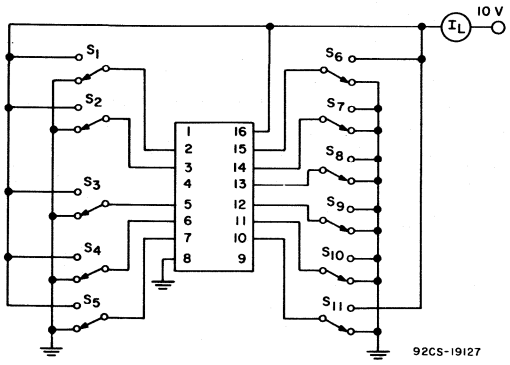


Fig.10 – Quiescent device current test circuit CD4038A.

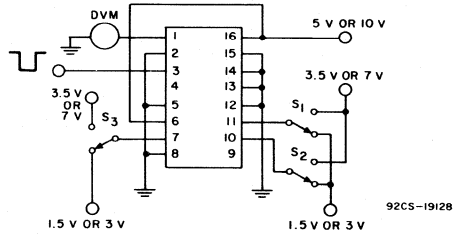


Fig.11 – Noise-immunity test circuit CD4038A.

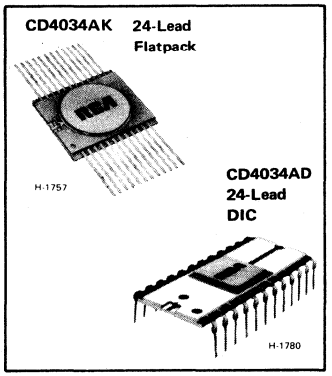
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

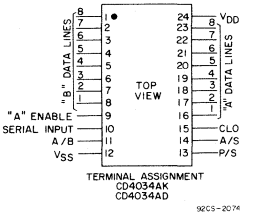
High-Reliability Slash(/) Series

CD4034A/...



High-Reliability COS/MOS MSI 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment



Special Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines
- Data recirculation for register storage
- Multipackage register expansion
- Fully static operation DC-to-5 MHz (typ.) at $V_{DD}-V_{SS}$ = 10 V

RCA CD4034A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4034A is a static eight-stage parallel- or serial-input parallel-output register. It can be used to: 1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single phase clock (CL), "A"-data enable (AE), Asynchronous/synchronous (A/S), "A" bus to "B" bus/"B" bus to "A" bus (A/B), and parallel/serial (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight "A" data lines are inputs (outputs) and the "B" data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for serial data is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A "high" P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is "low". If the A/S input is "high" this transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is "high" the A data lines are inputs (and B data lines are outputs); a "low" A/B signal reverses the direction of data flow.

Applications:

- Parallel Input/Parallel Output,
  Parallel Input/Serial Output,
  Serial Input/Parallel Output,
  Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

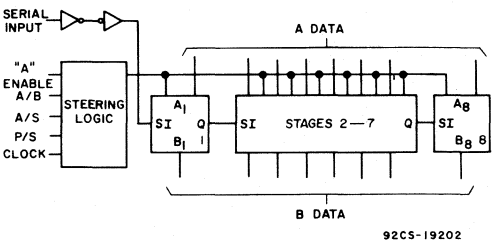


Fig. 1—Functional diagram.

These devices are electrically and mechanically identical with standard COS/MOS CD4034A types described in data bulletin 575 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4034A "Slash" (/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, and /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the chart below.

The CD4034A "Slash" (/) Series types are supplied in 24-lead dual-in-line ceramic packages ("D" suffix), in 24-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range:	
($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended	
DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended	
Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering)	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 24-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 24-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4034AD, CD4034AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4034AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A, D, /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A, H, /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4034AD, CD4034AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.3	5	–	–	300	μA	9	1
			10	–	–	10●	–	0.5	10●	–	–	200●			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	2.5	25	–	–	1500	μW	–	–
			10	–	–	100	–	10	100	–	–	2000			
Output Voltage Low-Level	V_{OL}		3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D = -10\,\mu A$		−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	V_{THP}	$I_D = 10\,\mu A$		0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}	0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	10	1
		1.0	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix SSD-207	V_{NH}	4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		9.0	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_{DN}	0.5	5	0.124	–	–	0.1●	0.2	–	0.07	–	–	mA	–	2
		0.5	10	0.31	–	–	0.25●	0.5	–	0.175	–	–			
P-Channel	I_{DP}	4.5	5	−0.075	–	–	−0.05●	0.1	–	−0.035	–	–	mA	–	2
		9.5	10	−0.188	–	–	−0.125●	−0.25	–	−0.088	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

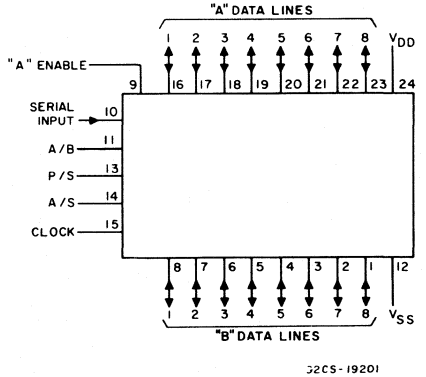


Fig.2—Functional and terminal assignment diagram for CD4034AK and CD4034AD.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CD4034AD,CD4034AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			V_{DD} Volts	Min.	Typ.	Max.			
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	600	1200	ns	5, 11, 12	1
			10	–	240	480●			
Transition Time	t_{THL}, t_{TLH}		5	–	250	750	ns	6, 11, 12	–
			10	–	100	300			
Minimum Clock Pulse Width	t_{WL}, t_{WH}		5	–	200	400	ns	–	–
			10	–	100	175			
Minimum High-Level AE, P/S, A/S Pulse Width	t_{WH}		5	–	240	480	ns	–	–
			10	–	85	195			
Clock Rise and Fall Time	*t_rCL, t_fCL		5	–	–	15	μs	–	1
			10	–	–	15●			
Set-Up Time	–		5	–	250	500	ns	11	–
			10	–	100	200			
Maximum Clock Frequency	f_{CL}		5	1.5	2.5	–	MHz	–	1
			10	3.0●	5	–			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–

* If more than one unit is cascaded, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF (see chart above) and the transition time of the output driving stage for the estimated capacitive load.

Note 1: Test is a one input one output only.

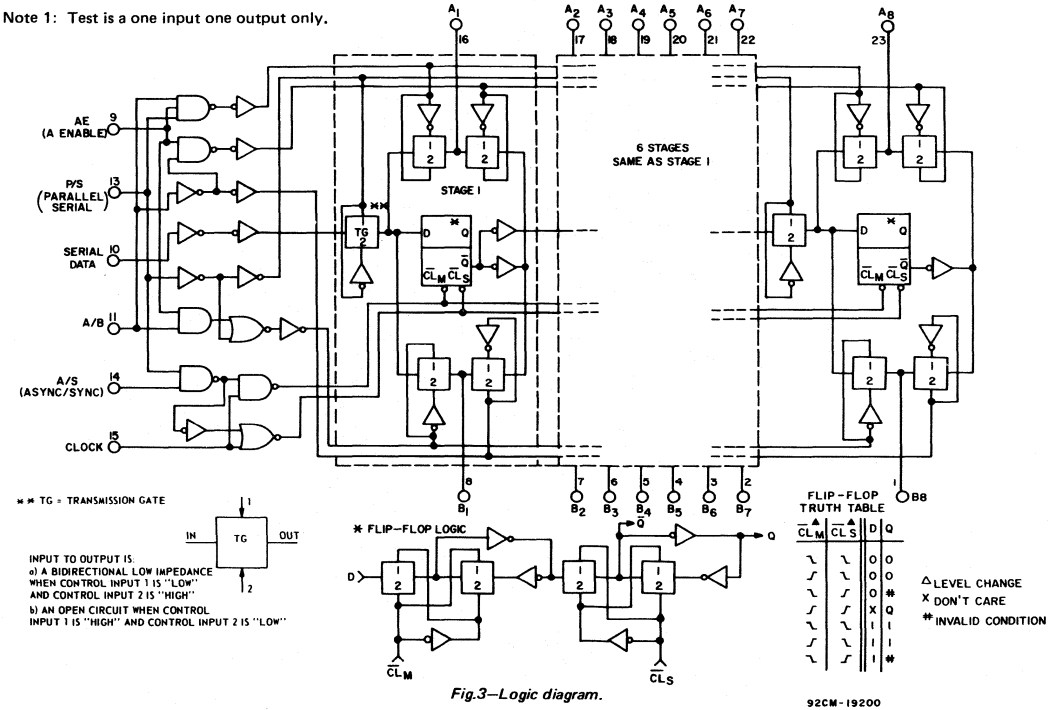


Fig.3—Logic diagram.

Table I Truth Table for Register Input-Levels and the Resulting Register Operation (L = Low Level, H = High Level, X = Don't Care)

"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled,"B" Parallel Data Outputs, Synch Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

* Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

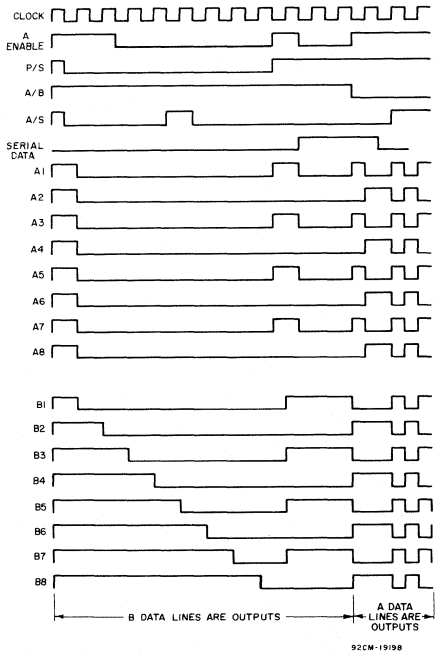


Fig. 4—Timing diagram.

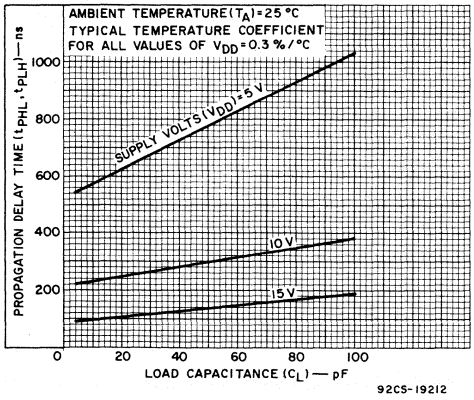


Fig. 5—Typical propagation delay time vs. C_L.

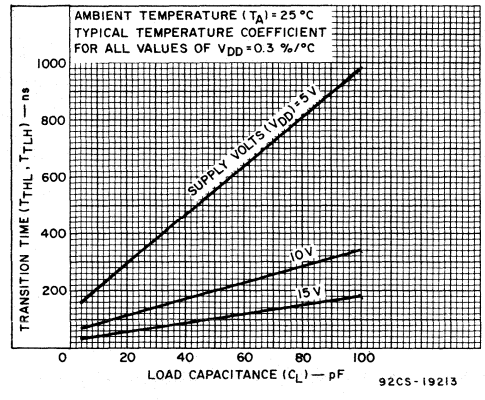


Fig. 6—Typical transition time vs. C_L.

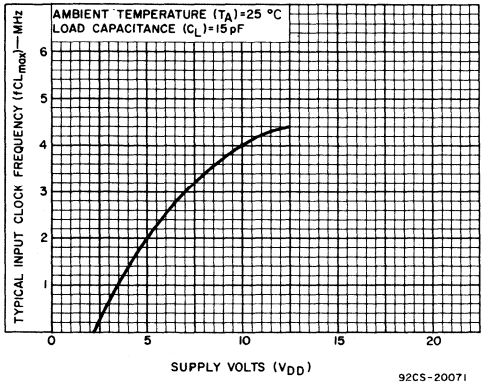


Fig. 7—Typical input frequency vs. V_{DD}.

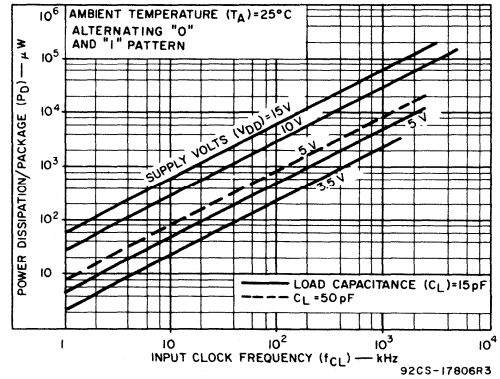


Fig. 8—Typical dissipation characteristics.

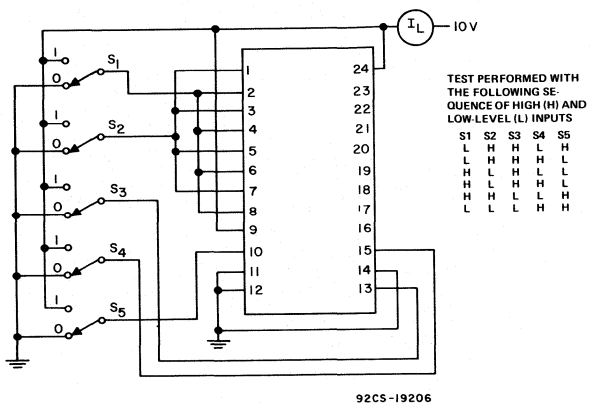


Fig. 9—Quiescent device current test circuit.

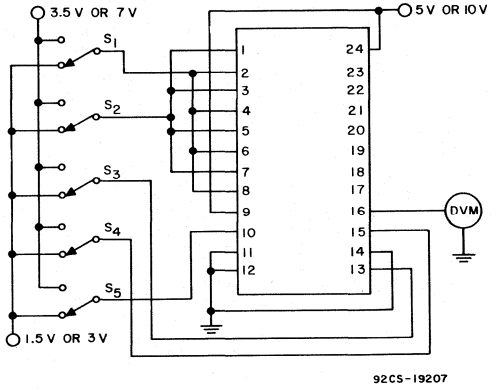


Fig. 10 — Noise immunity test circuit.

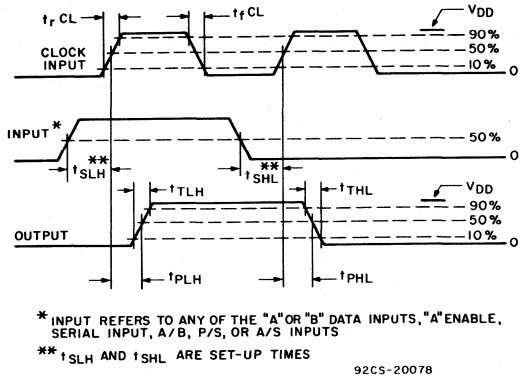


Fig. 11 — Synchronous operation propagation delay times, transition times, and set-up times.

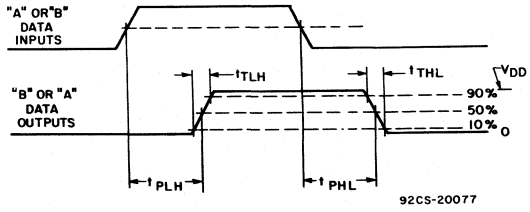
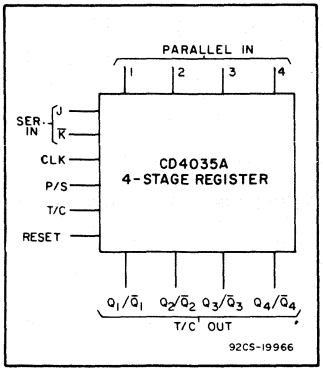


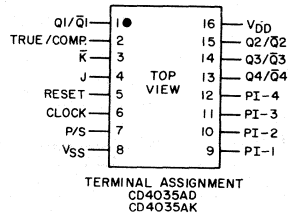
Fig. 12—Asynchronous operation propagation delay time.

RCA Solid State Division

Digital Integrated Circuits
Monolithic Silicon
High-Reliability Slash(/) Series
CD4035A/...



High-Reliability COS/MOS 4-Stage Parallel In/Parallel Out Shift Register



TERMINAL ASSIGNMENT
CD4035AD
CD4035AK

92CS-22905

with J-K Serial Inputs and True/Complement Outputs

For Logic Systems Applications on Aerospace, Military, and Critical Industrial Equipment

RCA CD4035A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4035A is a four-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via JK logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is "high". In the parallel or serial mode information is transferred on positive clock transitions.

When the True/Complement control is "high", the True contents of the register are available at the output terminals. When the True/Complement control is "low", the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the clock signal.

$\overline{JK}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With JK inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

These devices are electrically and mechanically identical with standard COS/MOS CD4035A types described in data bulletin 568 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4035A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1, /2, /3, /4 --- which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels --- /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types",*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see tables I and II.

The CD4035A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Applications:

- **Sequence generation, control circuits, code conversion**
- **Counters, Registers, Arithmetic-Unit Registers, Shift Left – Shift Right Registers, Serial-to-Parallel/Parallel-to-Serial conversions.**

Features:

- **4-Stage clocked shift operation**
- **Synchronous parallel entry on all 4 stages**
- **$\overline{JK}$ inputs on first stage**
- **Asynchronous True/Complement control on all outputs**
- **Reset control**
- **Static flip-flop operation; Master-slave configuration**
- **Buffered outputs**
- **Low-Power Dissipation - 5 μ W typ. (ceramic)**
- **High speed – to 5 MHz**

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4035AK, CD4035AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4035AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4035AD/1N

CD4035A D /1N

	Package Suffix Letter	Screening Level
Type Designation	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4035AH/N

CD4035A H /N

	Package Suffix Letter	Screening Level
Type Designation	H = Chip Version	/N /R

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range ..... −65 to +150 °C
Operating-Temperature Range ..... −55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) ..... −0.5 to +15 V
Device Dissipation (Per Package) ..... 200 mW
All Inputs ..... $V_{SS} \leq V_I \leq V_{DD}$
Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V
Recommended
Input-Voltage Swing ..... V_{DD} to V_{SS}
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32"
(1.59 ± 0.79 mm) from case
for 10 s max. ..... +265 °C

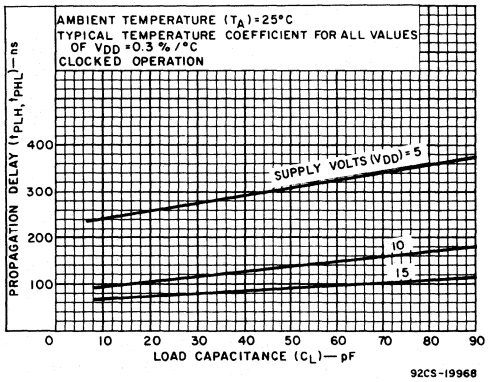


Fig. 1 — Typical Propagation Delay Time vs. Load Capacitance.

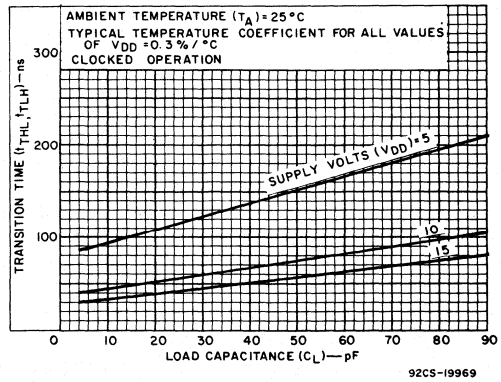


Fig. 2—Typical Transition Time vs. Load Capacitance.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4035AD, CD4035AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	5	–	0.3	5	–	–	300	μA	12	1
			10	–	–	10●	–	0.6	10●	–	–	200●			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	1.5	25	–	–	1500	μW	4	–
			10	–	–	100	–	5	100	–	–	2000			
Output Voltage Low-Level	V_{OL}		3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$		−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$		0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}	0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	11	1
		1	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix	V_{NH}	4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		9	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	$I_D N$	0.5	5	0.62	–	–	0.5●	1	–	0.35	–	–	mA	–	2
		0.5	10	1.55	–	–	1.25●	2.5	–	0.87	–	–			
P-Channel	$I_D P$	4.5	5	−0.31	–	–	−0.25●	−0.5	–	−0.17	–	–	mA	–	2
		9.5	10	−0.81	–	–	−0.65●	−1.3	–	−0.45	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

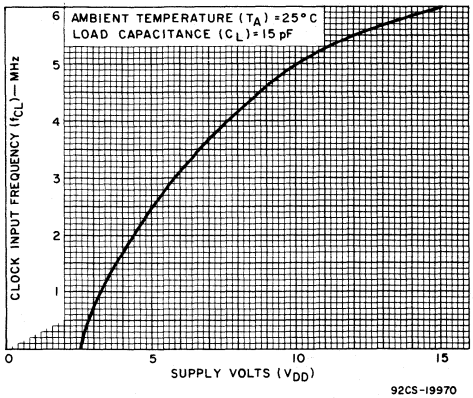


Fig. 3—Typical clock input frequency vs. V_{DD}

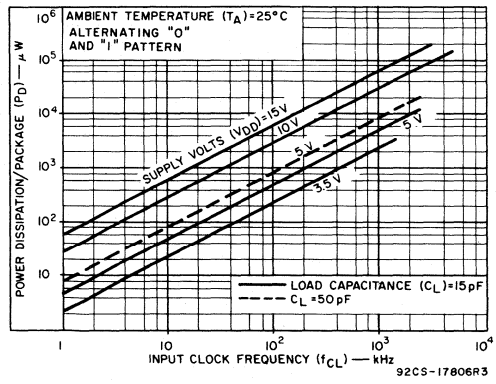


Fig. 4—Typical dissipation characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C and C_L = 15 pF*

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4035AD, CD4035AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
CLOCKED OPERATION								
Propagation Delay Time:	t_{PLH}, t_{PHL}	5	–	250	500	ns	1	1
		10	–	100	200●			
Transition Time:	t_{THL}, t_{TLH}	5	–	100	200	ns	2	1
		10	–	50	100●			
Minimum Clock Pulse Duration	t_{WL}, t_{WH}	5	–	200	335	ns	–	–
		10	–	100	165			
Clock Rise & Fall Time	t_{fCL}*, t_{fCL}	5		–	15	μs	–	1
		10		–	5			
Setup Time: $\overline{J/K}$ Lines		5	–	250	500	ns	–	–
		10	–	100	200			
Parallel-In Lines		5	–	100	350			
		10	–	50	80			
Maximum Clock Frequency	f_{CL}	5	1.5	2.5	–	MHz	3	1
		10	3 ●	5	–			
Input Capacitance	C_I	Any Input	–	5	–	pF	–	–
RESET OPERATION								
Propagation Delay Time:	t_{PHL}, t_{PLH}	5	–	250	500	ns	–	–
		10	–	100	200			
Minimum Reset Pulse Duration	t_{WL}, t_{WH}	5	–	200	400	ns	–	–
		10	–	100	175			

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is either a one input or a one output only.

*If more than one unit is cascaded t_{fCL} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

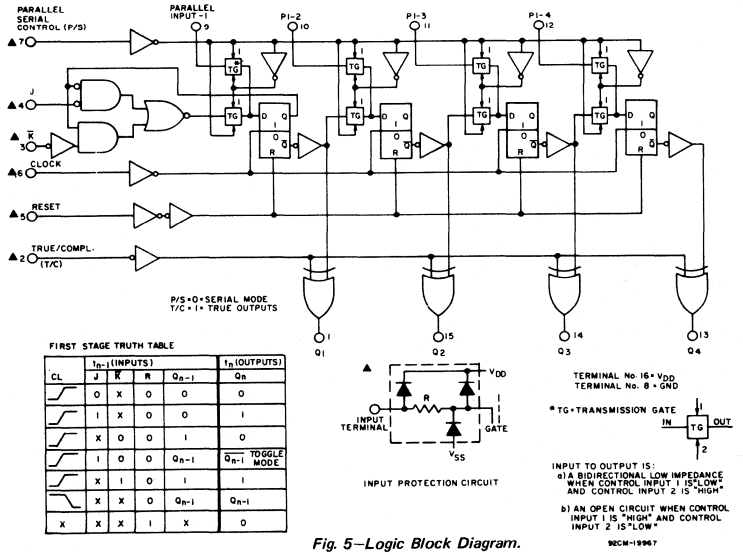


Fig. 5—Logic Block Diagram.

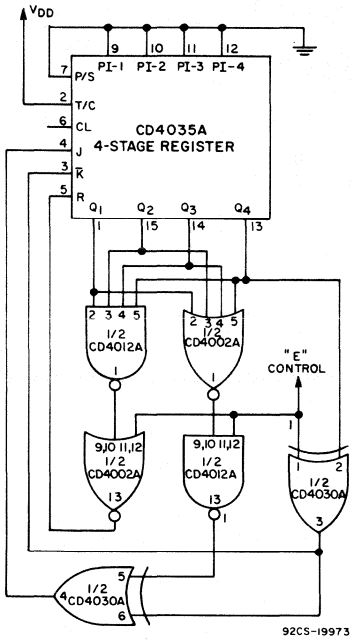


Fig. 6(a)—Double Sequence Generator.

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E)

Control = E =	0				1				
	Q_1	Q_2	Q_3	Q_4		Q_1	Q_2	Q_3	Q_4
	A	B	C	D		A	B	C	D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	1	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	0	0
8	0	0	0	1	7	1	1	1	0

Fig. 6(b)—State Sequences.

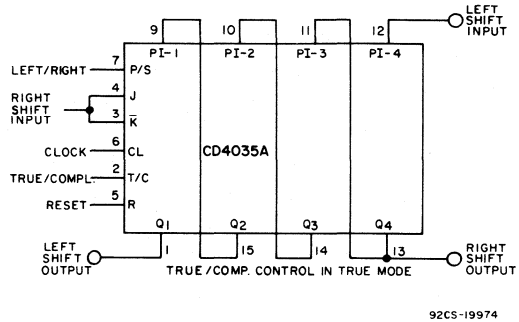


Fig. 7—Shift Left/Shift Right Register.

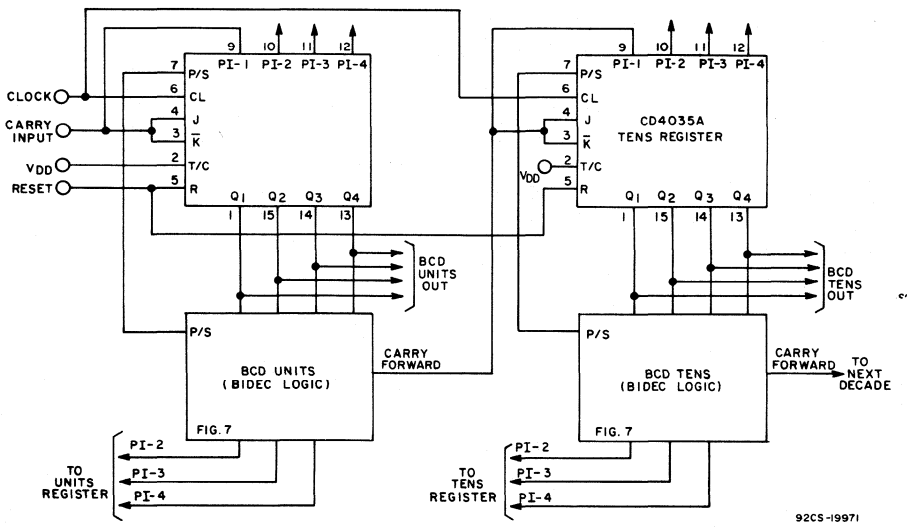


Fig. 8—Binary-to-BCD Converter.

Using Couleur's Technique (BIDEC)▲, a binary number (most significant bit, MSB) first is shifted and processed, such that the BCD equivalent is obtained when the last binary bit is clocked into the register. The CD4035A, with the correct conversion logic, can also be used as a BCD-to-binary converter.

▲The basic rule is: If a 4 or less is in a decade, shift with the next clock pulse; if a 5 or greater is in a decade, add 3 and then shift at the next clock pulse. For more information refer to "IRE TRANSACTIONS ON ELECTRONIC COMPUTERS", Dec. 1958, Pages 313–316.

							Units Register				Tens Register			
							1	2	4	8	1	2	4	8
		LSB				MSB								
58	=	0	1	0	1	1	1							
Shift														
			0	1	0	1	1	1						
Shift														
				0	1	0	1	1	1					
Shift														
					0	1	0	1	1	1				
Add* 3 to Units Decade & Shift							(1	1)						
						0	1	0	0	1	0	1		
Shift														
							0	1	0	0	1	0	1	
Add* 3 to Units Decade & Shift							(1	1)						
							0	0	0	1	1	0	1	0
*From Left to Right									8				5	

Fig. 9—Example of Binary-to-BCD Conversion.

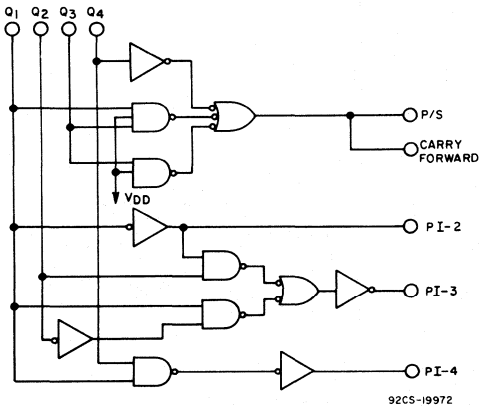


Fig. 10—BIDEC Logic.

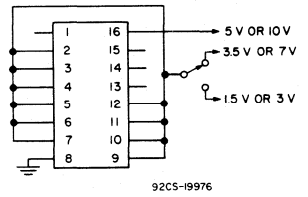


Fig. 11—Noise immunity.

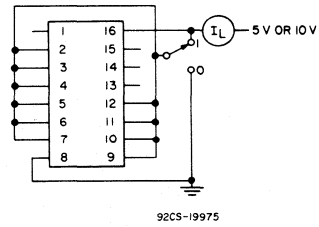


Fig. 12—Quiescent device current.

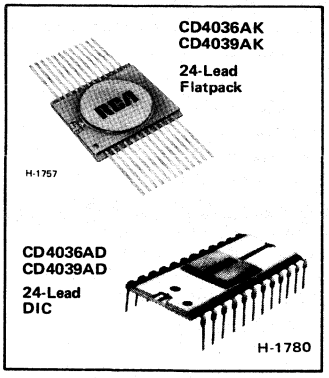
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4036A/..., CD4039A/...



High-Reliability COS/MOS 4-Word by 8-Bit Random-Access NDRO Memory

For Logic Systems Applications on Aerospace, Military, and Critical Industrial Equipment

Binary Addressing	CD4036AD, CD4036AK
Direct Word-Line Addressing	CD4039AD, CD4039AK

Special Features:

- **COS/MOS logic compatibility at all input and output terminals**
- **Memory bit expansion**
- **Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines**
- **Memory bypass capability for all bits**
- **Buffering on all outputs**
- **CD4036A- on-chip binary address decoding, separate READ INHIBIT and WRITE controls**
- **CD4039A-Direct word-line addressing**
- **Access Time—200 ns(Typ) at V_{DD}=10 V**

RCA CD4036A and CD4039A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4036A is a single monolithic integrated circuit containing a 4-word x 8-bit Random Access NDRO Memory. Inputs include 8 INPUT-BIT lines, CHIP INHIBIT, WRITE, READ INHIBIT, MEMORY BYPASS, and 2 ADDRESS inputs. 8 OUTPUT-BIT lines are provided.

All input and output lines utilize standard COS/MOS inverter configurations and hence can be directly interfaced with COS/MOS logic devices.

CHIP INHIBIT allows memory word expansion by WIRE-ORing of multiple CD4036A packages at either the 8-bit input and/or output lines (See Fig. 1). With CHIP INHIBIT "high", both READ and WRITE operations are inhibited on the CD4036A. With CHIP INHIBIT "low", information can be written into and/or read continuously from one of the

Applications

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements.

- **Channel Preset Memory in digital frequency-synthesizer circuits**
- **General-purpose and scratch-pad memory in COS/MOS and other low-power systems.**

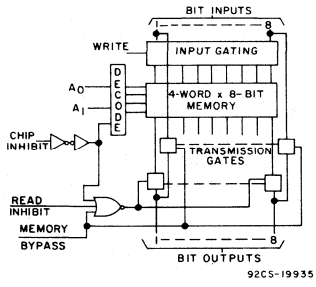


Fig. 1— CD4036A — Logic block diagram.

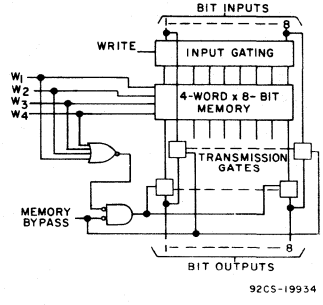


Fig. 2—CD4039A — Logic block diagram.

four words selected by the binary code on the two address lines. With CHIP INHIBIT "low", a "high" WRITE signal and a "low" READ INHIBIT signal activate WRITE and READ operations, respectively, at the addressed word location (See Fig. 9).

The MEMORY BYPASS signal, when "high", allows shunting of information from the 8 INPUT-BIT lines directly to the 8 OUTPUT-BIT lines without disturbing the state of the 4 words. During the bypass operation input information may also be written into a selected word location, provided the CHIP INHIBIT is "low" and the WRITE is "high". The READ operation is deactivated during the BYPASS operation because information is fed directly from the 8 INPUT-BIT lines to the 8 OUTPUT-BIT lines.

RCA type CD4039A is identical to the CD4036A with the exception that individual address-line inputs have been provided for each memory word in place of the binary ADDRESS, CHIP INHIBIT, and READ INHIBIT inputs. When Wire-Oring multiple CD4039A packages for memory word expansion, an individual CD4039A is selected by addressing one of its word locations. The READ operation is activated whenever a word location is addressed (via a "high" signal—see Fig. 10).

These devices are electrically and mechanically identical with standard COS/MOS CD4036A and CD4039A types described in data bulletin 613 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4036A and CD4039A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1, /2, /3, /4 --- which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels --- /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types",*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the tables on this page.

The CD4036A and CD4039A "Slash" (/) Series types are supplied in 24-lead dual-in-line ceramic packages ("D" suffix), in 24-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 24-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 24-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4036AD, CD4036AK, CD4039AD, CD4039AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4036AH, CD4039AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} < V_I < V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4036AD/1N

CD4036A	D	/1N
Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4036AH/N

CD4036A	H	/N
Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4036AD, CD4036AK CD4039AD, CD4039AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.			
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	μA	12,13	1
				10	–	–	10●	–	1	10●	–	–	200●			
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	μW	–	–
				10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}			3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
				5	–	–	0.01	–	0	0.01	–	–	0.05			
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.5●	–	–	0.5●			
High-Level	V_{OH}			3	1.45●	–	–	1.5●	–	–	–	–	–	V	–	1
				5	4.99	–	–	4.99	5	–	4.95	–	–			
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D = -20$ μA			−0.7●	−1.7	−3●	−0.7●	−1.5●	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	V_{THP}	$I_D = 20$ μA			0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●	V	–	2
Noise Immunity (All inputs except bit inputs when in memory bypass mode.)	V_{NL}		0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	14	1
			1	10	3●	–	–	3●	4.5	–	2.9●	–	–			
	V_{NH}		4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–			
			9	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_DN	Normal Read Modes	0.5	5	0.12	–	–	0.10●	0.2	–	0.07	–	–	mA	4	2
			0.5	10	0.3	–	–	0.25●	0.5	–	0.17	–	–			
P-Channel	I_DP		4.5	5	−0.12	–	–	−0.10●	−0.2	–	−0.07	–	–	mA	5	2
			9.5	10	−0.3	–	–	−0.25●	−0.5	–	−0.17	–	–			
Output Drive Current N-Channel	I_DN	Memory Bypass Mode +	0.5	5	0.04	–	–	0.03●	0.06	–	0.02	–	–	mA	–	2
			0.5	10	0.09	–	–	0.075●	0.15	–	0.05	–	–			
P-Channel	I_DP		4.5	5	−0.04	–	–	−0.03●	−0.06	–	−0.02	–	–	mA	–	2
			9.5	10	−0.09	–	–	−0.075●	−0.15	–	−0.05	–	–			
Diode Test	V_{DF}	100 μA Test Pin			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I		–	–	–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

+Bit inputs driven from low-impedance driver.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

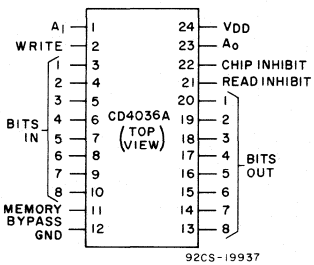
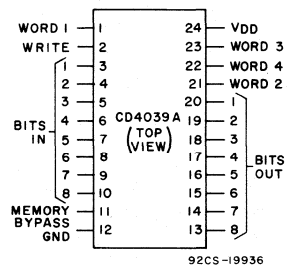


Fig. 3a)—CD4036AD and CD4036AK terminal assignments.



b)—CD4039AD and CD4039AK terminal assignments.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C and C_L = 15 pF*
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

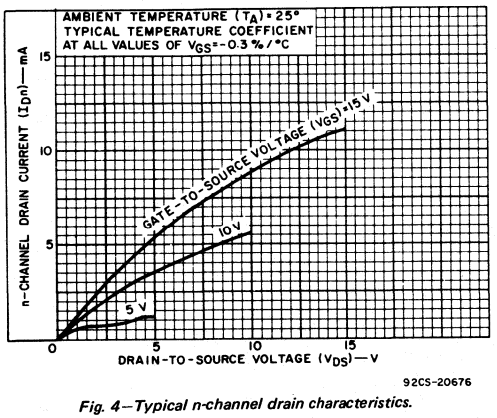
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	V_{DD} Volts	CD4036AD, CD4036AK CD4039AD, CD4039AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
Read Delay Time: (Access time) Read Inhibit (RI)	t_{rd}	OUTPUT TIED THROUGH 100 kΩ TO V_{SS} FOR DATA OUTPUT "HIGH" AND TO V_{DD} FOR DATA OUTPUT "LOW"	5	–	375	750	ns	9, 10	4
			10	–	150	300●			
Chip Inhibit (CI)			5	–	500	1000	ns	9, 10	4, 7
			10	–	200	400●			
Memory Bypass (MB)			5	–	375	750	ns	9, 10	7
			10	–	150	300●			
Address (ADD)			5	–	500	1000	ns	6, 9, 10	1, 7
			10	–	200	400●			
Write Set-up Time	t_{WS}		5	250	125	–	μs	9, 10	2, 7
			10	100●	50	–			
Write Removal Time	t_{WR}		5	0	0	–	ns	9, 10	3, 7
			10	30●	0	–			
Write Pulse Duration	t_W		5	150	75	–	ns	9, 10	7
			10	60●	30	–			
Data Set-up Time	t_{DS}		5	–	0	0*	ns	9, 10	5
			10	–	0	0*			
Data Overlap Time	t_{DO}		5	100▲	50	–	ns	9, 10	6
			10	40▲	20	–			
Output Transition Time	t_{THL}, t_{TLH}		5	–	200	400	ns	7	–
			10	–	100	200			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–

1. For CD4036A only, remove 100-kΩ test condition and write all 1's in word one, and all 0's in word two, or vice-versa.
2. Delay from change of ADDRESS or CHIP-INHIBIT signals to application of WRITE pulse.
3. Delay from removal of WRITE pulse to change of ADDRESS or CHIP-INHIBIT signals.
4. Values for CD4036AD & 4036AK only.
5. The time that DATA signal must be present before the WRITE pulse removal.
6. The time that DATA signal must remain present after the WRITE pulse removal.
7. Test is a one input one output only.

▲ Min. indicates satisfactory operation if t_{DO} equals or exceeds this value.

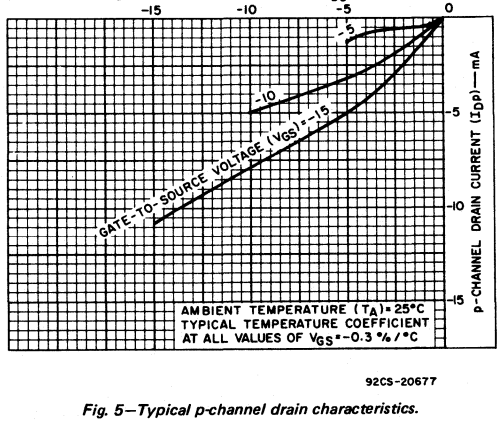
* Max. indicates satisfactory operation if t_{DS} equals or exceeds this value.

● For footnote, see Page 3.



92CS-20676

Fig. 4—Typical n-channel drain characteristics.



92CS-20677

Fig. 5—Typical p-channel drain characteristics.

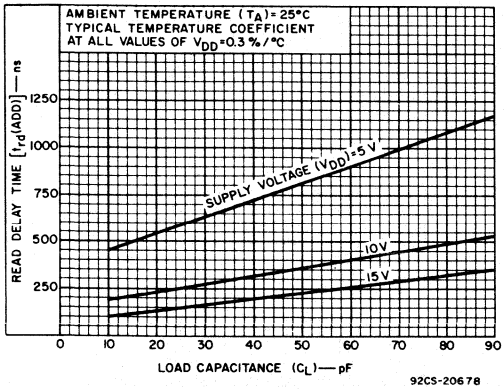


Fig. 6—Typical read delay time vs C_L.

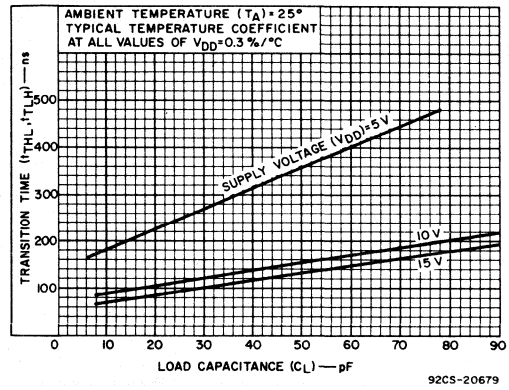


Fig. 7—Typical transition time vs. C_L.

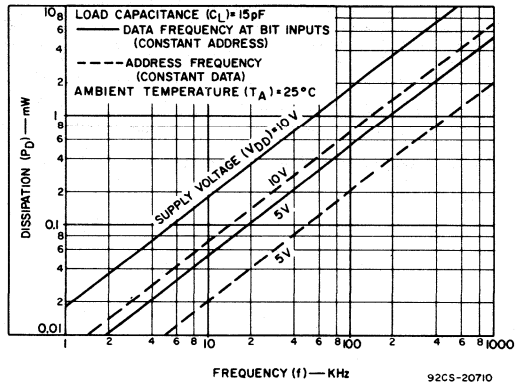


Fig. 8—Typical power dissipation vs. frequency.

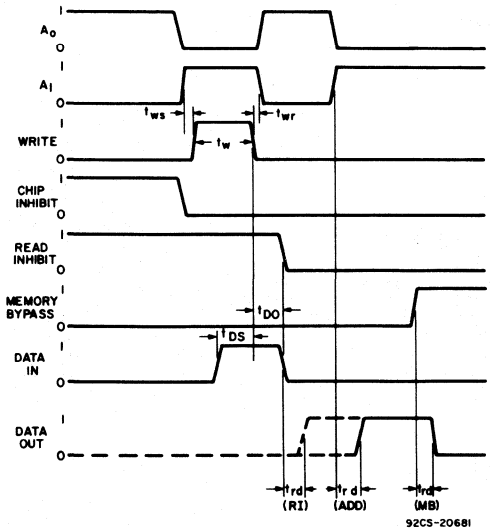


Fig. 9—CD4036A Timing Diagram.

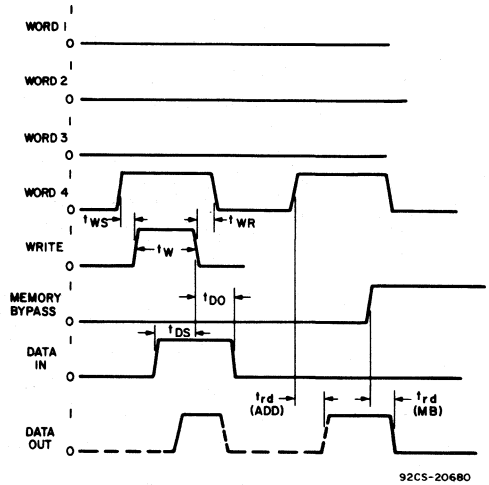


Fig. 10—CD4039A Timing Diagram.

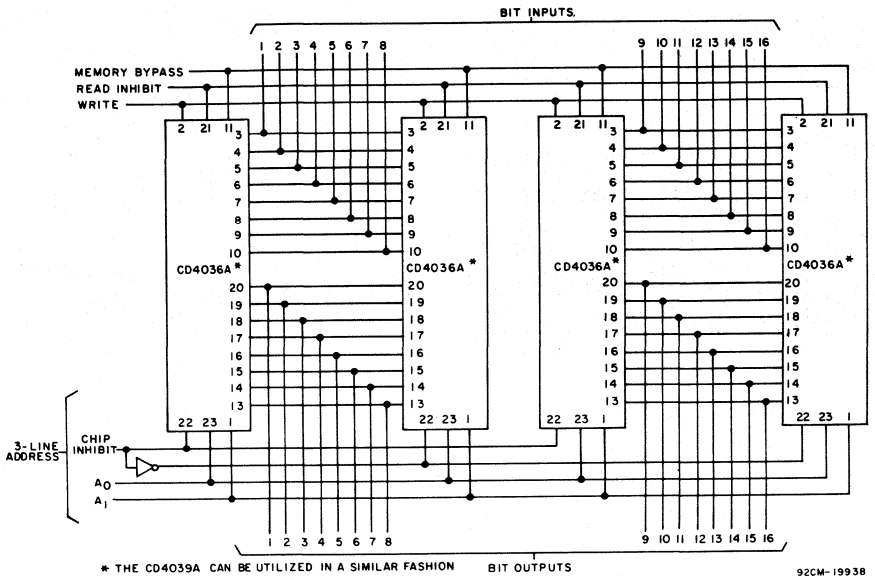
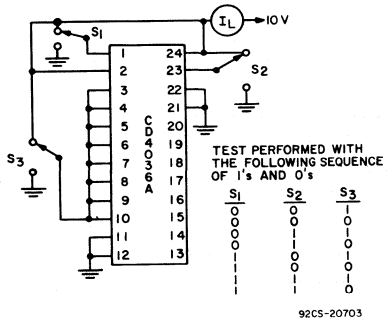
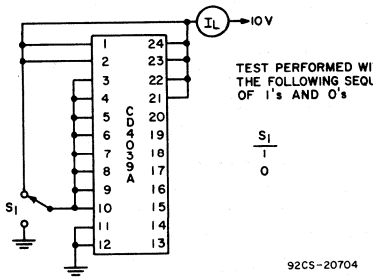


Fig. 11—General-purpose memory storage — 8 words x 16 bits (RAM or ROM).

TEST CIRCUITS





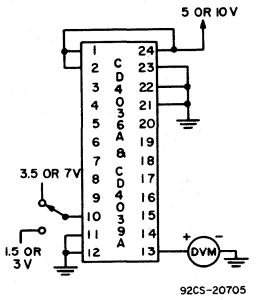


Fig. 12—Quiescent current (CD4036A).

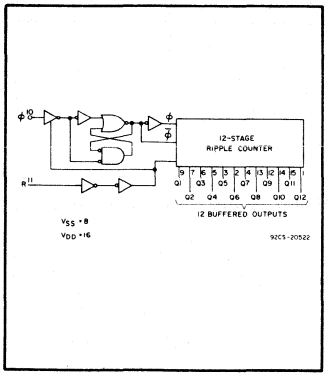
Fig. 13—Quiescent current (CD4039A).

Fig. 14—Noise immunity.

RCA Solid State Division

Digital Integrated Circuits
Monolithic Silicon

High-Reliability Slash(/) Series
CD4040A/...



High-Reliability COS/MOS 12-Stage Ripple-Carry Binary Counter/Divider

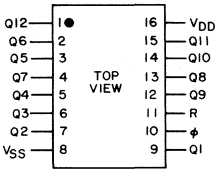
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Medium-speed operation . . . . .5-MHz (typ.) input pulse rate at $V_{DD}-V_{SS}$ = 10V**
- **Low "high"- and "low"-level output impedance . . . . . 750 Ω (typ.) at $V_{DD}-V_{SS}$ = 10 V and V_{DS} = 0.5 V**
- **Common reset**
- **Fully static operation**
- **All 12 buffered outputs available**
- **Low-power TTL compatible**

Applications:

- **Frequency-dividing circuits**
- **Time-delay circuits**
- **Control counters**



TERMINAL ASSIGNMENT
CD4040AD
CD4040AK

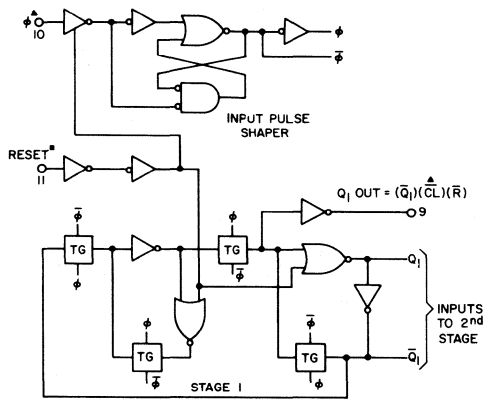
92CS-22901

RCA CD4040A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

These devices are electrically and mechanically identical with standard COS/MOS CD4040A types described in data bulletin 624 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4040A "Slash" (/) Series can be supplied to six screening levels --- /1N, /1R, /1, /2, /3, /4 --- which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels --- /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the



■ R=HIGH DOMINATES (RESETS ALL STAGES)

▲ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE. COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE φ TRANSITION (4096 TOTAL BINARY COUNTS).

92CM-20748R1

Fig. 1—Logic diagram of CD4040A input pulse shaper and 1 of 12 stages.

COS/MOS high-reliability integrated circuit part number, see the following page.

The CD4040A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic packages ("K" suffix), or in chip form ("H" suffix).

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4040AK, CD4040AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4040AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4040AD/1N

CD4040A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic	/1N
	K = Ceramic Flat-Pack	/1R
		/1
		/2
		/3
		/4

Chip Version, CD4040AH/N

CD4040A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N
		/R

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} < V_I < V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

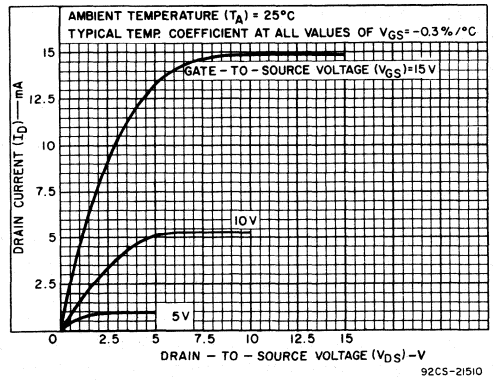


Fig. 2—Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	LIMITS CD4040AD, CD4040AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device Current	I_L		5	–	–	15	–	0.5	15	–	–	900	μA	12	1
			10	–	–	25●	–	1	25●	–	–	500●			
Quiescent Device Dissipation/Package	P_D		5	–	–	75	–	2.5	75	–	–	4500	μW	–	–
			10	–	–	250	–	10	250	–	–	5000			
Output Voltage Low-Level	V_{OL}	Fanout of 50 COS/MOS Inputs	3	–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -20\ \mu A$		−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	$V_{TH}P$	$I_D = 20\ \mu A$		0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}	0.8	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	10, 11	1
For Definition, See Appendix SSD-207		1	10	3●	–	–	3●	4.5	–	2.9●	–	–			
	V_{NH}	4.2	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		9	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_DN	0.5	5	0.22	–	–	0.18●	0.36	–	0.125	–	–	mA	2, 4	2
		0.5	10	0.44	–	–	0.36●	0.75	–	0.25	–	–			
P-Channel	I_DP	4.5	5	−0.15	–	–	−0.125●	−0.25	–	−0.085	–	–	mA	3, 5	2
		9.5	10	−0.3	–	–	−0.25●	−0.5	–	−0.175	–	–			
Diode Test, 100 μA Test Pin	V_{DF}			–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

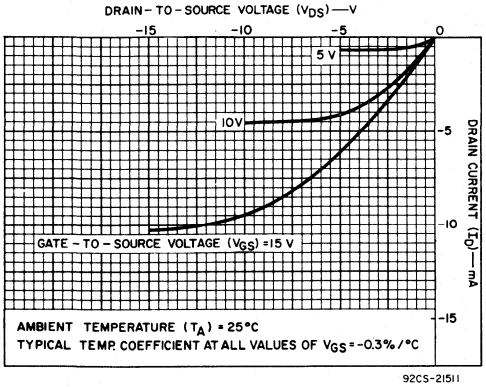


Fig. 3—Typical p-channel drain characteristics.

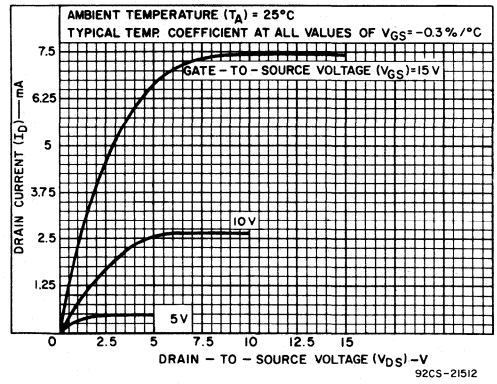


Fig. 4—Minimum n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS, *At T_A = 25°C, V_{SS} = 0V, C_L = 15 pF (unless otherwise specified), and input rise and fall times = 20 ns, except t_fCL and t_fCL. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4040AK, AD			UNITS	NOTE
			V_{DD}	Min.	Typ.	Max.		
Input-Pulse Operation								
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	300	400	ns	1, 4
			10	–	150	200●		
Transition Time	t_{THL}, t_{TLH}		5	–	150	300	ns	4
			10	–	75	150●		
Min. Input-Pulse Width	t_{WL}, t_{WH}	f = 100KHz	5	–	200	400	ns	–
			10	–	75	110		
Input-Pulse Rise & Fall Time	$t_{r\phi}$, $t_{f\phi}$		5	–	–	15	μs	2, 4
			10	–	–	7.5●		
Max. Input-Pulse Frequency	f_ϕ		5	1.5	1.75	–	MHz	4
			10	5●	6	–		
Input Capacitance	C_I	Any input		–	5	–	pF	
Reset Operation								
Propagation Delay Time	t_{PHL}		5	–	500	1000	ns	3
			10	–	250	500		
Minimum Reset Pulse Width	t_{WH}		5	–	500	1000	ns	–
			10	–	250	500		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTES:

1. Measured from the 50% level of the negative clock edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.
2. Maximum input rise or fall time for functional operation.
3. Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).
4. Test is a one input one output only.

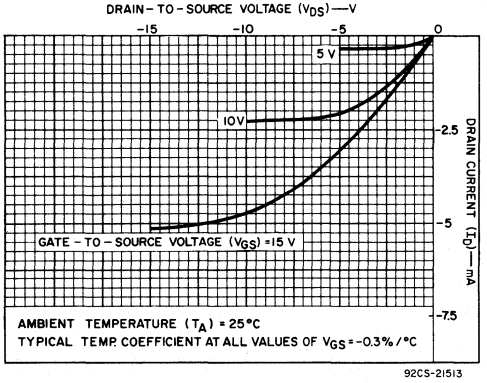


Fig. 5—Minimum p-channel drain characteristics.

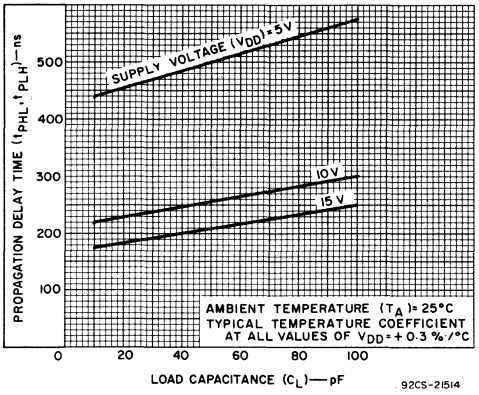


Fig. 6—Typical propagation delay time vs. load capacitance (per stage).

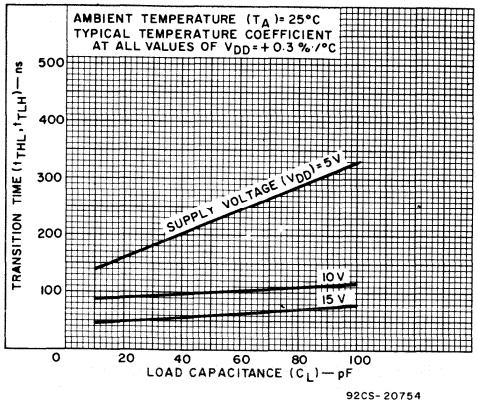


Fig. 7—Typical transition time vs. load capacitance.

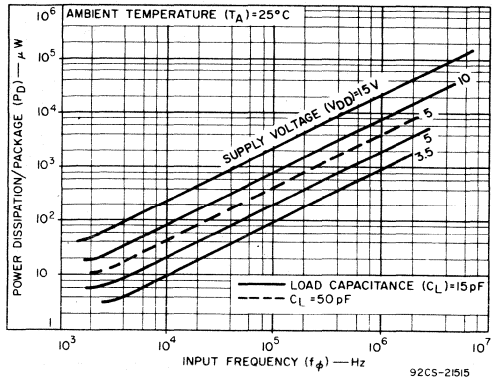


Fig. 8—Typical dissipation characteristics.

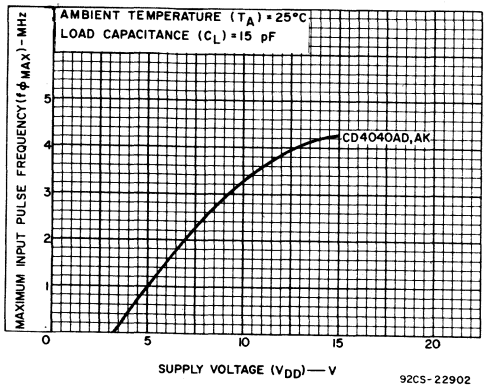


Fig. 9—Maximum input-pulse frequency vs. supply voltage.

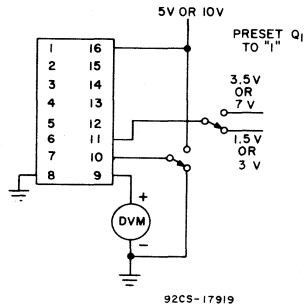


Fig. 10—Reset-noise-immunity test circuit.

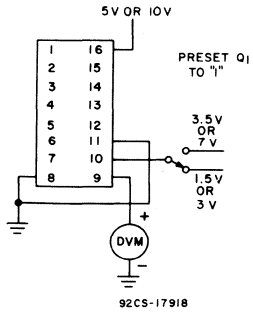


Fig. 11—Input-pulse noise-immunity test circuit.

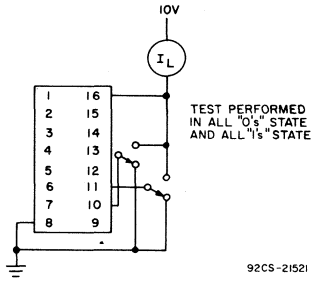


Fig. 12—Quiescent-device-current test circuit.

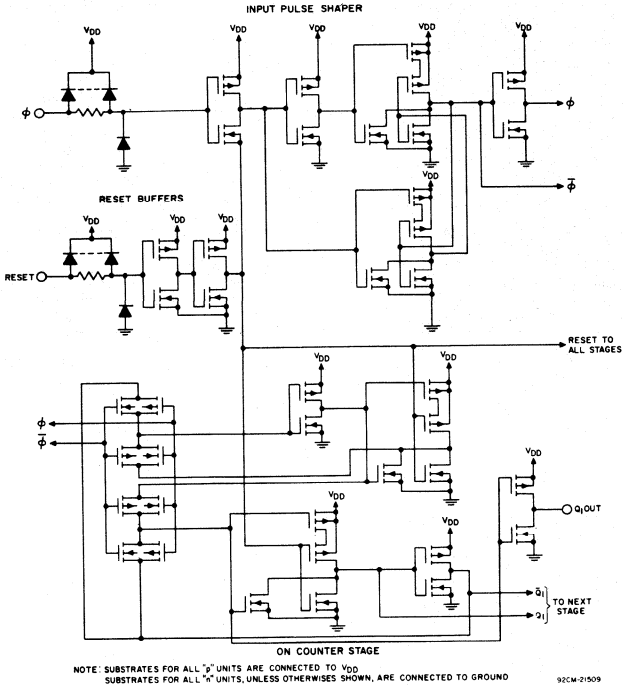


Fig. 13—Schematic diagram of input shaping, reset buffers, and one counter stage of CD4040A.

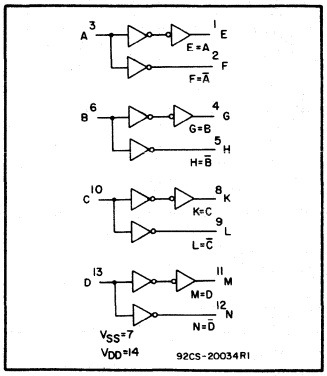
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4041A/...



High-Reliability COS/MOS Quad True/Complement Buffer

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

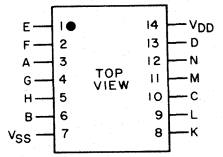
Features:

True Output

- **High current source and sink capability**
  8 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  3.2 mA (typ.) @ V_{DS} = 0.4 V, V_{DD} = 5 V
  (two TTL loads)

Complement Output

- **Medium current source and sink capability**
  3.6 mA (typ) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  1.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 5 V



TERMINAL ASSIGNMENT
CD4041AD
CD4041AK

92CS-20755

RCA CD4041A "Slash" (/) Series types are high-reliability COS/MOS integrated circuit Quad True/Complement Buffers designed for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4041A consists of n-and p-channel units having low channel resistance and high current (source and sink) capability. It is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can also be used as an ultra-low power resistor-network driver, and in other applications where high noise immunity and low power dissipation are primary design requirements.

These devices are electrically and mechanically identical with standard COS/MOS CD4041A types described in data bulletin 572 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4041A "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /N, /R, and standard chip. For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with RCA high-reliability devices, refer to High-Reliability Report RIC-102B "High-Reliability CD4000S Slash (/) Series Types", For a list of the Screening Level Options available for both packaged devices and chips and for a description of the high-reliability part numbers, see the following page.

Applications:

- **High current source/sink driver**
- **COS/MOS-to-DTL/TTL converter**
- **Display driver**
- **MOS clock driver**
- **Resistor network driver (Ladder or weighted R)**
- **Buffer**
- **Transmission line driver**

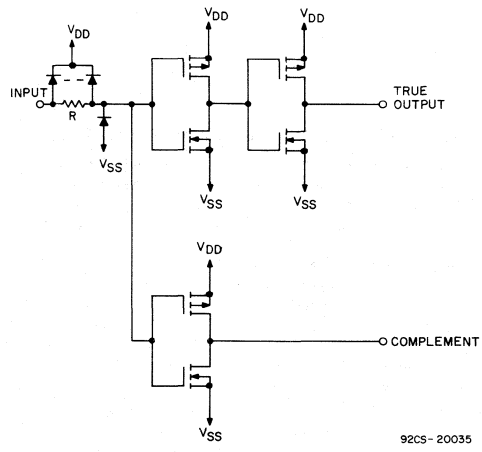


Fig. 1 – CD4041A schematic diagram.

The CD4041A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in the 14-lead ceramic flat package ("K" suffix), or in chip form ("H" suffix).

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4041AD CD4041AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4041AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4041AD/1N

CD4041A, D, /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4041AH/N

CD4041A, H, /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range	−65°C to +150	°C
Operating Temperature Range	−55°C to +125	°C
DC Supply Voltage Range ($V_{DD} - V_{SS}$)	−0.5 V to +15	V
Device Dissipation (Per Pkg.)	200	mW
Average Dissipation Per Output	100	mW
Allowable Input Rise and Fall Time vs Supply and Frequency	See Fig. 17	
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply Voltage ($V_{DD} - V_{SS}$)	3 to 15	V
Recommended Input Voltage Swing	V_{DD} to V_{SS}	
Lead Temperature (During soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

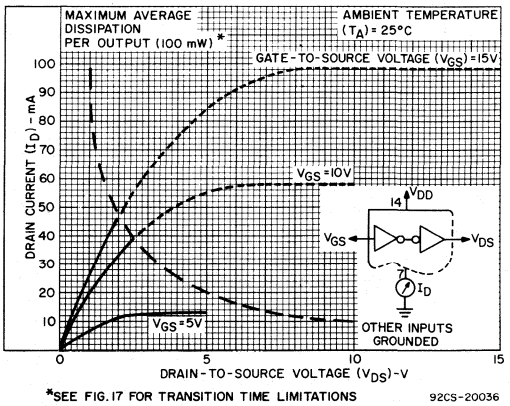


Fig.2 — Typical n-channel drain characteristics-true output.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4041AD, CD4041AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	Notes
					−55°C			25°C			125°C					
			V_O Volts	V_{DD} Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I_L	Inputs to Ground or V_{DD}		5	–	–	1	–	0.005	1	–	–	60	μA	18	1
				10	–	–	2●	–	0.005	2●	–	–	40●			
Quiescent Device Dissipation/Package	P_D			5	–	–	5	–	0.025	5	–	–	300	μW		
				10	–	–	20	–	0.05	20	–	–	400			
Output Voltage: Low-Level	V_{OL}	Fan-out of 50 COS/MOS Inputs		3			0.55●			0.50●				V	10, 11	1
				5	–	–	0.01	–	0	0.01			0.05			
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15						0.50●			0.55●			1
High-Level	V_{OH}			3	2.25●			2.3●						V		1
				5	4.99	–	–	4.99	5	–	4.95	–	–			
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15				14.40●			14.45●					1
Threshold Voltage: N-Channel	V_{THN}	$I_D = -10\ \mu A$			−0.7●	−1.7	−3.0●	−0.7●	−1.5	−3.0●	−0.3●	−1.3	−3.0●	V		2
P-Channel	V_{THP}	$I_D = 10\ \mu A$			0.7●	1.7	3.0●	0.7●	1.5	3.0●	0.3●	1.3	3.0●	V		
Noise Immunity▲ (All Inputs)	V_{NL}	True Output	0.95	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	19	
			2.9	10	3●	–	–	3●	4.5	–	2.9●	–	–			
	V_{NH}		3.6	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
			7.2	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_DN	True Output	0.4	5	2.1	–	–	1.6●	3.2	–	1.2	–	–	mA	2,6	2
			0.5	10	6.25●	–	–	5●	10	–	3.5●	–	–			
		Complement Output	0.5	5	1	–	–	0.8●	1.6	–	0.55	–	–		4,8	
			0.5	10	2.5●	–	–	2●	4	–	1.4	–	–			
P-Channel	I_DP	True Output	4.5	5	−1.75	–	–	−1.4●	−2.8	–	−1	–	–	mA	3,7	
			9.5	10	−5●	–	–	−4●	−8	–	−2.8●	–	–			
		Complement Output	4.5	5	−0.75	–	–	−0.6●	−1.2	–	−0.4	–	–		5,9	
			9.5	10	−2.25	–	–	−1.8●	−3.6	–	−1.25●	–	–			
Diode Test		10 μA at any input or output					1.5●			1.5●			1.5●	V		3
Input Current	I_I	Any Input			–	–	–	–	10	–	–	–	–	pA		

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs. ▲ Values shown are for True Output.
Note 2: Test is either a one input or a one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .

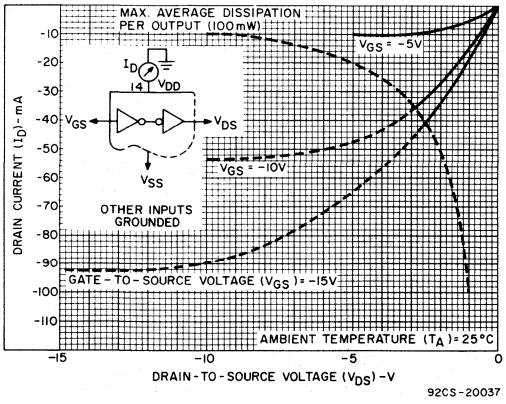


Fig.3 — Typical p-channel drain characteristics-true output.

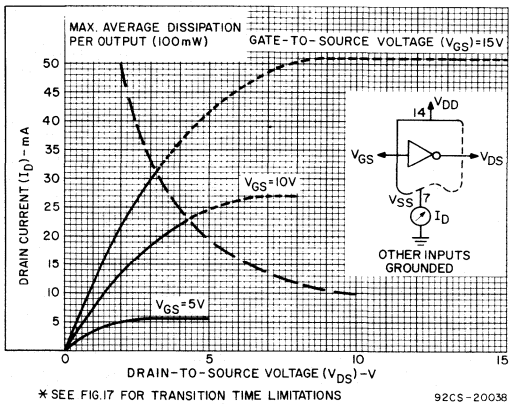


Fig.4 — Typical n-channel drain characteristics-complement output.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C and C_L = 15pF
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4041AD, CD4041AK MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.
Propagation Delay Time: High-to-Low Level	t_{PHL}	True Output	5	–	65	115	ns	Note 1
			10	–	40	75 •		–
		Complement Output	5		55	100	ns	Note 1
			10		30	45 •		
Low-to-High Level	t_{PLH}	True Output	5	–	75	125	ns	Note 1 14
			10	–	45	75 •		
		Complement Output	5	–	45	100	ns	Note 1 15
			10	–	25	40 •		
Transition Time: High-to-Low Level	t_{THL}	True Output	5	–	20	40	ns	Note 1 12
			10	–	13	25 •		
		Complement Output	5	–	40	60	ns	Note 1 13
			10	–	25	40 •		
Low-to-High Level	t_{TLH}	True Output	5	–	20	40	ns	Note 1 12
			10	–	13	25 •		
		Complement Output	5	–	35	55	ns	Note 1
			10	–	25	40 •		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input one output only.

DYNAMIC ELECTRICAL CHARACTERISTICS (Driving TTL,DTL) AT T_A = 25°C, $V_{DD}-V_{SS}$ = 5V, C_L = 15pF (True Output)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Driving TTL,DTL	LIMITS CD4041AD CD4041AK MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES Fig. No.
Propagation Delay Time: High-To-Low Level	t_{PHL}	R_L = 2kΩ	Med. Power	–	75	150	ns	–
		R_L = 20kΩ	Low Power	–	75	150		
Low-To-High Level	t_{PLH}	R_L = 2kΩ	Med. Power	–	85	175	ns	–
		R_L = 20kΩ	Low Power	–	85	175		
Transition Time	t_{THL} = t_{TLH}	R_L = 2kΩ	Med. Power	–	20	50	ns	–
		R_L = 20kΩ	Low Power	–	20	50		

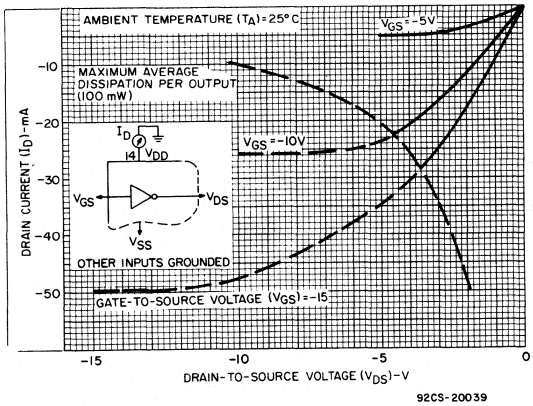


Fig.5 – Typical p-channel drain characteristics-complement output.

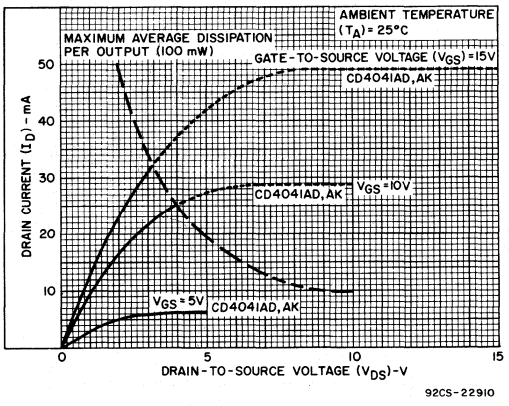


Fig.6 – Minimum n-channel drain characteristics-true output.

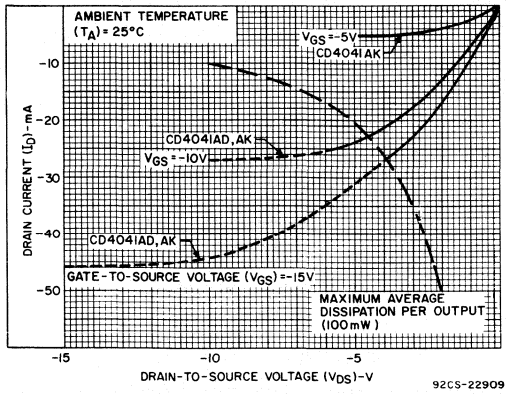


Fig.7 – Minimum p-channel drain characteristics-true output.

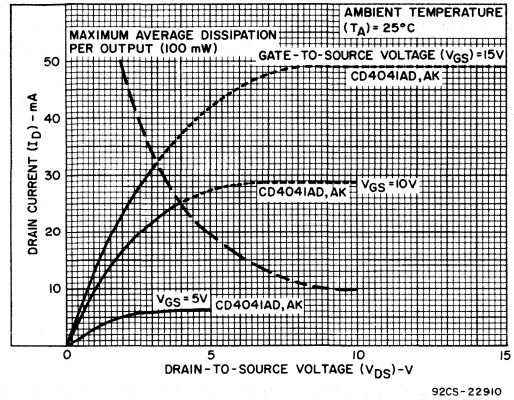


Fig.8 – Minimum n-channel drain characteristics-complement output.

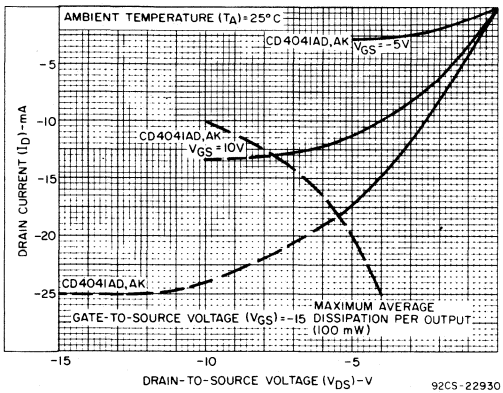


Fig.9 – Minimum p-channel drain characteristics-complement output.

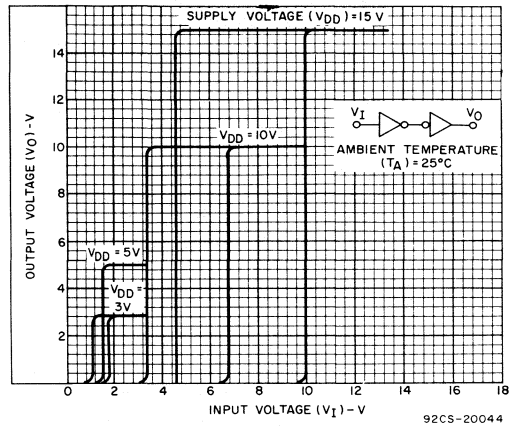


Fig.10 – Minimum and maximum transfer characteristics-true output.

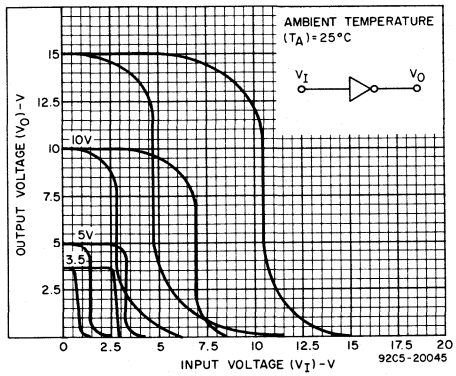


Fig.11 – Minimum and maximum transfer characteristics-complement output.

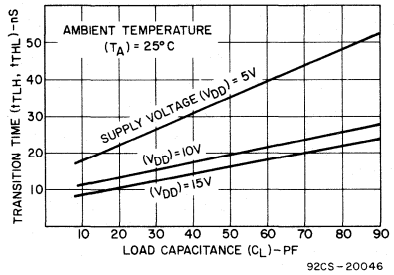


Fig.12 – Typical transition time vs. C_L-true output.

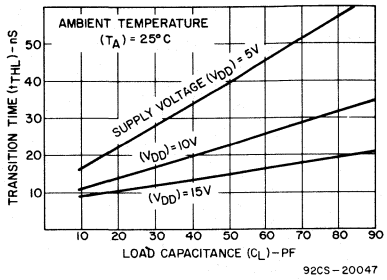


Fig.13 – Typical high-to-low level transition time vs. C_L-complement output.

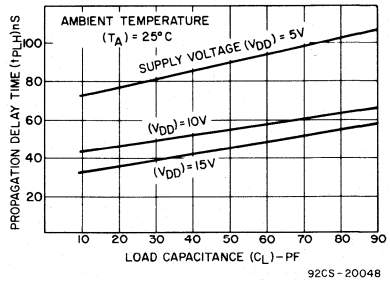


Fig.14 – Typical low-to-high level propagation delay time vs. C_L-true output.

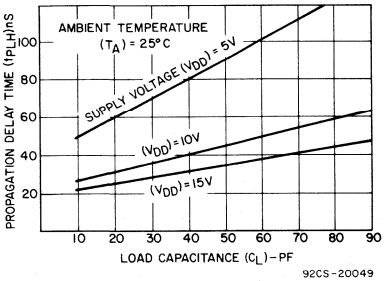


Fig.15 – Typical low-to-high level propagation delay time vs. C_L-complement output.

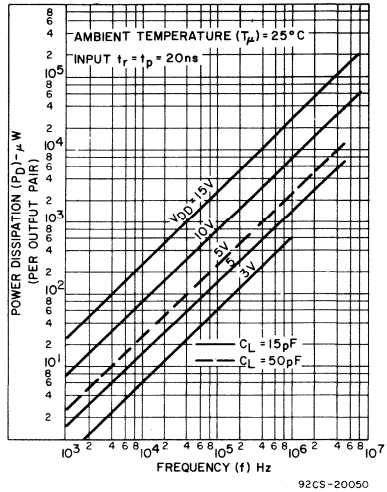


Fig.16 – Typical power dissipation vs. frequency per output pair

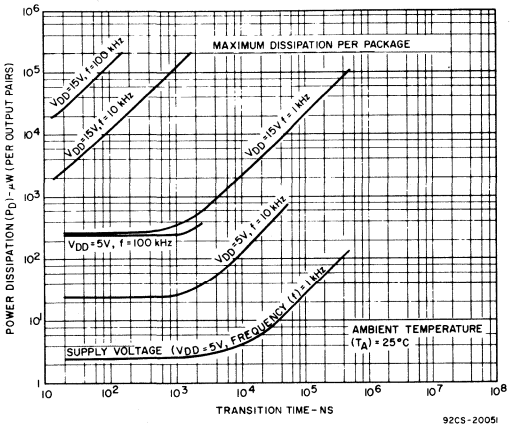


Fig.17 – Typical power dissipation vs. input rise & fall time per output pair.

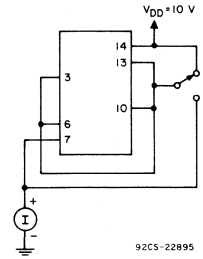


Fig.18 – Quiescent device current test circuit.

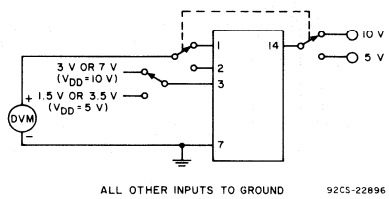


Fig.19 – Noise immunity test circuit.

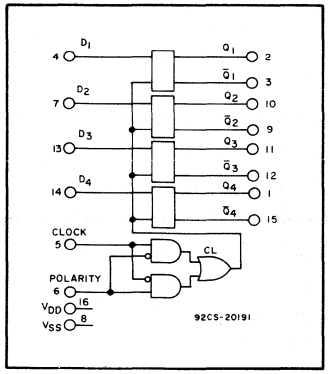
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4042A/...



High-Reliability COS/MOS Quad Clocked "D" Latch

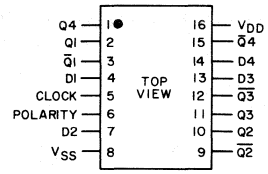
For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- Medium Speed Operation . . . $t_{PHL} = t_{PLH} = 50$ ns (typ) at $V_{DD} = 10$ V and $C_L = 15$ pF
- Clock Polarity Control
- Q and $\overline{Q}$ Outputs
- Common Clock
- Low Power TTL Compatible

Applications:

- Buffer Storage
- Holding Register
- General Digital Logic



TERMINAL ASSIGNMENT
CD4042AD
CD4042AK

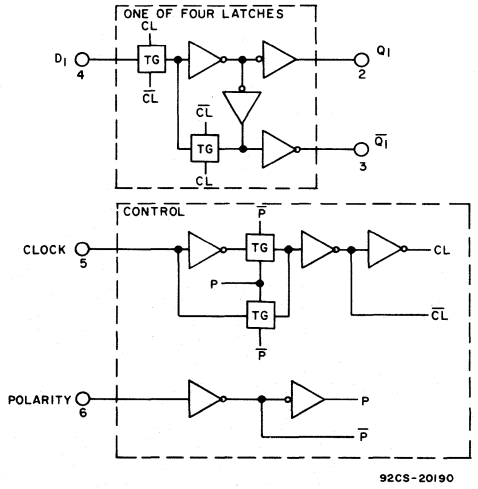
92CS-20756

RCA CD4042A "Slash" (/) Series are high-reliability COS/MOS integrated circuit Quad Clocked "D" Latches intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4042A types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) in information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

These devices are electrically and mechanically identical with standard COS/MOS CD4042A types described in data bulletin 589 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4042A "Slash" (/) Series can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and



CLOCK	POLARITY	Q
0	0	D
⌐	0	LATCH
1	1	D
¬	1	LATCH

Fig.1 — Logic block diagram & truth table.

"C". The chip versions of these types can be supplied to three screening levels – /N, /R, and standard chip. For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types",

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the tables below.

The CD4042A "Slash" (/) Series types are supplied in 16-lead welded-seal dual-in-line ceramic packages ("D" suffix), in the 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4042AD CD4042AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4042AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4042AD/1N

CD4042A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic	/1N
	K = Ceramic Flat-Pack	/1R
		/1
		/2
		/3
		/4

Chip Version, CD4042AH/N

CD4042A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N
		/R

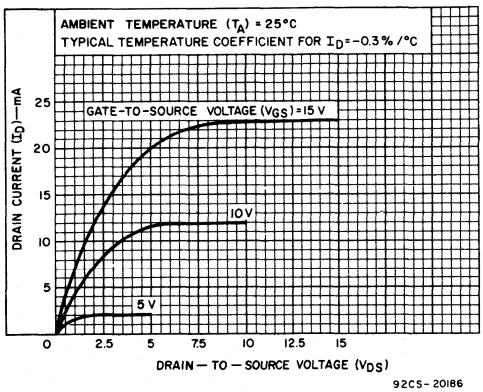


Fig.2 – Typ. n-channel drain characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

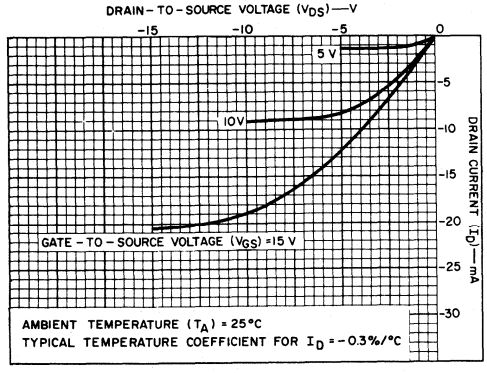
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS CD4042AD, CD4042AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	Notes
Quiescent Device Current	I_L	Inputs to Ground or V_{DD}		5	—	—	1	—	0.005	1	—	—	60	μA	8	1
				10	—	—	2●	—	0.005	2●	—	—	40●			
Quiescent Device Dissipation/Package	P_D			5	—	—	5	—	0.025	5	—	—	300	μW	—	—
				10	—	—	20	—	0.05	20	—	—	400			
Output Voltage: Low-Level	V_{OL}	Fan-out of 50 COS/MOS Inputs		3			0.55●			0.50●				V	—	1
				5	—	—	0.01	—	0	0.01			0.05			—
				10	—	—	0.01	—	0	0.01	—	—	0.05			—
				15						0.50●			0.55●			1
High-Level	V_{OH}			3	2.25●			2.3●						V	—	1
				5	4.99	—	—	4.99	5	—	4.95	—	—			—
				10	9.99	—	—	9.99	10	—	9.95	—	—			—
				15				14.5●			14.45●					1
Threshold Voltage: N-Channel	V_{THN}	$I_D = -10$ μA			−0.7●	−1.7	−3.0●	−0.7●	−1.5	−3.0●	−0.3●	−1.3	−3.0●	V	—	2
P-Channel	V_{THP}	$I_D = 10$ μA			0.7●	1.7	3.0●	0.7●	1.5	3.0●	0.3●	1.3	3.0●	V		
Noise Immunity (All Inputs)	V_{NL}		0.95	5	1.5	—	—	1.5●	2.25	—	1.4	—	—	V	9	1
			2.9	10	3●	—	—	3●	4.5	—	2.9●	—	—			
	V_{NH}		3.6	5	1.4	—	—	1.5●	2.25	—	1.5	—	—	V		
			7.2	10	2.9●	—	—	3●	4.5	—	3●	—	—			
Output Drive Current: N-Channel	I_{DN}		0.5	5	0.5	—	—	0.4●	1	—	0.27	—	—	mA	—	2
			0.5	10	1.25	—	—	1●	2	—	0.7	—	—	mA	—	
P-Channel	I_{DP}		4.5	5	−0.45	—	—	−0.35●	−1	—	−0.25	—	—		—	2
			9.5	10	−1.15	—	—	−0.9●	−2	—	−0.6	—	—		—	
Diode Test	V_{DF}	10 μA at any input or output			—	—	1.5●	—	—	1.5●	—	—	1.5●	—	—	3
Input Current	I_I	Any Input			—	—	—	—	10	—	—	—	—	pA	—	—

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.

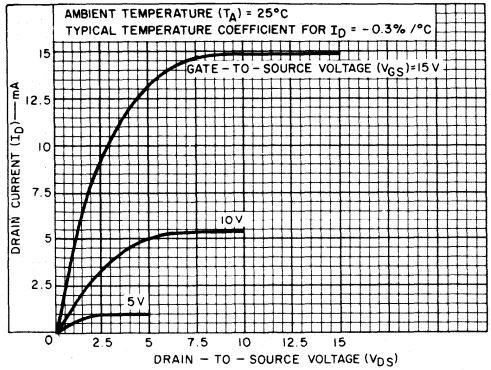
Note 2: Test is either a one input or a one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix .



92CS-20187

Fig.3 — Typ. p-channel drain characteristics.



92CS-22848

Fig.4 — Min. n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = OV, C_L = 15pF, and input rise and fall times = 20 ns, except t_rCL and t_fCL.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS CD4042AD, CD4042AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
		V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time	t_{PHL}, t_{PLH}	5	–	150	300	ns	–	1
		10	–	75	125●			
Transition Time	t_{THL}, t_{TLH}	5	–	100	200	ns	–	1
		10	–	50	100●			
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5	–	175	250	ns	–	–
		10	–	50	75			
Clock Rise & Fall Time	t_{rCL}, t_{fCL}	5		–	15	μs	–	1
		10		–	5●			
Set-Up Time		5	–	50	100	ns	–	–
		10	–	25	50			
Input Capacitance	C_I	–	–	5	–	pF	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is a one input , one output only.

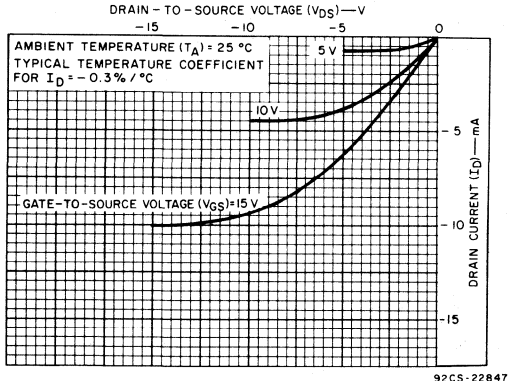


Fig.5 – Min. p-channel drain characteristics.

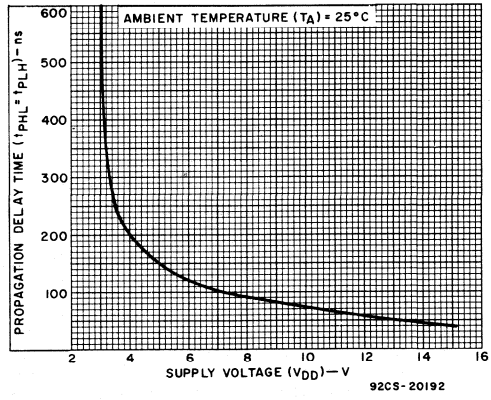


Fig.6 – Typical propagation delay time vs. V_{DD}.

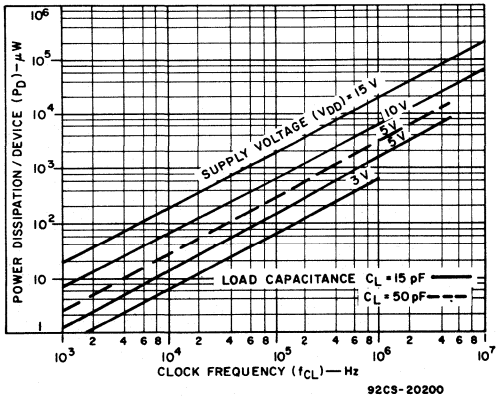


Fig.7 – Typical dissipation characteristics.

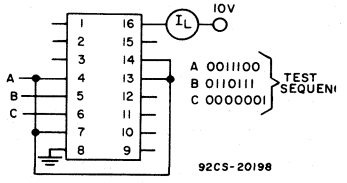


Fig.8 – Quiescent device current.

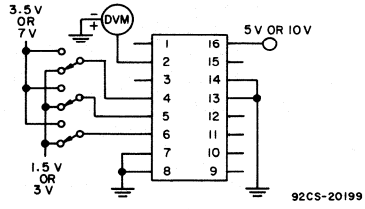


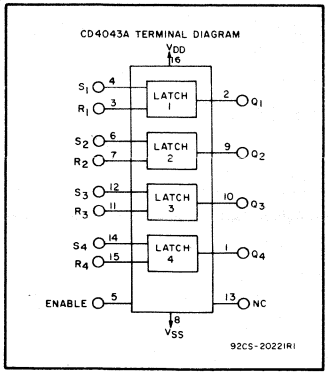
Fig.9 – Noise immunity.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4043A/..., CD4044A/...



High-Reliability COS/MOS Quad 3-State R/S Latches

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Quad NOR R/S Latch – CD4043A

Quad NAND R/S Latch - CD4044A

Special Features:

- **Medium Speed Operation**
- **3-Level Outputs with Common Output Enable**
- **Separate Set and Reset Inputs for Each Latch**
- **Low Power TTL Compatible**
- **NOR and NAND Configurations**

Applications:

- **Holding Register in Multi-Register System**
- **Four Bits of Independent Storage with Output Enable**
- **Strobed Register**
- **General Digital Logic**

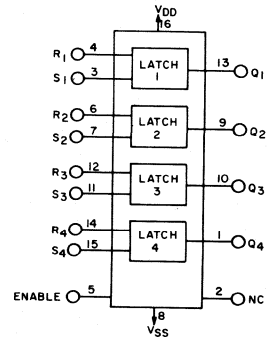
RCA-CD4043A and CD4044A "Slash" (/) Series are high-reliability COS/MOS integrated circuit Quad 3-State R/S Latches intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4043A types are quad cross-coupled 3-State NOR latches; the CD4044A types, quad cross-coupled 3-State NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are gated through transmission gates controlled by a common ENABLE input. A logic "1" or "high" on the ENABLE input connects the latch states to the Q outputs. A logic "0" or "low" on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs. The logic operation of the latches is summarized in the truth table on the following page.

These devices are electrically and mechanically identical with standard COS/MOS CD4043A and CD4044A types described in data bulletin 590 and DATABOOK SSD-203B Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4043A and CD4044A "Slash" (/) Series can be supplied to six screening levels —/1N,/1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C".The chip versions of these types can be supplied to three screening levels — /N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types",*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the following page.

The CD4043A and CD4044A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).



CD4044A Terminal Diagram

Table I — Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4043AD, CD4043AK, CD4044AD, CD4044AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4043AH, CD4044AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II — Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4043AD/1N

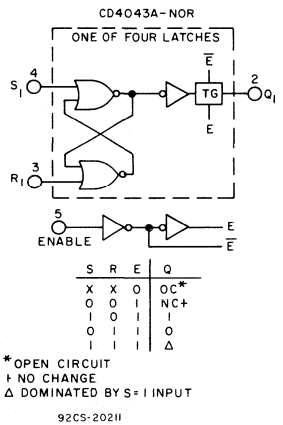
CD4043A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4043AH/N

CD4043A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R



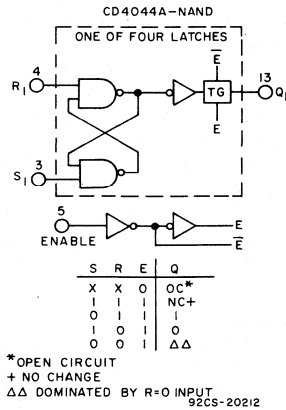


Fig. 1—Logic diagrams & truth tables.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} Volts	LIMITS CD4043AD, CD4043AK, CD4044AD, CD4044AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	Notes
Quiescent Device Current	I_L	Inputs to Ground or V_{DD}	5	–	–	1	–	0.005	1	–	–	60	μA	11	1
			10	–	–	2●	–	0.005	2●	–	–	40●			
Quiescent Device Dissipation/Package	P_D		5	–	–	5	–	0.025	5	–	–	300	μW		–
			10	–	–	20	–	0.05	20	–	–	400			
Output Voltage: Low-Level	V_{OL}	Fan-out of 50 COS/MOS inputs	3	–	–	0.55●	–	–	0.5●	–	–	–	V		1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3	2.25●	–	–	2.3●	–	–	–	–	–	V		1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D = -10\ \mu A$		−0.7●	−1.7	−3.0●	−0.7●	−1.5	−3.0●	−0.3●	−1.3	−3.0●	V		2
P-Channel	V_{THP}	$I_D = 10\ \mu A$		0.7●	1.7	3.0●	0.7●	1.5	3.0●	0.3●	1.3	3.0●	V		
Noise Immunity (All Inputs)	V_{NL}	$V_O = 0.95$ V	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	12	1
		$V_O = 2.9$ V	10	3●	–	–	3●	4.5	–	2.9●	–	–			
	V_{NH}	$V_O = 3.6$ V	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
		$V_O = 7.2$ V	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_{DN}	$V_O = 0.5$ V	5	0.25	–	–	0.2●	0.5	–	0.14	–	–	mA	4, 6	2
			10	0.61	–	–	0.5●	1	–	0.35	–	–			
P-Channel	I_{DP}	$V_O = 4.5$ V	5	−0.22	–	–	−0.175●	−0.5	–	−0.12	–	–	mA	5, 7	2
		$V_O = 9.5$ V	10	−0.5	–	–	−0.4●	−1	–	−0.28	–	–			
Diode Test	V_{DF}	100 μA at any input or output		–	–	1.5●	–	–	1.5●	–	–	1.5●	V		3
Input Current	I_I	Any Input		–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{SS} = 0V$, $C_L = 15pF$, and input rise and fall times = 20 ns, except t_rCL and t_fCL.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4043AD, CD4043AK CD4044AD, CD4044AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES Fig. No.	NOTES
Propagation Delay Time	t_{PHL}, t_{PLH}		5	–	175	350	ns	8	1
			10	–	75	175●			
Transition Time	t_{THL}, t_{TLH}		5	–	100	200	ns	9	1
			10	–	50	100●			
Minimum Set and Reset Pulse Width	$t_{WH(S)}$, $t_{WH(R)}$		5	–	80	200	ns	–	1
			10	–	40	100●			
Input Capacitance	C_I		–	–	5	–	pF	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Test is one input or a one output only.

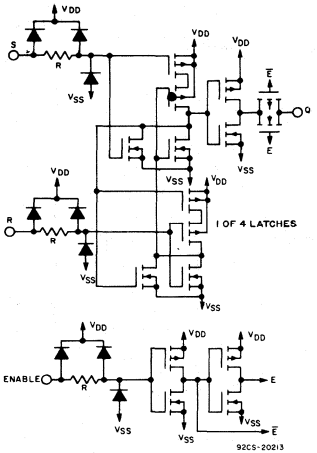


Fig.2—Schematic diagram—CD4043A.

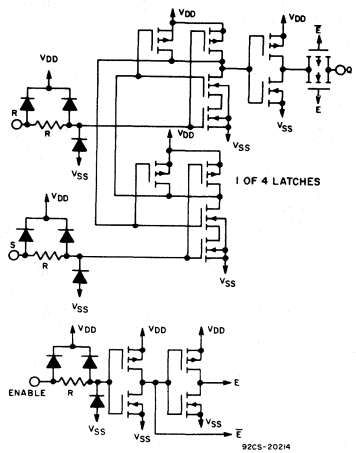


Fig.3—Schematic diagram-CD4044A.

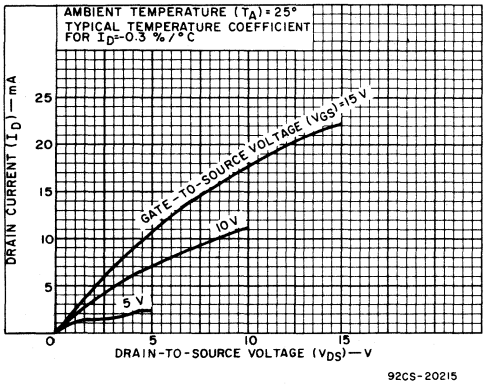


Fig.4—Typical n-channel drain characteristics.

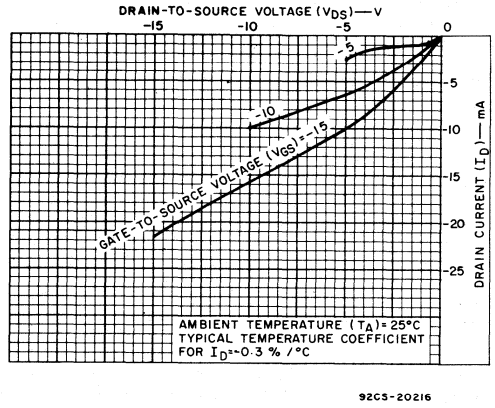


Fig.5—Typical p-channel drain characteristics.

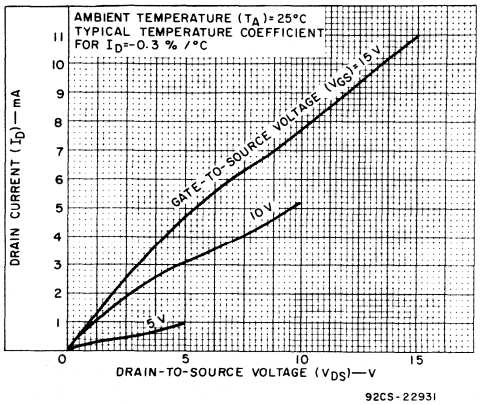


Fig.6—Min. n-channel drain characteristics.

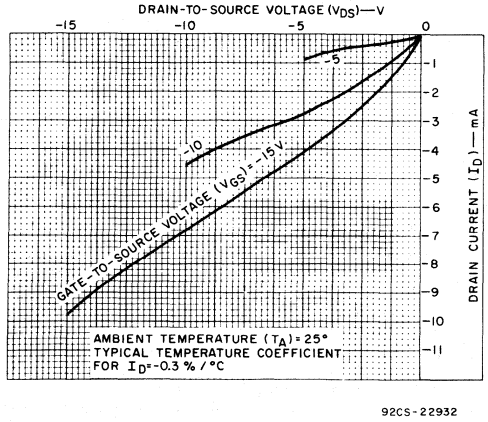


Fig.7—Min. p-channel drain characteristics.

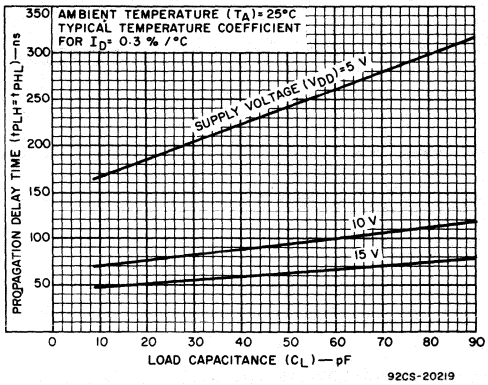


Fig.8—Typ. propagation delay time vs. C_L.

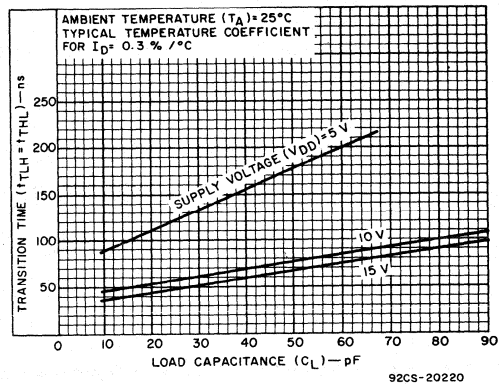


Fig.9—Typ. transistion time vs. C_L.

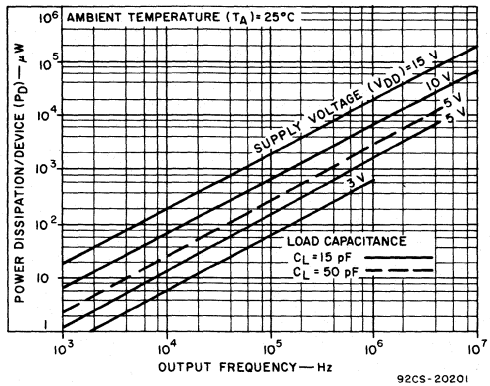


Fig.10—Typ. dissipation characteristics.

TEST CIRCUITS

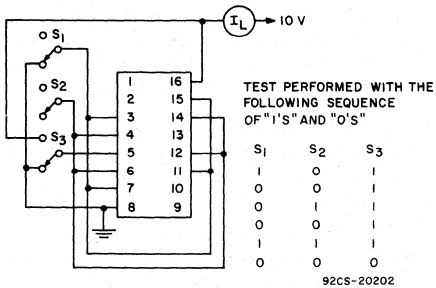


Fig.11—Quiescent current.

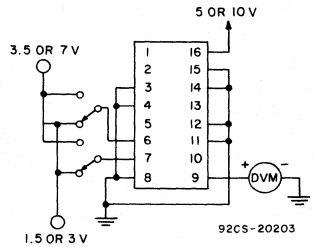


Fig.12—Noise immunity.

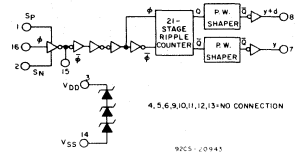
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4045A/...



CD4045A Block Diagram

High-Reliability COS/MOS 21-Stage Counter

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**

RCA CD4045A "Slash" (/) Series types are high-reliability COS/MOS integrated circuit 21-Stage Counters intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4045A is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, three 5.5 V zener diodes (providing transient protection at 16.5 V), and input inverters for use in a crystal oscillator. This device may be operated over a 3-to-15 V supply voltage range. The CD4045A configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired.

A crystal oscillator circuit can be made less sensitive to voltage supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_P to V_{DD}, S_N to V_{SS}). See Fig. 1.

These devices are electrically and mechanically identical with standard COS/MOS CD4045A types described in data bulletin 614 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4045A "Slash" (/) Series can be supplied to six screening levels—/1N, /1R, /1, /2, /3, /4—which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels—/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types"*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the following page.

The CD4045A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Features:

- **Operation from 3 to 15 volts**
- **Microwatt quiescent dissipation . . .**
  2.5 μW (typ.) @ V_{DD} = 5 V; 10 μW (typ.) @ V_{DD} = 10 V
- **Very-low operating dissipation . . .**
  1 mW (typ.); @ V_{DD} = 5 V, fϕ = 1 MHz
- **Output drivers with sink or source capability . . .**
  7 mA (typ.) @ V_O = 0.5 V, V_{DD} = 5 V (sink)
  5 mA (typ.) @ V_O = 4.5 V, V_{DD} = 5 V (source)
- **Medium speed (typ.) . . . fϕ = 5 MHz @ V_{DD} = 5 V**
  fϕ = 10 MHz @ V_{DD} = 10 V
- **16.5 V zener diode transient protection on chip for automotive use**

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4045AD CD4045AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4045AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

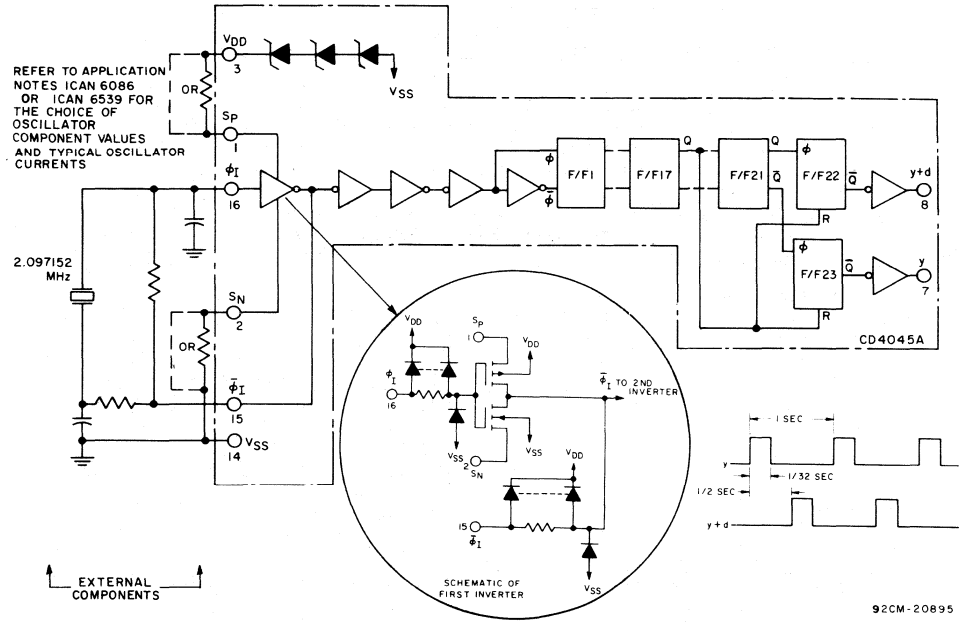


Fig. 1– CD4045A and outboard components in a typical 21-stage counter application.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS CD4045AD,CD4045AK −55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Quiescent Device▲ Current	I_L			5	—	—	15	—	0.5	15	—	—	900	μA	11	1
				10	—	—	25●	—	1	25●	—	—	500●			
Quiescent Device▲ Dissipation/Package	P_D			5	—	—	0.075	—	0.0025	0.075	—	—	4.5	mW	—	—
				10	—	—	0.25	—	0.01	0.25	—	—	5			
Output Voltage Low-Level	V_{OL}	Driving COS/MOS		3	—	—	0.55●	—	—	0.5●	—	—	—	V		1
				5	—	—	0.01	—	0	0.01	—	—	0.05			—
				10	—	—	0.01	—	0	0.01	—	—	0.05			—
				15	—	—	—	—	—	0.50●	—	—	0.55●			1
High-Level	V_{OH}			3	2.25●	—	—	2.3●	—	—	—	—	—	V		1
				5	4.99	—	—	4.99	5	—	4.95	—	—			—
				10	9.99	—	—	9.99	10	—	9.95	—	—			—
				15	—	—	—	14.5●	—	—	14.45●	—	—			1
Threshold Voltage: N-Channel	$V_{TH}N$	$I_D = -10\ \mu A$			−0.3●	−1.7	−3●	−0.3●	−1.5	−2.8●	−0.3●	−1.3	−2.8●	V	14	2
P-Channel	$V_{TH}P$	$I_D = 10\ \mu A$			0.3●	1.7	3●	0.3●	1.5	2.8●	0.3●	1.3	2.8●		15	
Sum	V_{THS}				—	—	3.7	—	—	3.6	—	—	3.7		—	2
Noise Immunity (Any Input)	V_{NL}			5	1.5	—	—	1.5●	2.25	—	1.4	—	—	V	12	1
				10	3●	—	—	3●	4.5	—	2.9●	—	—			
	V_{NH}			5	1.4	—	—	1.5●	2.25	—	1.5	—	—			
				10	2.9●	—	—	3●	4.5	—	3●	—	—			
Output Drive Current N-Channel	I_DN		0.5	5	4.4	—	—	3.5●	7	—	2.5	—	—	mA	13	2
			0.5	10	6.9	—	—	5.5●	11	—	3.9	—	—			
P-Channel	I_DP		4.5	5	−3.1	—	—	−2.5●	−5	—	−1.8	—	—	mA		
			9.5	10	−5.6	—	—	−4.5●	−9	—	−3.2	—	—			
Input Current	I_I				—	—	—	—	10	—	—	—	—	pA	—	—
Diode Test	V_{DF}	100 μA at each input or output			—	—	1.5●	—	—	1.5●	—	—	1.5●	V	—	—
Zener Breakdown Voltage	$V_{(BR)Z}$	I = 100 μA			13.3	—	17.8	13.5	16.5	18	13.7	—	18.2	V	—	—

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A/Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.

Note 2: Test is either a one input or a one output only.

Note 3: Test on all inputs and outputs.

▲Maximum noise-free saturated Bipolar output voltage.

†Minimum noise-free saturated Bipolar output voltage.

For Noise Immunity Test Circuits, Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range:	
Ceramic packages	−55°C to +125°C
Plastic package	−40°C to +85°C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation: (Per package, including zener diodes)	200 mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Peak Zener Diode Current (Decay τ = 80 ms)	150 mA

Note 1: To minimize power dissipation in the zener diodes, and to ensure device dissipation less than 200 mW, a 150 Ω current-limiting resistor must be placed in series with the power supply for $V_{DD} > 13$ V.

Note 2: Observe power supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in all other CD4000A Series 16-lead devices).

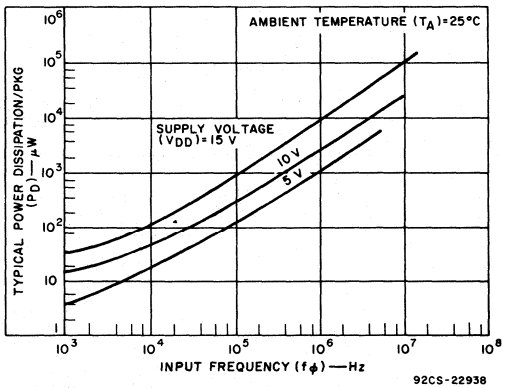


Fig. 2— Typical dissipation vs. input frequency (21 counting stages).

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns, except $t_f\phi$ and $t_f\phi$.
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{DD} (Volts)	LIMITS CD4045AD,CD4045AK Min.	Typ.	Max.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Propagation Delay Time ϕ_1 to y or y+d out	t_{PHL},	5	–	2.2	4.4	μs	8	–
	t_{PLH}	10	–	1.2	2.4			
Transition Time	t_{THL},	5	–	450	800	ns	8	–
	t_{TLH}	10	–	375	650			
Minimum Input-Pulse Width	t_{WL},	5	–	100	115	ns	–	–
	t_{WH}	10	–	50	60			
Input Pulse Rise & Fall Time	$t_r\phi$,	5	–	–	15	μs	–	–
	$t_f\phi$	10	–	–	10			
Maximum Input-Pulse Frequency	fϕ	3	50●	–	–	kHz	–	1
	$f_m\phi$	5	4.4	5	–	MHz	10	–
	$f_m\phi$	10	8.5	10	–			
	fϕ	15	2●	–	–	MHz	–	1
Input Capacitance	C_I	Any Input	–	5	–	pF	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional tests, all inputs/outputs to truth table.

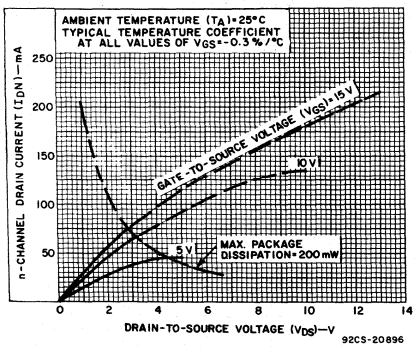


Fig. 3— Typical n-channel drain characteristics.

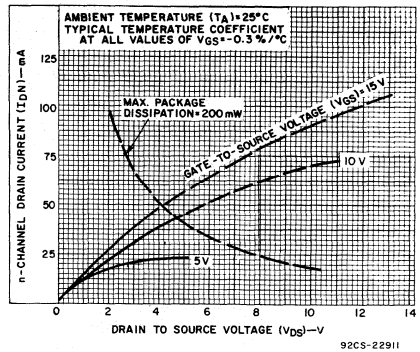


Fig. 4— Minimum n-channel drain characteristics.

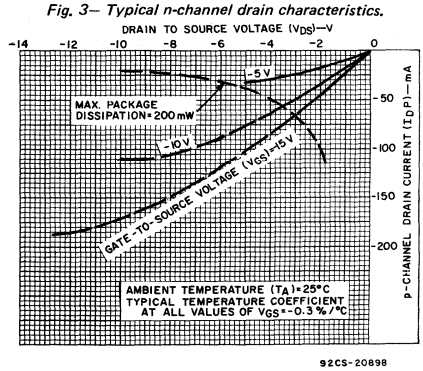


Fig. 5— Typical p-channel drain characteristics.

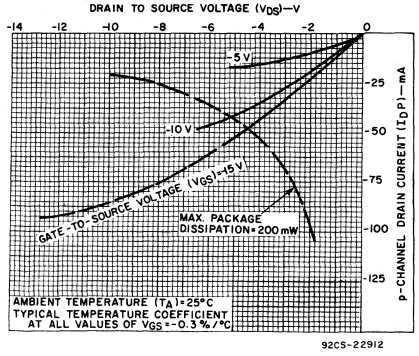


Fig. 6— Minimum p-channel drain characteristics.

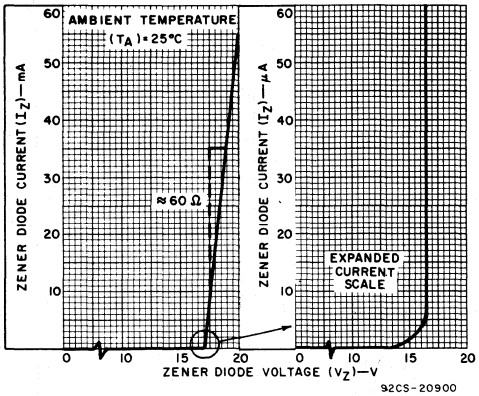


Fig. 7— Typical zener diode characteristics.

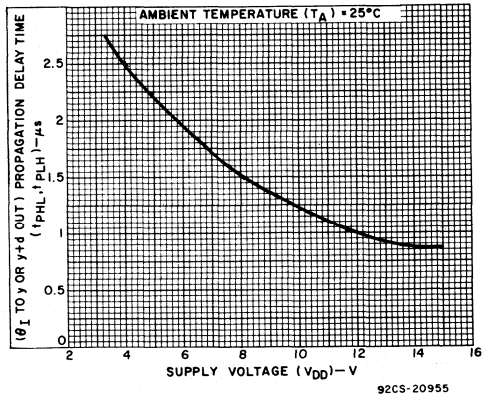


Fig. 8— Typical propagation delay (ϕ_1 to y or y+d out) vs. V_{DD}.

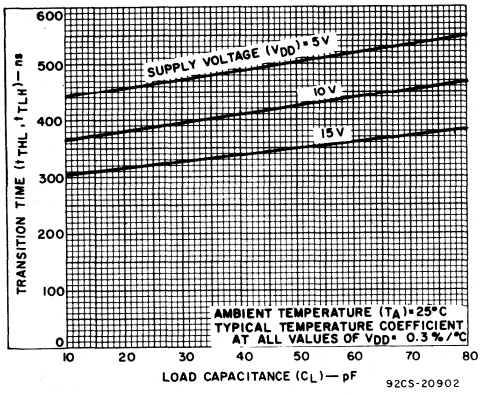


Fig. 9— Typical transition time vs. C_L.

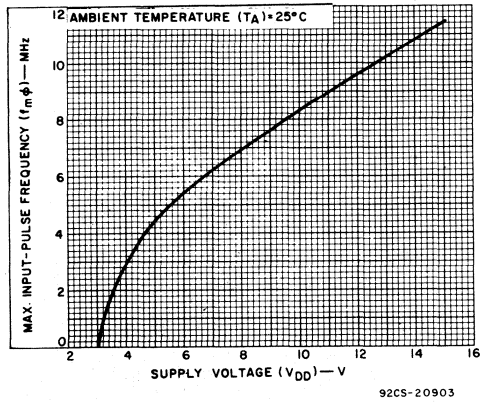


Fig. 10— Minimum $f_{m\phi}$ vs. V_{DD}

TEST CIRCUITS

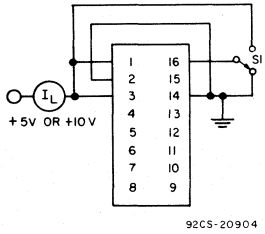


Fig. 11— Quiescent current.

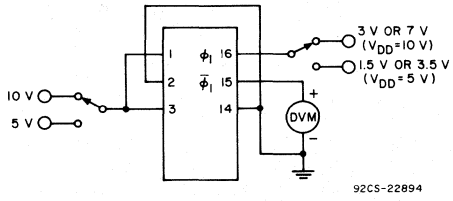


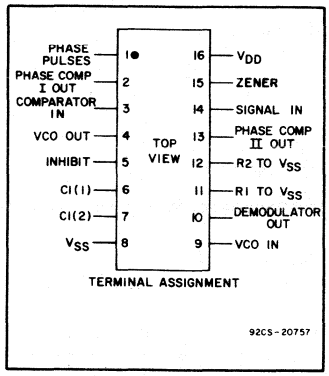
Fig. 12— Noise immunity.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

CD4046A/...



High-Reliability COS/MOS Micropower Phase-Locked Loop

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- Very low power consumption ..... 70 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V
- Operating frequency range ..... up to 1.2 MHz (typ.) at V_{DD} = 10 V
- Wide supply-voltage range ..... $V_{DD} - V_{SS}$ = 5 to 15 V
- Low frequency drift ..... 0.06%/°C (typ.) at V_{DD} = 10 V
- Choice of two phase comparators ..... 1. Exclusive-OR network
  2. Edge-controlled memory network with phase-pulse output for lock indication
- High VCO linearity ..... 1% (typ.)
- VCO inhibit control for ON-OFF keying and ultra-low standby power consumption
- Zener diode to assist supply regulation
- Source-follower output of VCO control input (Demod. output)

Applications:

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discriminator
- Data synchronization
- Voltage-to-frequency conversion
- Tone decoding
- FSK – Modems
- Signal conditioning
- (See companion application note ICAN-6101 for application information and circuit details)

RCA-CD4046A "Slash" (/) Series are high-reliability COS/MOS integrated circuit Phase-Locked Loops intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment.

These devices are electrically and mechanically identical with standard COS/MOS CD4046A types described in data bulletin 637 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4046A "Slash" (1) Series can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels — /N, /R, and standard chip. For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with High-Reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types",

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the following page.

The CD4046A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

The RCA-CD4046A COS/MOS Micropower Phase-Locked Loop (PPL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a

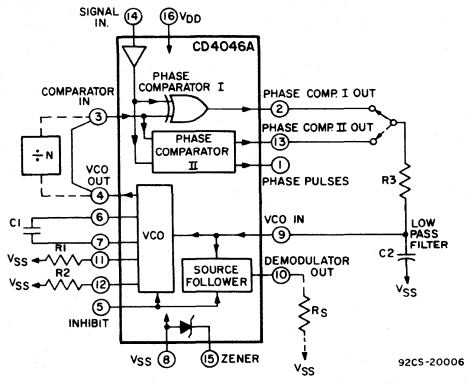


Fig. 1 – COS/MOS phase-locked loop block diagram.

common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary. The CD4046A is supplied in a 16-lead dual-in-line ceramic package (CD4046AD), It is also available in chip form (CD4046AH).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD4024A,CD4018A,CD4020A,CD4022A, or CD4029A. One or more CD4018A (Presettable Divide-by-N Counter) or CD4029A (Presettable Up/Down Counter), together with the CD4046A (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ⩽ 30% ($V_{DD}-V_{SS}$), logic "1" ⩾ 70% ($V_{DD}-V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_c$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ⩽ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

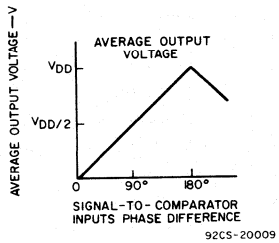


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON continuously. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs

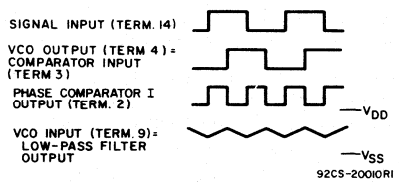


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

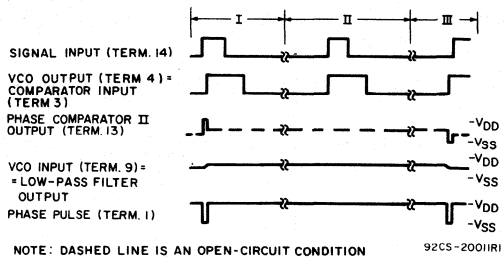


Fig.4 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4046AD CD4046AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4046AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4046AD/1N

CD4046A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4046AH/N

CD4046A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range . . . . −65°C to +150 °C

Operating Temperature Range:
Ceramic Package Types . . . . . −55°C to +125 °C

DC Supply Voltage Range
($V_{DD} - V_{SS}$) . . . . . −0.5 V to +15 V

Device Dissipation (Per Pkg.) . . . . 200 mW

All Inputs . . . . . $V_{SS} \leq V_I \leq V_{DD}$

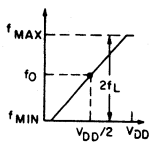
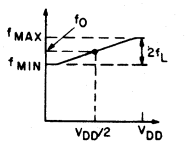
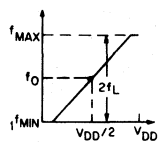
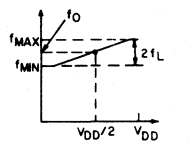
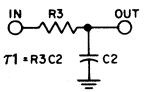
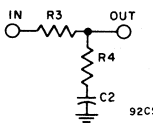
Lead Temperature (During soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . 265 °C

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$10\ k\Omega \leq R1, R2, R_S \leq 1\ M\Omega$
$C1 \geq 100\ pF$ at $V_{DD} \geq 5\ V$;
$C1 \geq 50\ pF$ at $V_{DD} \geq 10\ V$

In addition to the given design information refer to Fig. 5 for R1, R2, and C1 component selections.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency	 VCO INPUT VOLTAGE	 VCO INPUT VOLTAGE	 VCO INPUT VOLTAGE	 VCO INPUT VOLTAGE 92CS-20012RI
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	 (1),(2) $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$		$f_C = f_L$	
Loop Filter Component Selection	 For $2f_C$, see Ref. (2)			
Phase Angle between Signal and Comparator	90^o at center frequency (f_o), approximating 0^o and 180^o at ends of lock range ($2f_L$)		Always 0^o in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	– Given: f_o – Use f_o with Fig.5a to determine R1 and C1	– Given: f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Fig. 5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1	– Given: f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ – Use f_o with Fig.5a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1

For further information, see
(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O VOLTS	V_{DD} VOLTS	LIMITS CD4046AD, CD4046AK MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
VCO Section									
Operating Supply Voltage	$V_{DD}-V_{SS}$	As fixed oscillator only			3	–	15	V	–
		Phase-lock-loop operation			5	–	15		
Operating Power Dissipation	P_D	f_o = 10 kHz, R_1 = 1 MΩ, R2 = ∞, $VCO_{IN} = \frac{V_{DD}}{2}$		5	–	70	–	µW	6a
				10	–	600	–		
				15	–	2400	–		
Maximum Operating Frequency	f_{MAX}	R1 = 10 kΩ, R2 = ∞, $VCO_{IN} = V_{DD}$, C1 = 100 pF		5	0.25	0.5	–	MHz	–
				10	0.6	1.2	–		
		C1 = 50 pF		15	–	1.5	–		
Center Frequency and Frequency Range	f_o and $f_{MAX}-f_{MIN}$	Programmable with external components R1, R2, and C1							See Design Info.
Linearity	–	VCO_{IN} = 2.5 V ±0.3 V, R1 >10 kΩ		5	–	1	–	%	–
		= 5 V ± 2.5 V, R1 >400 kΩ		10	–	1	–		7a,b
		= 7.5 V ±5 V, R1 = 1 MΩ		15	–	1	–		
Temperature-Frequency Stability: No Frequency Offset, f_{MIN} = 0	–	R2 = ∞, %/°C ∝ $\frac{1}{f \cdot V_{DD}}$		5	–	0.12–0.24	–	%/°C	–
				10	–	0.04–0.08	–		
				15	–	0.015–0.03	–		
Frequency Offset, $f_{MIN} \neq 0$	–	%/°C ∝ $\frac{1}{f \cdot V_{DD}}$		5	–	0.06–0.12	–		–
				10	–	0.05–0.1	–		
				15	–	0.03–0.06	–		
Input Resistance of VCO_{IN} (Term 9)	R_I			5,10,15	–	10^{12}	–	Ω	–
VCO Output Voltage (Term 4) Low Level	V_{OL}	Driving COS/MOS-Type Load (e.g. Term 3 Phase Comparator Input)		5,10,15	–	–	0.01	V	–
High Level	V_{OH}			5	4.99	–	–		–
				10	9.99	–	–		
				15	14.99	–	–		
VCO Output Duty Cycle				5,10,15	–	50	–	%	–
VCO Output Transition Times	t_{THL}, t_{TLH}		V_O VOLTS	5	–	75	150	ns	–
				10	–	50	100		
				15	–	40	–		
VCO Output Drive Current: n-Channel (Sink)	I_{DN}		0.5	5	0.43	0.86	–	mA	–
			0.5	10	1.3	2.6	–		
p-Channel (Source)	I_{DP}		4.5	5	–0.3	–0.6	–		–
			9.5	10	–0.9	–1.8	–		
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	–	R_S >10 kΩ		5,10	–	1.5	2.2	V	–
				15	–	1.5	–		
Linearity	–	R_S >50 kΩ, VCO_{IN} = 2.5 ±0.3 V		5	–	0.1	–	%	–
		= 5 ± 2.5 V		10		0.6			
		= 7.5 ± 5 V		15	–	0.8	–		
Zener Diode Voltage CD4046AD, CD4046AK	V_Z	I_Z = 50 µA			4.7	5.2	5.7	V	–
Zener Dynamic Resistance	R_Z	I_Z = 1 mA			–	100	–	Ω	–

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O VOLTS	V_{DD} VOLTS	LIMITS CD4046AD, CD4046AK MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
PHASE COMPARATOR Section									
Operating Supply Voltage	$V_{DD}-V_{SS}$	Amplifier Operation		–	5	–	15	V	–
		Comparators only		–	3	–	15		–
Total Quiescent Device Current:	I_L								
Term. 14 Open		Term. 15 open, Term. 5 at V_{DD}, Terms. 3 & 9 at V_{SS}		5	–	25	55	μA	–
				10	–	200	410		
Term. 14 at V_{SS} or V_{DD}				5	–	5	15		
				10	–	25	60		
Term. 14 (SIGNAL IN) Input Impedance	Z_{14}			5	1	2	–	MΩ	–
				10	0.2	0.4	–		
				15	–	0.2	–		
AC-Coupled Signal Input Voltage Sensitivity				5	–	200	400	mV	8
				10	–	400	800		
				15	–	700	–		
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity:									
Low Level				5	1.5	2.25	–	V	–
				10	3	4.5	–		
				15	4.5	6.75	–		
High Level				5	–	2.75	3.5		–
			V_O VOLTS	10	–	5.5	7		
				15	–	8.25	–		
Output Drive Current:									
n-Channel (Sink)	I_DN	Phase Comparator I & II Term. 2 & 13	0.5	5	0.43	0.86	–	mA	–
			0.5	10	1.3	2.5	–		–
		Phase Pulses	0.5	5	0.23	0.47	–		–
			0.5	10	0.7	1.4	–		–
p-Channel (Source)	I_DP	Phase Comparator I & II Term. 2 & 13	4.5	5	−0.3	−0.6	–		–
			9.5	10	−0.9	−1.8	–		–
		Phase Pulses	4.5	5	−0.08	−0.16	–		–
			9.5	10	−0.25	−0.5	–		–

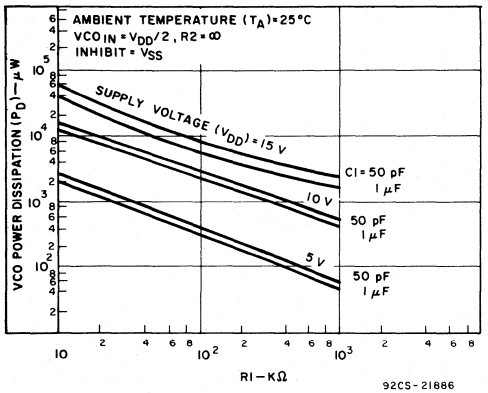


Fig.5 (a) – Typical VCO power dissipation at center frequency vs R1.

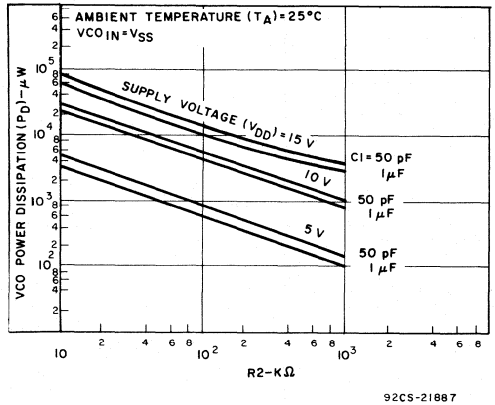


Fig.5 (b) – Typical VCO power dissipation at f_{min} vs R2.

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S) – Phase Comparator I

P_D (Total) = P_D (f_{MIN}) – Phase Comparator II

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_O Volts	V_{DD} Volts	LIMITS AT INDICATED TEMPERATURES CD4046AD, CD4046AK −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	NOTES
Static												
Total Quiescent Device Current (Term 16 at V_{DD})	I_L			10	–	10•	–	10•	–	200•	μA	1
Quiescent Device Dissipation Per Package (Term 16 at V_{DD})	P_D			10	–	100	–	100	–	2000	μW	–
VCO Oscillator Current	I_{VCO}	Adjust R_2 on −10 μA		10	–	–	−20•	−30•	–	–	μA	2
		Term 12 For: −100 μA		10	–	–	−200•	−260•	–	–	μA	2
Output Voltage: Low Level	V_{OL}			4.5	–	0.55•	–	0.5•	–	–	V	1
				15	–	–	–	0.5•	–	0.25•		
High-Level	V_{OH}			4.5	3.95•	–	4.0•	–	–	–	V	1
				15	–	–	14.5•	–	14.7•	–		
Threshold Voltage: n-Channel	$V_{TH}N$	I_D = −10 μA		10	−7.5•	–	−7.8•	–	−7.8•		V	2
p-Channel	$V_{TH}P$	I_D = 10 μA		10	7.5•	–	7.8•	–	7.8•			
Output Drive Current: n-Channel:	I_{DN}		0.5	10							mA	2
VCO Out (Term 4)					–	–	1.3•	–	–	–		
VCO C1 (Term 6)					–	–	1.9•	–	–	–		
VCO C1 (Term 7)					–	–	1.9•	–	–	–		
VCO R_2 to V_{SS} Term 12					–	–	5.0•	–	–	–		
Phase Comp. I Out (Term 2)					–	–	1.3•	–	–	–		
Phase Comp.II Out (Term 13)					1.6•	–	1.3•	–	1.1•	–		
Phase Comp.II Phase Pulses (Term 1)					–	–	0.7•	–	–	–		
p-Channel:	I_DP		9.5	10							mA	2
VCO Out (Term 4)					–	–	−0.9•	–	–	–		
Phase Comp. I Out (Term 2)					–	–	−0.9•	–	–	–		
Phase Comp.II Out (Term 13)					−1.1•	–	−0.9•	–	0.7•	–		
Phase Comp.II Phase Pulses (Term 1)					–	–	−0.65•	–	–	–		
Zener Diode Voltage	V_Z	V_{SS} = Ground, 50 μA into Term 15	–	–	–	–	4.7•	5.7•	–	–	V	2
Diode Test	V_F	100 μA at each input or output	–	–	–	1.5•	–	1.5•	–	1.5•	V	
Dynamic												
Phase Comp. No. 1 Output Voltage		Input Signal Voltage (Term 14) = 400 mV f = 10 kHz, See Fig. 7	–	5	–	–	2.4•	2.6•	–	–	V	2
Phase Comp. No. 1 Output Voltage		Input Signal Voltage (Term 14) = 800 mV f = 10 kHz, See Fig. 7	–	10	–	–	4.8•	5.2•	–	–	V	2

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.

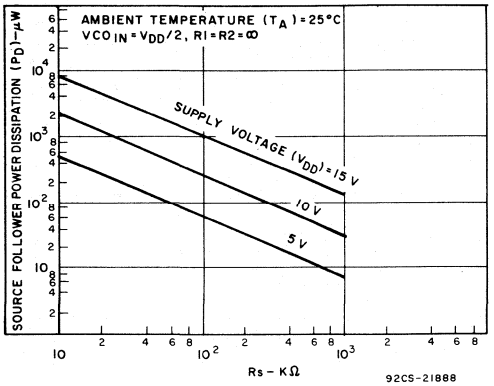


Fig. 5(c) Typical source follower power dissipation vs. R_S.

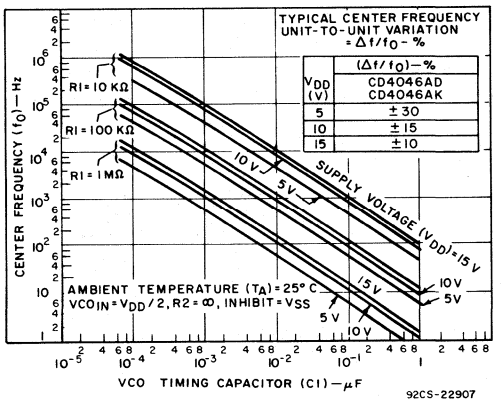


Fig. 6(a) — Typical center frequency vs. C1 for R1 = 10 kΩ, 100 kΩ, and 1 MΩ. Lower frequency values are obtainable if larger values of C1 are used.

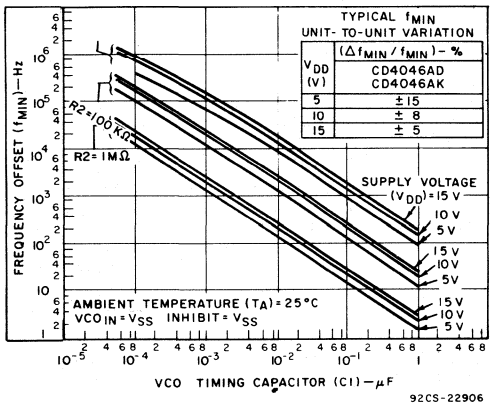


Fig. 6(b) — Typical frequency offset vs. C1 for R2 = 10 kΩ, 100 kΩ, and 1 MΩ. Lower frequency values are obtainable if larger values of C1 are used.

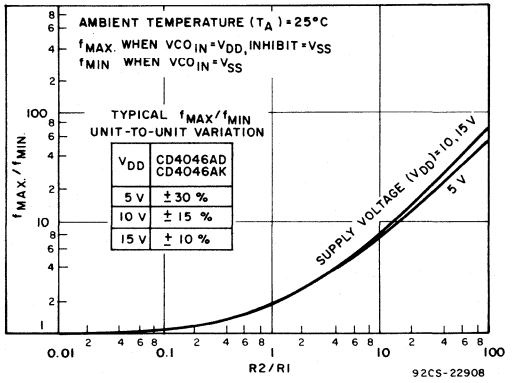


Fig. 6(c) — Typical $f_{max.}/f_{min.}$ vs. R2/R1.

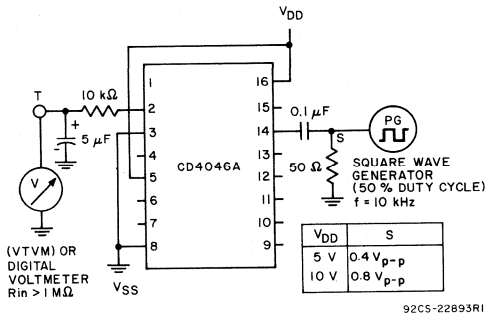


Fig. 7 — Test circuit for Phase Comparator I Output voltage.

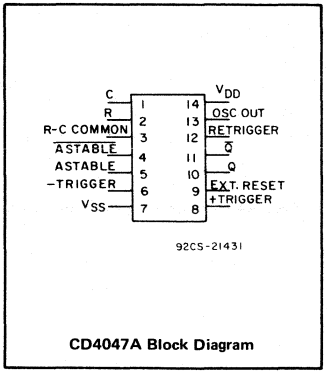
RCA
Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4047A/...



CD4047A Block Diagram

High-Reliability COS/MOS Low-Power Monostable/Astable Multivibrator

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features:

- **Low power consumption: special COS/MOS oscillator configuration**
- **Monostable (one-shot) or astable (free-running) operation**
- **True and complemented buffered outputs**
- **Only one external R and C required**

Monostable Multivibrator Features:

- **Positive- or negative-edge trigger**
- **Output pulse width independent of trigger pulse duration**
- **Retriggerable option for pulse width expansion**
- **Long pulse widths possible using small RC components by means of external counter provision**
- **Fast recovery time essentially independent of pulse width**
- **Pulse-width accuracy maintained at duty cycles approaching 100%**

Astable Multivibrator Features:

- **Free-running or gatable operating modes**
- **50% duty cycle**
- **Oscillator output available**
- **Good astable frequency stability:**
  frequency deviation = ±2% + 0.03%/°C @ 100 kHz*
  = ±0.5% + 0.015%/°C @ 10 kHz*

COS/MOS Features:

- **Microwatt quiescent power dissipation: 0.5 μW (typ.)**
- **High noise immunity: 45% of supply voltage (typ.)**
- **Wide operating-temperature range: −55°C to +125°C**

Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- **Frequency discriminators**
- **Envelope detection**
- **Timing circuits**
- **Frequency multiplication**
- **Time-delay applications**
- **Frequency division**

RCA CD4047A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment.

RCA CD4047A consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action having retriggering and external counting options.

Inputs include +Trigger, −Trigger, Astable, $\overline{\text{Astable}}$, Retrigger, and External Reset. Buffered outputs are Q, $\overline{Q}$, and Oscillator. In all modes of operation an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the Astable input. The period of the square wave at the Q and $\overline{Q}$ outputs in this mode of operation is a function of the external components employed. "True" input pulses on the Astable input or "Complement" pulses on the $\overline{\text{Astable}}$ input allow the circuit

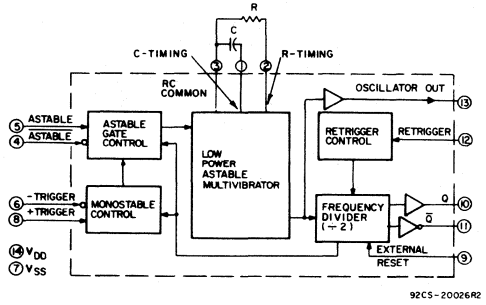


Fig.1 – CD4047A logic block diagram.

* Circuits "trimmed" to frequency; V_{DD} = 10 V ± 10%.

to be used as a gatable multivibrator. An output whose period is half of that which appears at the Q terminal is available at the Oscillator Output terminal. However, a 50% duty cycle is not guaranteed at this output.

In the monostable mode positive-edge triggering is accomplished by application of a leading-edge pulse to the "+Trigger" input and a low level to the "–Trigger" input. For negative-edge triggering a trailing-edge pulse is applied to the "–Trigger" and a high level is applied to the "+Trigger". Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the "Retrigger" and "+Trigger" inputs. In this mode the output pulse remains "high" as long as the input pulse period is shorter than the period determined by the RC components.

An external countdown option can be implemented by coupling "Q" to an external "N" counter (e.g. CD4017A) and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{Astable}}$ input and has a duration equal to N times the period of the multivibrator.

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 14-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 14-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4047AD, CD4047AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4047AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range ..... –65 to +150 °C
Operating-Temperature Range ..... –55 to +125 °C
DC Supply-Voltage Range:
($V_{DD} - V_{SS}$) ..... –0.5 to +15 V
Device Dissipation (Per Package) ..... 200 mW
All Inputs† ..... $V_{SS} \leq V_I \leq V_{DD}$
Recommended
DC Supply-Voltage ($V_{DD} - V_{SS}$) ..... 3 to 15 V
Recommended
Input-Voltage Swing ..... V_{DD} to V_{SS}

† Special input protection circuit permits terminal 3 voltage to exceed V_{DD} or V_{SS} by as much as 15 volts.

A high level on the External Reset input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time.

These devices are electrically and mechanically identical with standard COS/MOS CD4047A types described in data bulletin 623 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4047A "Slash" (/) Series can be supplied to six screening levels–/1N, /1R, /1, /2, /3, /4–which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels–/N, /R, and standard chip. *For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliabillty COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".*

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part numbers, see the chart below.

The CD4047A "Slash" (/) Series types are supplied in 14-lead dual-in-line ceramic packages ("D" suffix), in 14-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A | D | /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4000AH/N

CD4000A | H | /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

CD4047A FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	$t_A(10,11)=4.40\ RC$
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	$t_A(13)=2.20\ RC$
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator:					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	$t_M(10,11)=2.48\ RC$
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown*	14	5, 6, 7, 8, 9, 12	–	10, 11	

* Input Pulse to Reset of External Counting Chip
External Counting Chip Output To Terminal 4
▲ See Text.

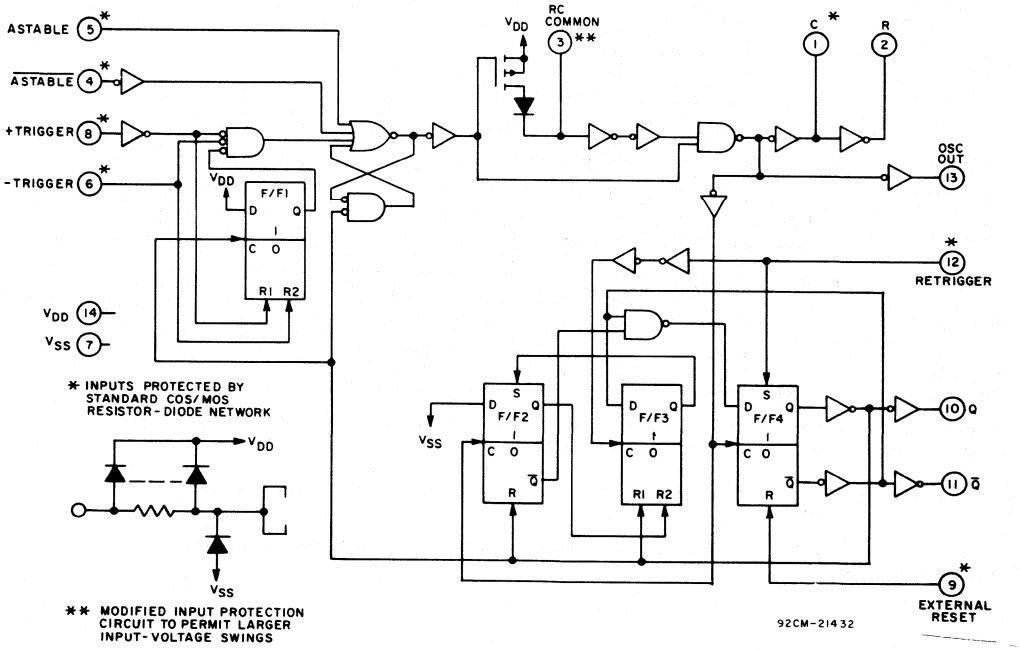


Fig.2 – CD4047A logic diagram.

STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage 3 to 15 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CD4047AD,CD4047AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
				−55°C			25°C			125°C					
		V_O Volts	V_{DD} Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I_L		5	–	–	5	–	0.5	5	–	–	300	μA	33	1
			10	–	–	10•	–	1	10•	–	–	200•			
Quiescent Device Dissipation/Package	P_D		5	–	–	25	–	2.5	25	–	–	1500	μW	–	–
			10	–	–	100	–	10	100	–	–	2000			
Output Voltage: Low-Level	V_{OL}		3	–	–	0.55•	–	–	0.5•	–	–	–	V	–	1
			5	–	–	0.01	–	0	0.01	–	–	0.05			
			10	–	–	0.01	–	0	0.01	–	–	0.05			
			15	–	–	–	–	–	0.5•	–	–	0.55•			
High-Level	V_{OH}		3	2.25•	–	–	2.3•	–	–	–	–	–	V	–	1
			5	4.99	–	–	4.99	5	–	4.95	–	–			
			10	9.99	–	–	9.99	10	–	9.95	–	–			
			15	–	–	–	14.5•	–	–	14.45•	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D = -10$ μA		−0.7•	−1.7	−3•	−0.7•	−1.5	−3•	−0.3•	−1.3	−3•	V	–	2
P-Channel	V_{THP}	$I_D = 10$ μA		0.7•	1.7	3•	0.7•	1.5	3•	0.3•	1.3	3•			
Noise Immunity (Any input) *For Definition, see Appendix in SSD-207*	V_{NL}	0.8	5	1.5	–	–	1.5•	2.25	–	1.4	–	–	V	34	1
		1.0	10	3•	–	–	3•	4.5	–	2.9•	–	–			
	V_{NH}	4.2	5	1.4	–	–	1.5•	2.25	–	1.5	–	–	V		
		9.0	10	2.9•	–	–	3•	4.5	–	3•	–	–			
Output Drive Current: (Q and $\overline{Q}$) N-Channel	I_DN	0.5	5	0.5	–	–	0.4•	0.8	–	0.28	–	–	mA	3,4	2
		0.5	10	1.25	–	–	1•	2	–	0.7	–	–			
P-Channel	I_DP	4.5	5	−0.5	–	–	−0.4•	−0.8	–	−0.28	–	–	mA	5,6	
		9.5	10	−1.25	–	–	−1•	−2	–	−0.7	–	–			
(OSCILLATOR) N-Channel	I_DN	0.5	5	–	–	–	0.8	–	–	–	–	–	–	–	–
		0.5	10	–	–	–	2	–	–	–	–	–			
P-Channel	I_DP	4.5	5	–	–	–	−0.8	–	–	–	–	–	–	–	
		9.5	10	–	–	–	−2	–	–	–	–	–			
Diode Test 100 μA Test Pin	V_{DF}			–	–	1.5•	–	–	1.5•	–	–	1.5•	V	–	3
Input Current	I_I			–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table. Note 3: Test on all inputs and outputs.
Note 2: Test is either a one input or one output only.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
				CD4047AK CD4047AD					
			V_{DD} (Volts)	Min.	Typ.	Max.			
Propagation Delay Time: Astable, Astable to Osc. Out	t_{PHL}, t_{PLH}		5	–	200	400	ns	–	–
			10	–	100	200			
Astable, Astable to Q, $\overline{Q}$			5	–	550	900		–	1
			10	–	250	500●			
+Trigger, –Trigger to Q, $\overline{Q}$			5	–	700	1200		7	1
			10	–	300	600●			
+Trigger, Retrigger to Q, $\overline{Q}$			5	–	300	600		–	–
			10	–	175	300			
External Reset to Q, $\overline{Q}$			5	–	300	600		–	–
			10	–	125	250			
Transition Time: Q, $\overline{Q}$	t_{THL}, t_{TLH}		5	–	75	125	ns	8	–
			10	–	45	75			
Osc. Out			5	–	75	150		–	–
			10	–	45	100			
Minimum Input Pulse Duration (Any input)	t_{WL}, t_{WH}		5	–	500	1000	ns	–	–
			10	–	200	400			
+Trigger, Retrigger Rise & Fall Time	t_r, t_f		5	–	–	15	μs	–	–
			10	–	–	5			
Average Input Capacitance	C_I	Any input	–	–	5	–	pF	–	–

Note 1: Test is a one input, one output only.

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

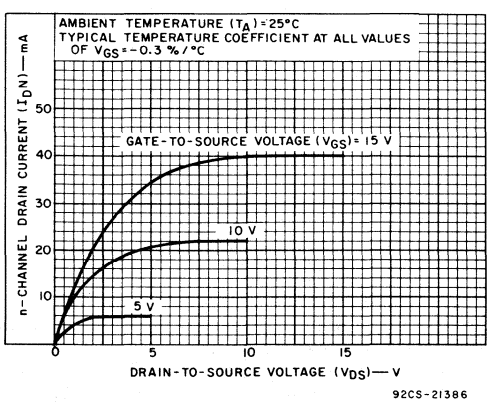


Fig.3 – Typical n-channel drain characteristics for Q and $\overline{Q}$ buffers.

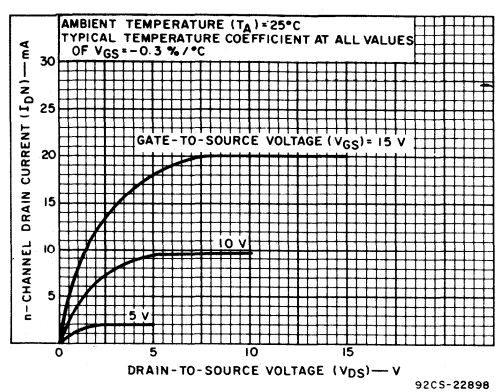


Fig.4 – Minimum n-channel drain characteristics for Q and $\overline{Q}$ buffers.

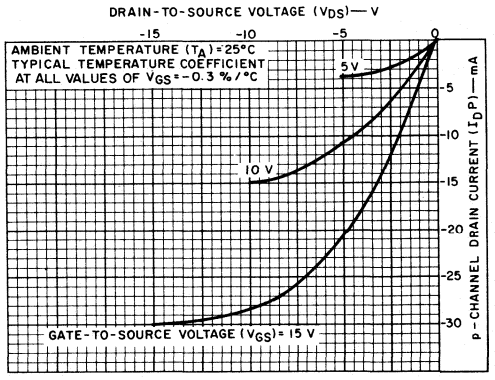


Fig.5 – Typical p-channel drain characteristics for Q and $\overline{Q}$ buffers.

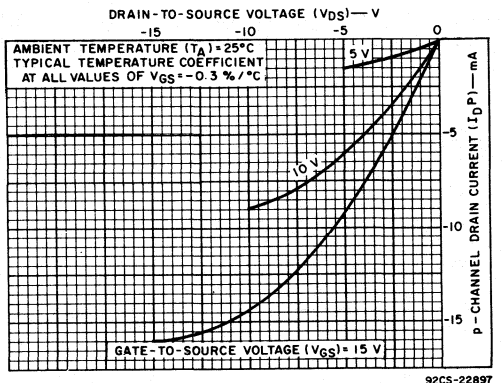


Fig.6 – Minimum p-channel drain characteristics for Q and $\overline{Q}$ buffers.

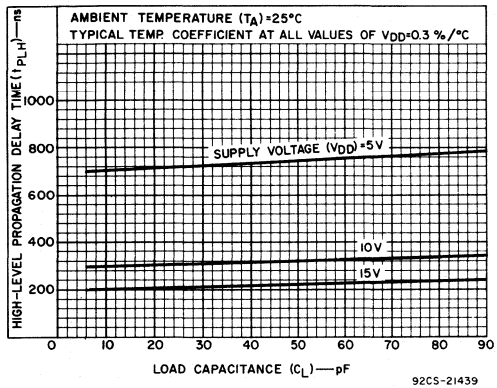


Fig.7 – Typical low-to-high level propagation delay time vs. load capacitance for Q and $\overline{Q}$ buffers.

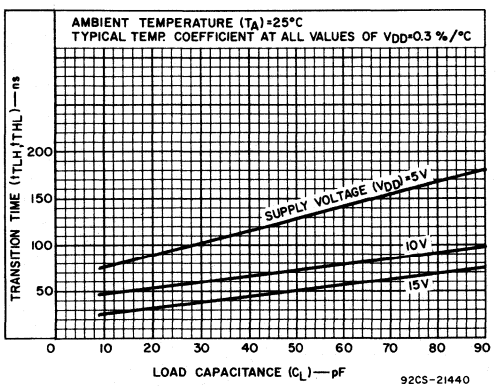


Fig.8 – Typical transition time vs. load capacitance for Q and $\overline{Q}$ buffers.

I. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33%–67% V_{DD}) for free-running (astable) operation.

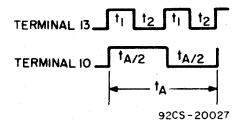


Fig.9 – Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2)$$

$$= -2\,RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ:	$V_{TR} = 0.5\,V_{DD}$	$t_A = 4.40\,RC$
Min:	$V_{TR} = 0.33\,V_{DD}$	$t_A = 4.62\,RC$
Max:	$V_{TR} = 0.67\,V_{DD}$	$t_A = 4.62\,RC$

thus if $\boxed{t_A = 4.40\,RC}$ is used, the maximum variation will be (+5.0%, –0.0%).

B. Variations Due to V_{DD} and Temperature Changes

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 10 to 20 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

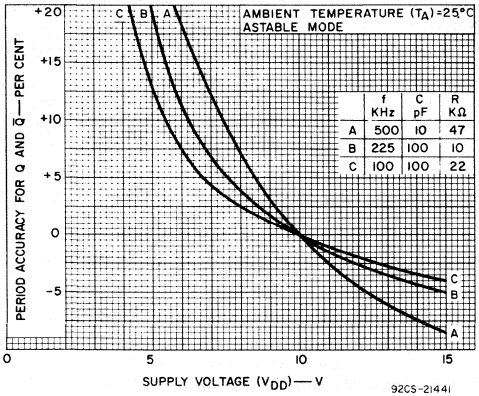


Fig.10 – Typical Q-and-$\bar{Q}$-period accuracy vs. supply voltage (high frequency).

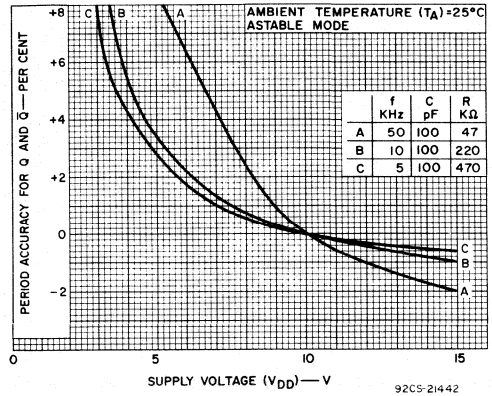


Fig.11 – Typical Q-and-$\bar{Q}$-period accuracy vs. supply voltage (medium frequency).

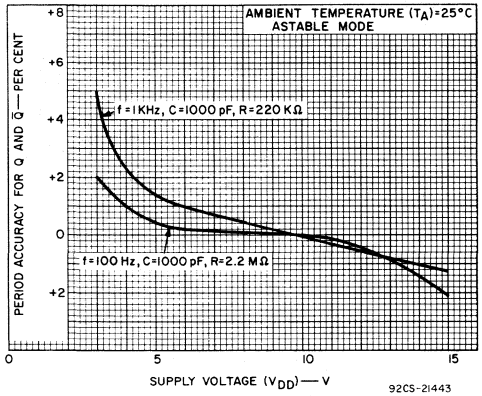


Fig.12 – Typical Q-and-$\bar{Q}$-period accuracy vs. supply voltage (low frequency).

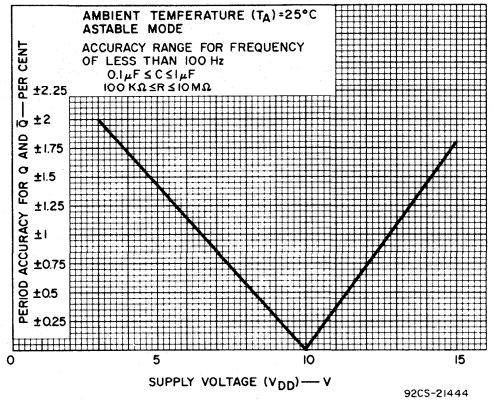


Fig.13 – Typical $\bar{Q}$-and-Q-period accuracy vs. supply voltage (very low frequency).

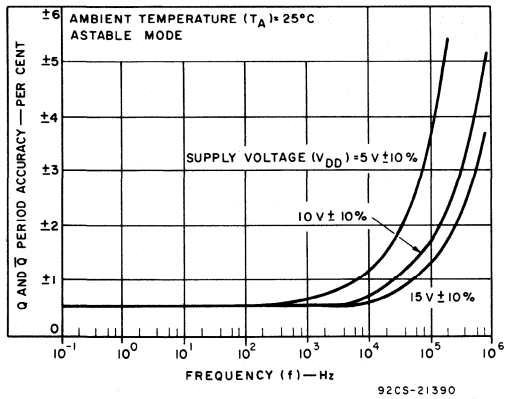


Fig.14 – Typical Q-and-$\bar{Q}$-period accuracy vs. frequency for V_{DD} variation of ± 10% from value indicated.

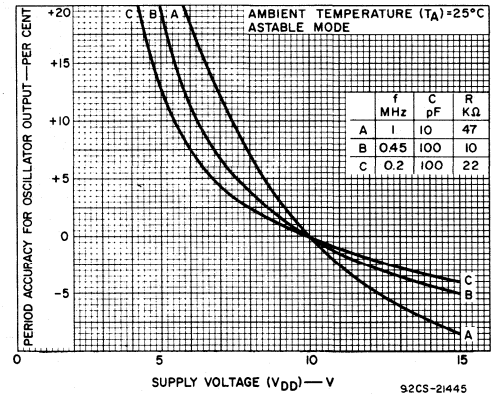
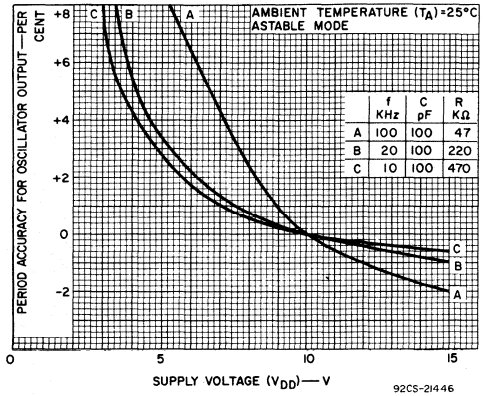
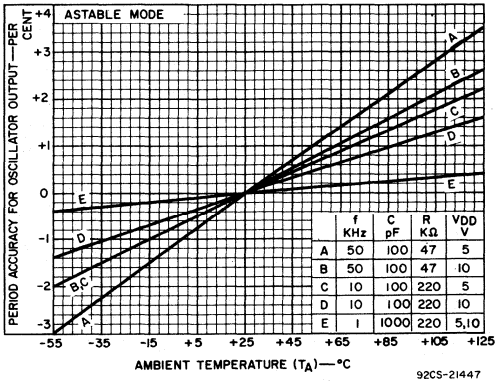


Fig.15 – Typical oscillator-output-period accuracy vs. supply voltage (high frequency).



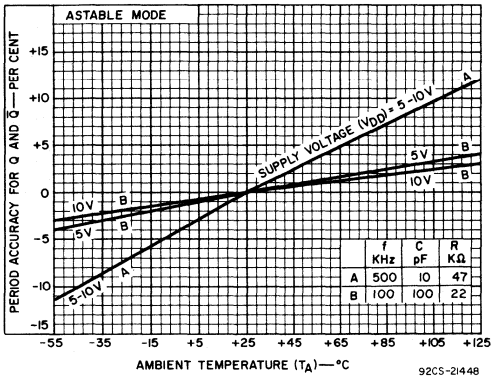
	f KHz	C pF	R KΩ
A	100	100	47
B	20	100	220
C	10	100	470

Fig.16 – Typical oscillator-output-period accuracy vs. supply voltage (medium frequency).



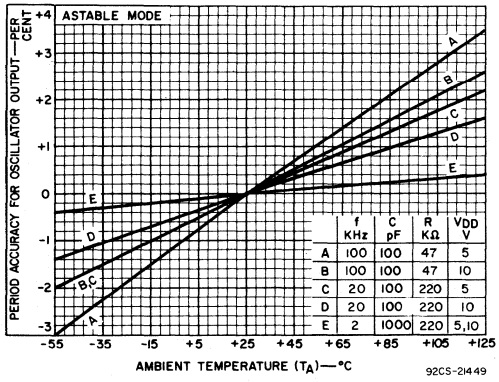
	f KHz	C pF	R KΩ	VDD V
A	50	100	47	5
B	50	100	47	10
C	10	100	220	5
D	10	100	220	10
E	1	1000	220	5,10

Fig.17 – Typical Q-and-$\overline{Q}$-period accuracy vs. temperature (medium frequency).



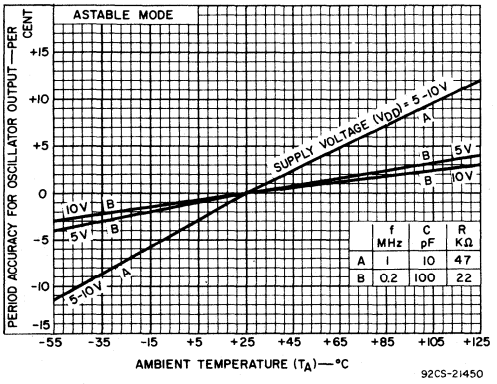
	f KHz	C pF	R KΩ
A	500	10	47
B	100	100	22

Fig.18 – Typical Q-and-$\overline{Q}$-period accuracy vs. temperature (high frequency).



	f KHz	C pF	R KΩ	VDD V
A	100	100	47	5
B	100	100	47	10
C	20	100	220	5
D	20	100	220	10
E	2	1000	220	5,10

Fig.19 – Typical oscillator-period accuracy vs. temperature (medium frequency).



	f MHz	C pF	R KΩ
A	1	10	47
B	0.2	100	22

Fig.20 – Typical oscillator-period accuracy vs. temperature (high frequency).

II. Monostable Mode Design Information

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% – 67% V_{DD}) for one-shot (monostable) operation.

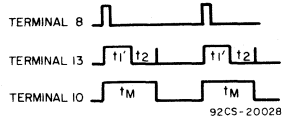


Fig.21 – Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$

Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$

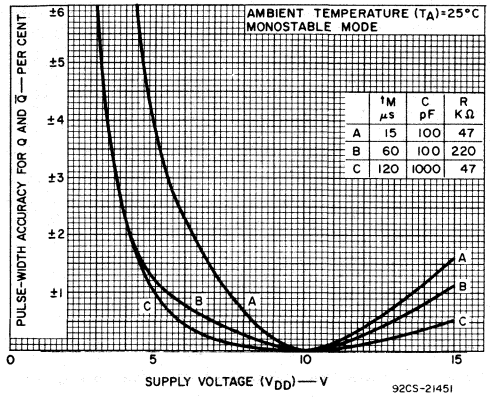
Max. $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

Thus if $t_M = 2.48\ RC$ is used, the maximum variation will be (+9.3%, −0.0%).

Note:

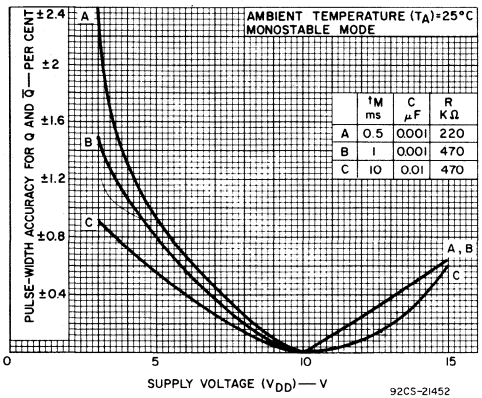
In the astable mode, the first positive half cycle has a duration of T_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature. These variations are presented in graphical form in Figs.22 to 27 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.



	t_M μs	C pF	R KΩ
A	15	100	47
B	60	100	220
C	120	1000	47

Fig.22 – Typical Q-and-$\overline{Q}$-pulse-width accuracy vs. supply voltage (t_M = 15, 60, 120 μs).



	t_M ms	C μF	R KΩ
A	0.5	0.001	220
B	1	0.001	470
C	10	0.01	470

Fig.23 – Typical Q-and-$\overline{Q}$-pulse-width accuracy vs. supply voltage (t_M = 0.5, 1, 10 ms).

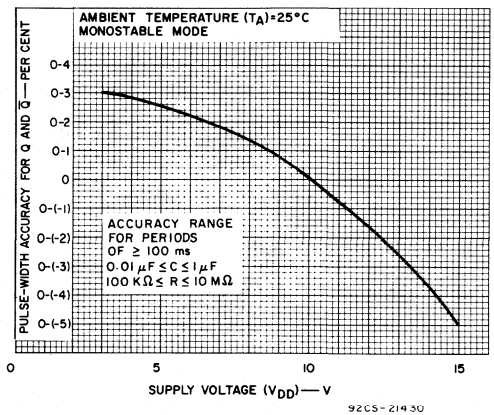


Fig.24 – Typical Q-and-$\overline{Q}$-pulse-width accuracy vs. supply voltage ($t_M \geq 100$ ms).

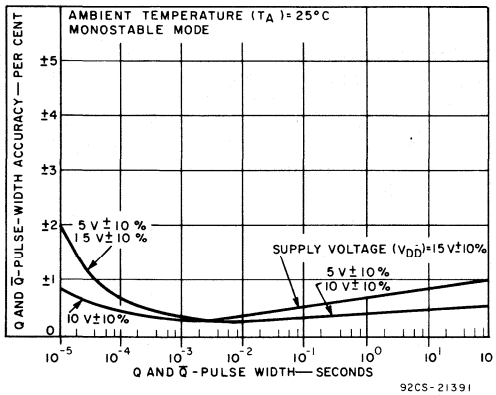
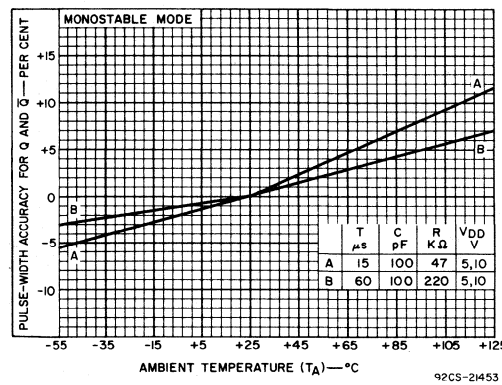


Fig.25 – Typical Q-and-$\overline{Q}$-pulse-width accuracy vs. Q and $\overline{Q}$ pulse width for a variation of ± 10% from value indicated.



	T μs	C pF	R KΩ	V_{DD} V
A	15	100	47	5,10
B	60	100	220	5,10

Fig.26 – Typical Q-and-$\overline{Q}$-pulse-width accuracy vs. temperature (high frequency).

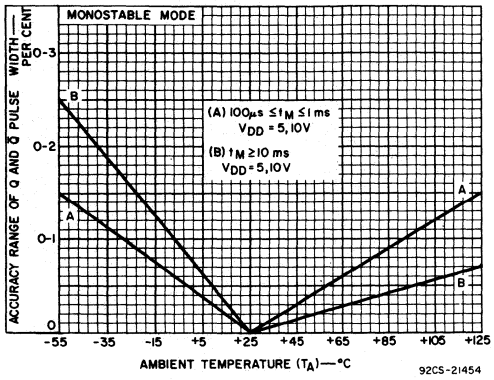


Fig.27 – Typical Q-and-$\overline{Q}$-pulse-width accuracy range vs. temperature.

III. Retrigger Mode Operation

The CD4047A can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig.28, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT) terminates at some variable time t_D

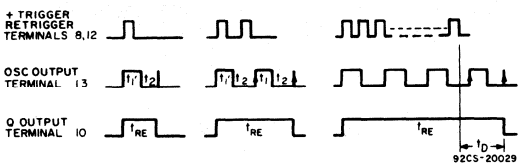


Fig.28 – Retrigger-mode waveforms.

after the termination of the last retrigger pulse. t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig.2).

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig.29. The pulse duration at the output is

$$t_{ext} = (N - 1)\,(t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

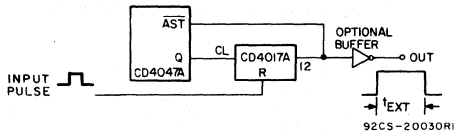


Fig.29 – Implementation of external counter option.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i. e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geq 100$ pF, up to any practical value, for astable modes;

$C \geq 1000$ pF, up to any practical value for monostable modes.

$10\ K\Omega \leq R \leq 1\ M\Omega$.

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode: $P = 2CV^2f$. (Output at terminal No. 13)

$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

Monostable Mode: $P = \dfrac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 30–32 for typical power consumption in astable mode.

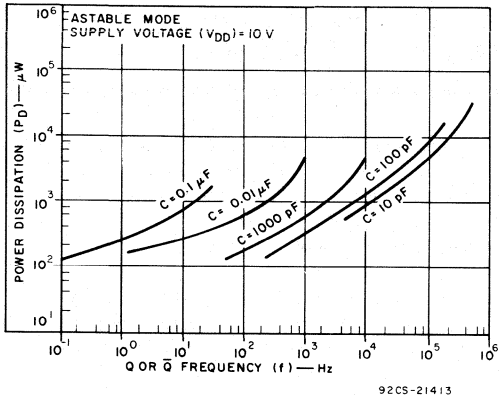


Fig.31 – Power dissipation vs. output frequency (V_{DD} = 10 V).

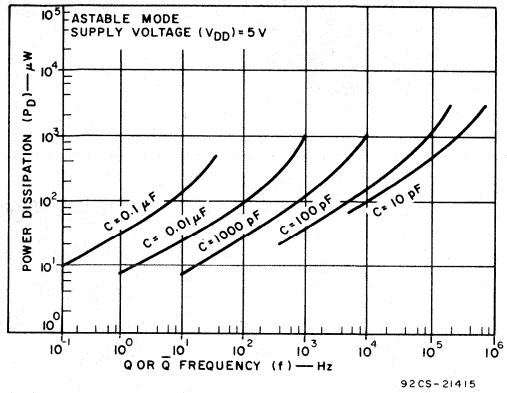


Fig.30 – Power dissipation vs. output frequency (V_{DD} = 5 V).

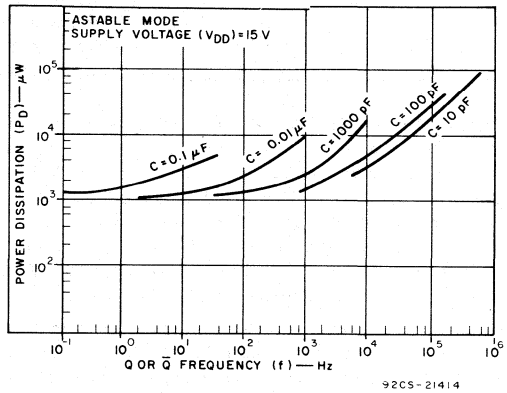
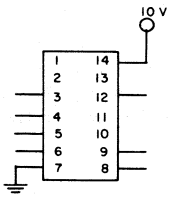


Fig.32 – Power dissipation vs. output frequency (V_{DD} = 15 V).



TEST	TERMINAL Nos.						
	3	4	5	6	8	9	12
1	1	1	1	1	1	0	1
2	1	1	1	0	1	1	0
3	0	0	1	1	0	1	0
4	NC	1	0	0	0	0	0

92CS-21321

Fig.33 – Quiescent device current.

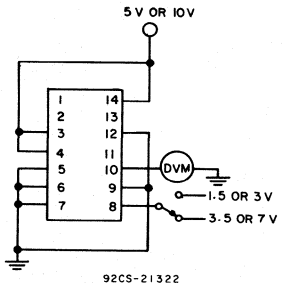


Fig.34 – Noise immunity.

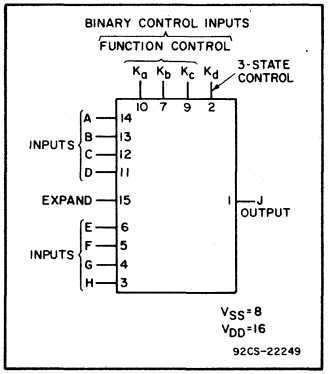
RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series

CD4048A/...



High-Reliability COS/MOS Multi-Function Expandable 8-Input Gate

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Special Features

- **Medium-power TTL drive capability**
- **Three-state output**
- **High-current source and sink capability 9 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V**
- **Many logic functions available in one package**

Applications:

- **Selection of up to 8 logic functions**
- **Digital control of logic**
- **General-purpose gating logic**
  - **—Decoding**
  - **—Encoding**

RCA CD4048A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment. The CD4048A is an 8-input gate having four control inputs. Three binary control inputs — Ka, Kb, and Kc — provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR.

A fourth control input — Kd — provides the user with 3-state outputs. When control input Kd is "high" the output is either a logic 1 or a logic 0 depending on the input states. When control input Kd is "low", the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048A, (see Fig. 2). For example, two CD4048A's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

These devices are electrically and mechanically identical with standard COS/MOS CD4048A types described in data bulletin 636 and DATABOOK SSD-203 Series, but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883.

The packaged types in the CD4048A "Slash" (/) Series can be supplied to six screening levels — /1N, /1R, /1, /2, /3, /4 — which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to

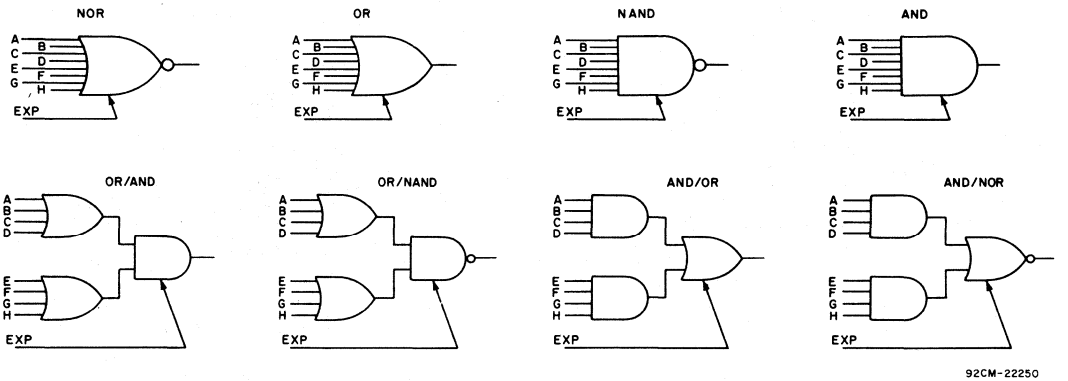


Fig. 1—Basic logic configurations.

three screening levels --- /N, /R, and standard chip. For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices, refer to High-Reliability Report RIC-102B, "High-Reliability COS/MOS CD4000A Slash (/) Series Types".

For a listing of the Screening Level Options available for both packaged devices and chips, and for a description of the COS/MOS high-reliability integrated circuit part number, see the tables below.

The CD4048A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

Table I – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4048AK, CD4048AD	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4048AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

Table II – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4048AD/1N

CD4048A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic K = Ceramic Flat-Pack	/1N /1R /1 /2 /3 /4

Chip Version, CD4048AH/N

CD4048A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N /R

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150 °C
Operating-Temperature Range	−55 to +125 °C
DC Supply-Voltage Range: ($V_{DD} - V_{SS}$)	−0.5 to +15 V
Device Dissipation (Per Package)	200 mW
All Inputs	$V_{SS} < V_I < V_{DD}$
Recommended	
DC Supply-Voltage ($V_{DD} - V_{SS}$)	3 to 15 V
Recommended Input-Voltage Swing	V_{DD} to V_{SS}
Lead Temperature (During Soldering) At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

STATIC ELECTRICAL CHARACTERISTICS *(All Inputs . . . $V_{SS} \leq V_I \leq V_{DD}$) Recommended DC Supply Voltage 3 to 15 V*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4048AD, CD4048AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
					−55°C			25°C			125°C					
		V_O Volts	V_{DD} Volts		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I_L		5		–	–	1	–	0.005	1	–	–	60	μA	6	1
			10		–	–	2●	–	0.01	2●	–	–	40●			
Quiescent Device Dissipation/Package	P_D		5		–	–	5	–	0.025	5	–	–	300	μW	–	–
			10		–	–	20	–	0.05	20	–	–	400			
Output Voltage Low-Level	V_{OL}		3		–	–	0.55●	–	–	0.5●	–	–	–	V	–	1
			5		–	–	0.01	–	0	0.01	–	–	0.05			
			10		–	–	0.01	–	0	0.01	–	–	0.05			
			15		–	–	–	–	–	0.5●	–	–	0.55●			
High-Level	V_{OH}		3		2.25●	–	–	2.3●	–	–	–	–	–	V	–	1
			5		4.99	–	–	4.99	5	–	4.95	–	–			
			10		9.99	–	–	9.99	10	–	9.95	–	–			
			15		–	–	–	14.5●	–	–	14.45●	–	–			
Threshold Voltage: N-Channel	V_{THN}	$I_D = -10\ \mu A$			−0.7●	−1.7	−3●	−0.7●	−1.5	−3●	−0.3●	−1.3	−3●	V	–	2
P-Channel	V_{THP}	$I_D = 10\ \mu A$			0.7●	1.7	3●	0.7●	1.5	3●	0.3●	1.3	3●			
Noise Immunity (Any Input)	V_{NL}		4.2	5	1.5	–	–	1.5●	2.25	–	1.4	–	–	V	–	1
			9	10	3●	–	–	3●	4.5	–	2.9●	–	–			
For Definition, See Appendix SSD-207	V_{NH}		0.8	5	1.4	–	–	1.5●	2.25	–	1.5	–	–	V		
			1	10	2.9●	–	–	3●	4.5	–	3●	–	–			
Output Drive Current: N-Channel	I_DN		0.4	4.5	2	–	–	1.6●	3.2	–	1.1	–	–	mA	4,7	2
			0.5	10	5.6	–	–	4.5●	9	–	3.1	–	–			
P-Channel	I_DP		4.6	5	−2	–	–	−1.6●	−3.2	–	−1.1	–	–	mA	8, 9	2
			9.5	10	−5.6	–	–	−4.5●	−9	–	−3.1	–	–			
High and Low Voltage Current Test	I_DN, I_DP		0	3	–	–	–	0.28●	–	–	–	–	–	μA	–	2
			0	15	–	–	–	1.7●	–	–	–	–	–			
Diode Test, 100 μA Test Pin	V_{DF}				–	–	1.5●	–	–	1.5●	–	–	1.5●	V	–	3
Input Current	I_I				–	–	–	–	10	–	–	–	–	pA	–	–

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or one output only.
Note 3: Test on all inputs and outputs.

For Threshold Voltage Test Circuits, Operating and Biased Life Test Circuits, Output Drive Current Test Circuits, and for Operating Considerations, see Appendix.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C and C_L = 15 pF and 50 pF*

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

C_L = 15 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (Volts)	LIMITS CD4048AD CD4048AK Min.	Typ.	Max.*	UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
Propagation Delay Time	t_{PLH}, t_{PHL}		5	–	750	1300	ns	10	1
			10	–	225	400●			
Transition Time: High-to-Low Level	t_{THL}		5	–	90	140	ns	12	1
			10	–	30	50●			
Low-to-High Level	t_{TLH}		5	–	130	250	ns	11	1
			10	–	40	60●			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–

C_L = 50 pF

Propagation Delay Time	t_{PLH}, t_{PHL}		5	–	775	1350	ns	10	–
			10	–	240	430			
Transition Time: High-to-Low Level	t_{THL}		5	–	105	170	ns	12	–
			10	–	40	70			
Low-to-High Level	t_{TLH}		5	–	145	280	ns	11	–
			10	–	50	80			
Input Capacitance	C_I	Any Input		–	5	–	pF	–	–

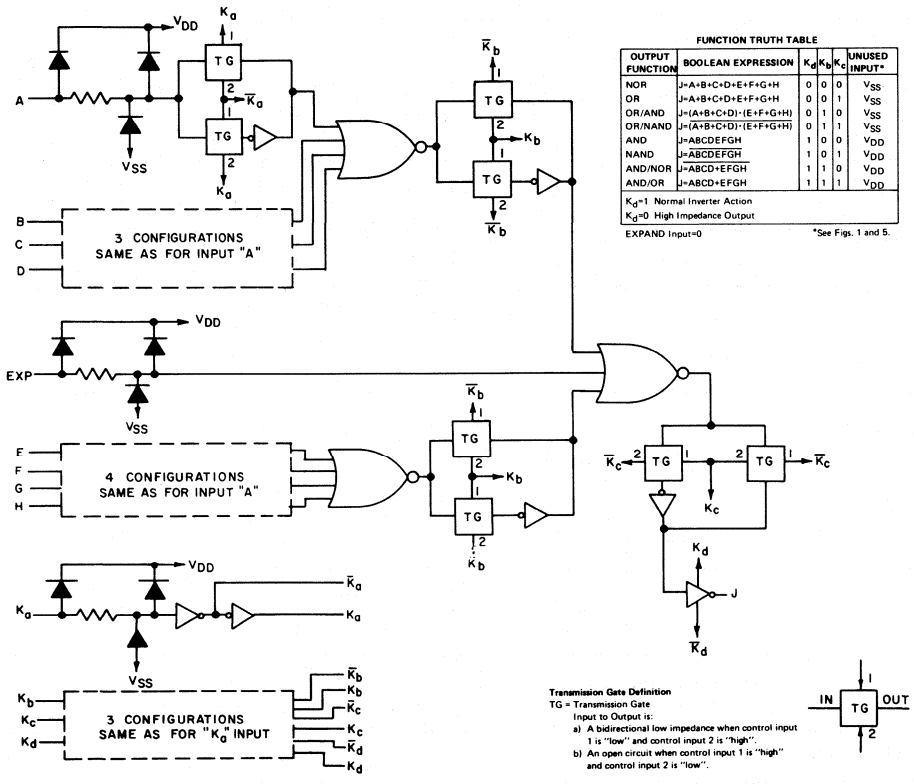
*Max. Limits represent worst-case limits for worst-case modes of operation shown in test circuits in Appendix.

Limits with black dot (●) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

NOTE 1: Test is a one input one output only.

DYNAMIC ELECTRICAL CHARACTERISTICS, Driving TTL at T_A = 25°C, $V_{DD} - V_{SS}$ = 5 V, C_L = 15 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Driving One TTL Load	LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES Fig. No.
Propagation Delay Time: High-to-Low Level	t_{PHL}	Series 54L, 74L	–	775	–	ns	–
		Series 54, 74	–	775	–		
Low-to-High Level	t_{PLH}	Series 54L, 74L	–	710	–	ns	
		Series 54, 74	–	600	–		



FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_d	K_b	K_c	UNUSED INPUT*
NOR	J=A+B+C+D+E+F+G+H	0	0	0	V_{SS}
OR	J=A+B+C+D+E+F+G+H	0	0	1	V_{SS}
OR/AND	J=(A+B+C+D)·(E+F+G+H)	0	1	0	V_{SS}
OR/NAND	J=$\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	J=ABCDEFGH	1	0	0	V_{DD}
NAND	J=$\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	J=$\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	J=ABCD+EFGH	1	1	1	V_{DD}

K_d=1 Normal Inverter Action
K_d=0 High Impedance Output
EXPAND Input=0
*See Figs. 1 and 5.

Fig. 2—Logic diagram and truth table.

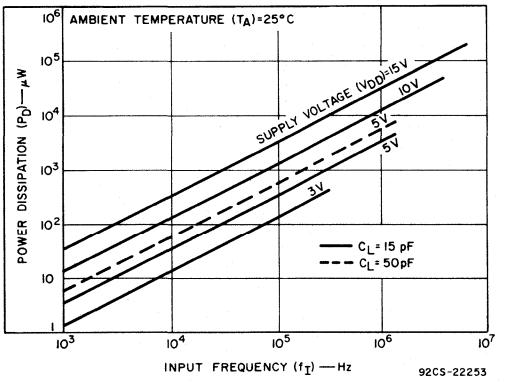


Fig. 3—Typical power dissipation as a function of input frequency.

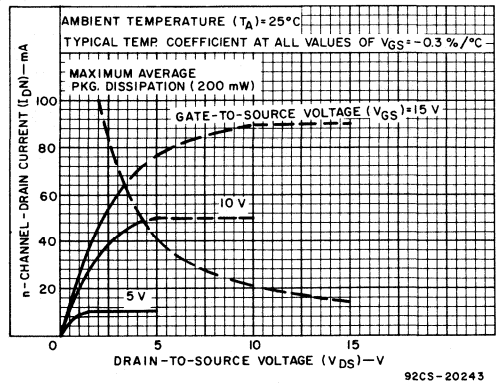
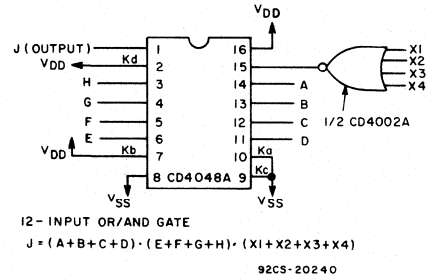


Fig. 4—Typical n-channel drain characteristics.

Applications of Expand Input

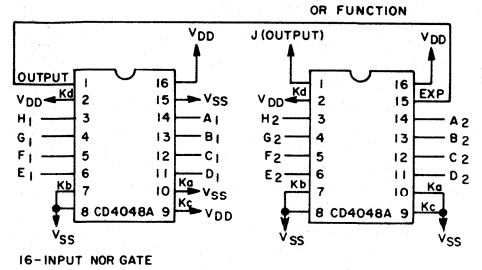


12-INPUT OR/AND GATE

$J=(A+B+C+D)\cdot(E+F+G+H)\cdot(XI+X2+X3+X4)$

92CS-20240

Fig. 5(a)—12-input OR/AND gate.

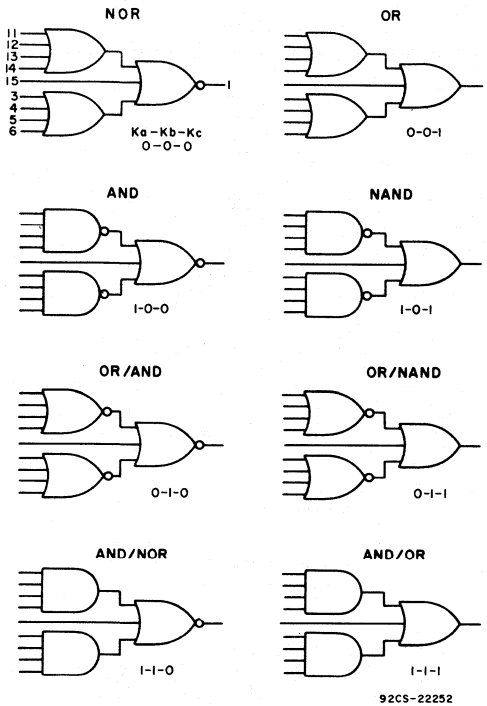


16-INPUT NOR GATE

$J=\overline{A_1+B_1+C_1+D_1+E_1+F_1+G_1+H_1+A_2+B_2+C_2+D_2+E_2+F_2+G_2+H_2}$

92CS-20241

Fig. 5(b)—16-input NOR gate.



92CS-22252

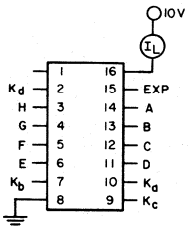
Fig. 5(c)—Actual-circuit logic configurations.

IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=\overline{(ABCDEFGH)\cdot(EXP)}$
NAND	NAND	$J=\overline{(ABCDEFGH)\cdot(EXP)}$
OR/AND	NOR	$J=(A+B+C+D)\cdot(E+F+G+H)\cdot(EXP)$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot(EXP)}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots.X_N$).

Fig. 5—Expansion logic and truth table.



Input Conditions For Leakage Measurements:

	K_d	H	G	F	E	K_b	K_c	K_a	D	C	B	A	EXP
(1)	0	0	0	0	0	0	0	0	0	0	0	0	0
(2)	1	0	0	0	0	1	1	1	0	0	0	0	0
(3)	0	1	1	1	1	0	0	0	1	1	1	1	1
(4)	1	1	1	1	1	1	1	1	1	1	1	1	1

92CS-22259

Fig. 6—Quiescent device current.

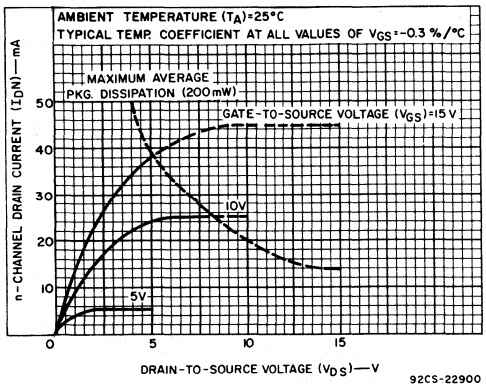


Fig. 7—Minimum n-channel drain characteristics.

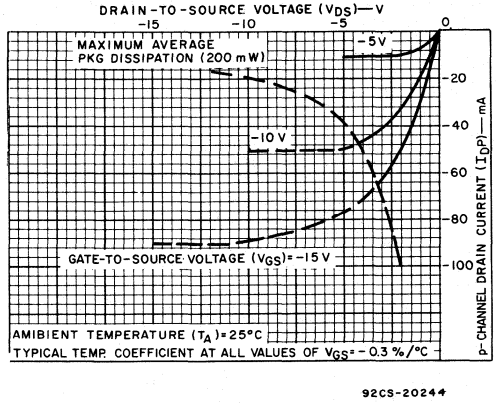


Fig. 8—Typical p-channel drain characteristics.

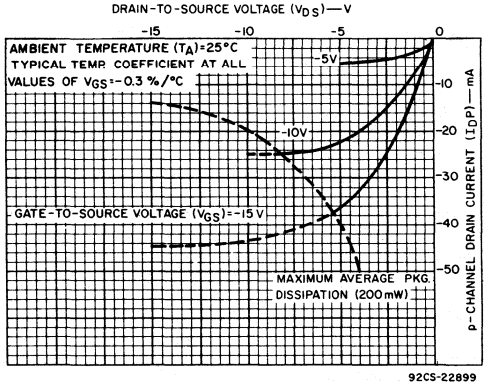


Fig. 9—Minimum p-channel drain characteristics.

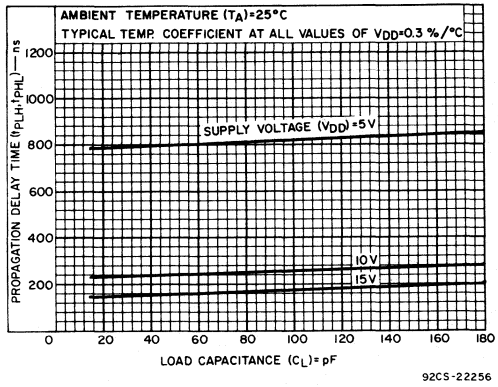


Fig. 10—Typical propagation delay time as a function of load capacitance.

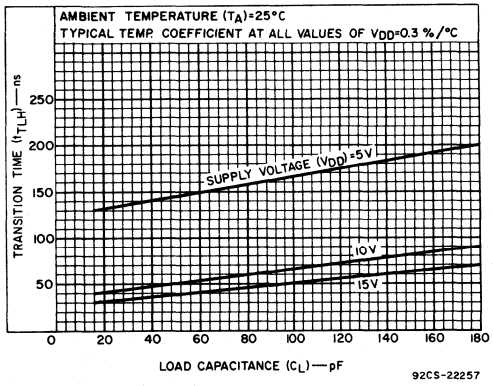


Fig. 11—Typical low-to-high level transition time as a function of load capacitance.

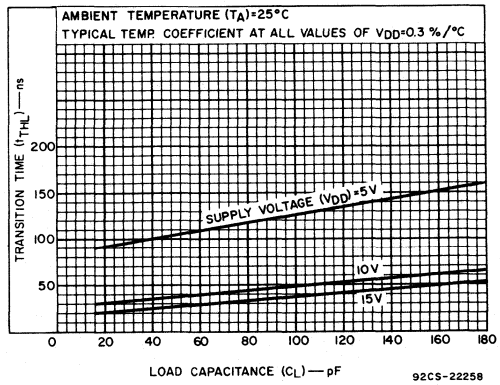


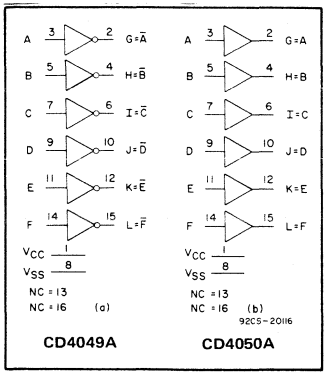
Fig. 12—Typical high-to-low level transition time as a function of load capacitance.

RCA Solid State Division

Digital Integrated Circuits

Monolithic Silicon

High-Reliability Slash(/) Series CD4049A/... CD4050A/...



CD4049A CD4050A

High-Reliability COS/MOS Hex Buffer/Converters

CD4049A—INVERTING TYPE CD4050A—NON-INVERTING TYPE

For Logic Systems Applications in Aerospace, Military, and Critical Industrial Equipment

Features:

- **Direct Drive to 2 TTL Loads at 5 V, V_{CC} = 5 V, $V_{OL} \leqslant$ 0.4 V, $I_{DN} \geqslant$ 3 mA**
- **High Source and Sink Current Capability**
- **General COS/MOS Characteristics**

Applications:

- **COS/MOS to DTL/TTL Hex Converter**
- **COS/MOS Current "Sink" or "Source" Driver**
- **COS/MOS High-to-Low Logic-Level Converter**

RCA CD4049A and CD4050A "Slash" (/) Series are high-reliability COS/MOS integrated circuits intended for a wide variety of logic function configurations in aerospace, military, and critical industrial equipment.

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC} = 5 V, $V_{OL} \leqslant$ 0.4 V, and $I_{DN} \geqslant$ 3 mA.)

Table 1 shows the range of voltage-supply levels that can be utilized for such logic level conversions. Conversion to logic-levels greater than +6 V is permitted provided that $V_{CC} \leqslant V_{IH}$. At 15 V the maximum allowable load capacitance is 5000 pF.

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation.

For simple logic-inversion applications it is more economical to use the CD4069A Hex Inverter scheduled for announcement in early 1974.

These devices are electrically and mechanically identical with standard COS/MOS CD4049A and CD4050A types described in data bulletin 599 and DATABOOK SSD-203 Series, but

TABLE I

FUNCTION	COS/MOS VOLTAGE RANGE (INPUT)	DTL/TTL VOLTAGE RANGE (OUTPUT)	POWER SUPPLY RANGE (V_{CC})
HEX LEVEL SHIFTER	3–15 V	3–6 V	3–6 V
HEX INVERTER HEX BUFFER	3–15 V	3–15 V	3–15 V

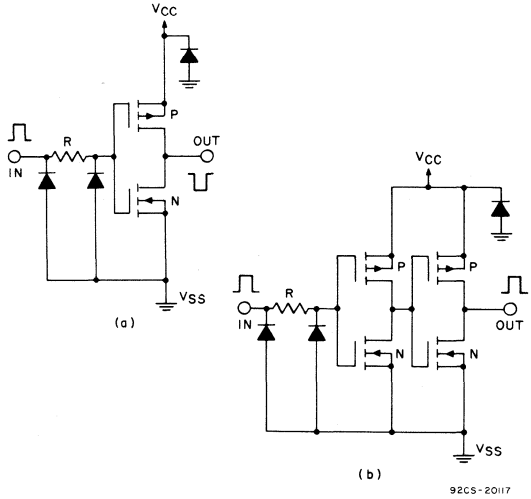


Fig. 1—a) Schematic diagram of CD4049A, 1 of 6 identical units; b) Schematic diagram of CD4050A, 1 of 6 identical units.

are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. In addition to the RCA high-reliability "Slash" (/) Series, RCA will offer these circuits screened to MIL-M-38510.

RCA Designation	MIL-M-38510 Designation
CD4049A	MIL-M-38510/05503
CD4050A	MIL-M-38510/05504

The packaged types in the CD4049A and CD4050A "Slash" (/) Series can be supplied to six screening levels – /1N, /1R, /1, /2, /3, /4 – which correspond to MIL-STD-883 Classes "A", "B", and "C". The chip versions of these types can be supplied to three screening levels – /N, /R, and standard chip.

Table II – Available Options Indicated by Check (√) Mark

Part Number	Screening Level		Package: 16-Lead Dual-in-Line Ceramic ("D" Suffix)	Package: 16-Lead Ceramic Flat-Pack ("K" Suffix)
Packaged Device				
CD4049AD, CD4049AK, CD4050AD, CD4050AK	Custom	/1N	√	√
		/1R	√	√
	Standard Equivalent to MIL-STD-883, Class "A","B","C"	/1	√	√
		/2	√	√
		/3	√	√
		/4	√	√
Chip			("H" Suffix)	
CD4049AH, CD4050AH	Custom	/N	√	
		/R	√	
	Standard Chip		√	

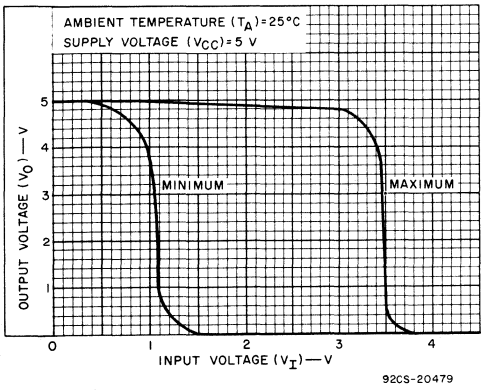


Fig. 2–Min. & max. voltage transfer characteristics of CD4049A.

For a description of these screening levels and for detailed information on test methods, procedures, and test sequence employed with high-reliability COS/MOS devices refer to high-reliability report RIC-102A, "High-Reliability COS/MOS CD4000A "Slash" (/) Series Types".

The CD4049A and CD4050A "Slash" (/) Series types are supplied in 16-lead dual-in-line ceramic packages ("D" suffix), in 16-lead ceramic flat packages ("K" suffix), or in chip form ("H" suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	−65 to +150	°C
Operating-Temperature Range	−55 to +125	°C
DC Supply Voltage Range (V_{CC}–V_{SS})	−0.5 to +15	V
Dissipation:		
Per Package	200	mW
Per Buffer	100	mW
All Inputs	$V_{SS} \leq V_I \leq 15$	V
Recommended Minimum DC Supply Voltage (V_{CC}–V_{SS})	3	V
Lead Temperature (During soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

Table III – Description of RCA IC High-Reliability Part Numbers

Packaged Device, CD4000AD/1N

CD4000A D /1N

Type Designation	Package Suffix Letter	Screening Level
	D = Dual-in-Line Ceramic	/1N
	K = Ceramic Flat-Pack	/1R
		/1
		/2
		/3
		/4

Chip Version, CD4000AH/N

CD4000A H /N

Type Designation	Package Suffix Letter	Screening Level
	H = Chip Version	/N
		/R

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	NOTES
					CD4049AD, CD4049AK CD4050AD, CD4050AK											
					−55°C			25°C			125°C					
		V_O Volts	V_{CC} Volts		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig. No.	
Quiescent Device Current	I_L	V_{IH} = V_{CC}		5	–	–	0.3	–	0.01	0.3	–	–	20	μA	17	1
				15	–	–	0.5•	–	0.01	0.5•	–	–	10•			
Quiescent Device Dissipation Package	P_D	V_{IH} = V_{CC}		5	–	–	1.5	–	0.05	1.5	–	–	100	μW		
				15	–	–	5	–	0.1	5	–	–	100			
Output Voltage Low-Level	V_{OL}			3	–	–	0.2•	–	–	0.6•	–	–	–	V	2–7	
				5	–	–	0.01	–	0	0.01	–	–	0.05			
				10	–	–	0.01	–	0	0.01	–	–	0.05			
				15	–	–	–	–	–	0.6•	–	–	0.7•			
High-Level	V_{OH}			3	2.8•	–	–	2.2•	–	–	–	–	–	V		
				5	4.99	–	–	4.99	5	–	4.95	–	–			
				10	9.99	–	–	9.99	10	–	9.95	–	–			
				15	–	–	–	14.4•	–	–	14.3•	–	–			
Threshold Voltage N-Channel	V_{THN}	I_D = -10μA			-0.7•	-1.7	-3 •	-0.7 •	-1.5	-3•	-0.3•	-1.3	-3•	V		2
P-Channel	V_{THP}	I_D = 10μA			0.7•	1.7	3 •	0.7 •	1.5	3•	0.3•	1.3	3•			
Noise Immunity (All Inputs) CD4049A	V_{NL}	V_{OH} = 3.6 V		5	1	–	–	1•	2.25	–	0.9	–	–	V	18	1
		V_{OH} = 7.2 V		10	2•	–	–	2•	4.5	–	1.9 •	–	–			
CD4050A		V_{OL} = 0.95 V		5	1.5	–	–	1.5•	2.25	–	1.4	–	–			
		V_{OL} = 2.9 V		10	3•	–	–	3•	4.5	–	2.9 •	–	–			
CD4050A	V_{NH}	V_{OH} = 7.2 V		10	2.9•	–	–	3•	4.5	–	3 •	–	–			
		V_{OH} = 3.6 V		5	1.4	–	–	1.5•	2.25	–	1.5	–	–			
CD4049A *For Definition, See Appendix SSD-207*		V_{OH} = 2.9 V		10	2.9•	–	–	3•	4.5	–	3 •	–	–			
		V_{OL} = 0.95 V		5	1.4	–	–	1.5•	2.25	–	1.5	–	–			
Output Drive Current N-Channel	I_{DN}		0.4	4.5	3.3	–	–	2.6•	5.2	–	1.8	–	–	mA	8,9	2
			0.4	5	3.75	–	–	3.0•	6	–	2.1	–	–			
			0.5	10	10	–	–	8•	16	–	5.6	–	–			
P-Channel	I_{DP}		4.5	5	-0.62	–	–	-0.5•	-1	–	-0.35	–	–			
			2.5	5	-1.85	–	–	-1.25•	-2.5	–	-0.9	–	–			
			9.5	10	-1.85	–	–	-1.25•	-2.5	–	-0.9	–	–			
Diode Test 100 μA Test Pin	V_{DF}				–	–	1.5•	–	–	1.5•	–	–	1.5•			
Input Current	I_I	V_{IH} = V_{CC}			–	–	–	–	10	–	–	–	–	pA		

Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

Note 1: Complete functional test, all inputs and outputs to truth table.
Note 2: Test is either a one input or a one output only.
Note 3: Test on all inputs and outputs.

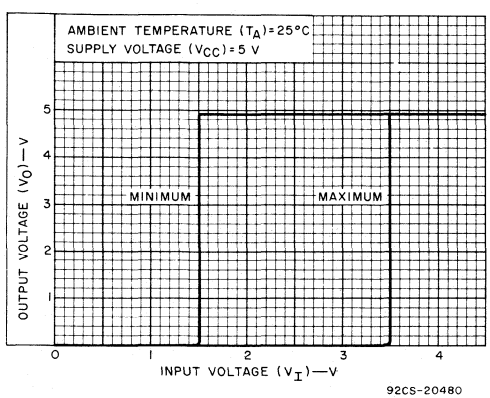


Fig. 3—Min. & max. voltage transfer characteristics of CD4050A.

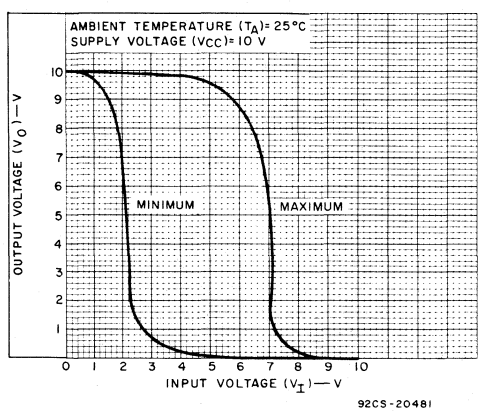


Fig. 4—Min. & max. voltage transfer characteristics for CD4049A.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns
Typical Temperature Coefficient for all values of V_{CC} = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	NOTES
				CD4049AD CD4049AK			CD4050AD CD4050AK					
			V_{CC} (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.			
Propagation Delay Time: High-to-Low Level	t_{PHL}	$V_{IH} = V_{CC}$	5	–	15	55	–	55	110	ns	10,11	1
			10	–	10	30•	–	25	55•			
Low-to-High Level	t_{PLH}	$V_{IH} = V_{CC}$	5	–	50	80	–	90	140	ns	12,13	
			10	–	25	55•	–	40	85•			
Transition Time: High-to-Low Level	t_{THL}	$V_{IH} = V_{CC}$	5	–	20	45	–	20	45	ns	14	1
			10	–	16	40•	–	16	40•			
Low-to-High Level	t_{TLH}	$V_{IH} = V_{CC}$	5	–	50	100	–	50	100	ns	15	
			10	–	30	60•	–	30	60•			
Input Capacitance	C_I	Any Input		–	5	–	–	5	–	pF	—	—

NOTE 1: Test is a one-input, one-output only.
Limits with black dot (•) designate 100% testing. Refer to RIC-102B "High-Reliability COS/MOS CD4000A Slash (/) Series Types", Tables 2 through 7 for testing sequence. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

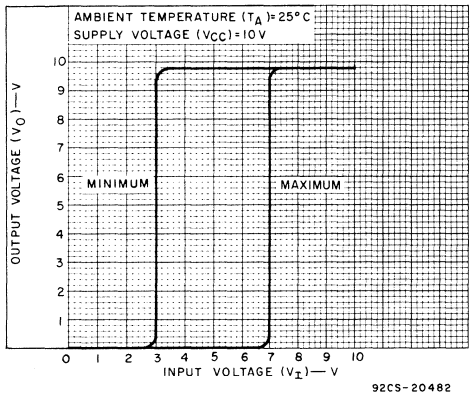


Fig. 5—Min. & max. voltage transfer characteristics for CD4050A.

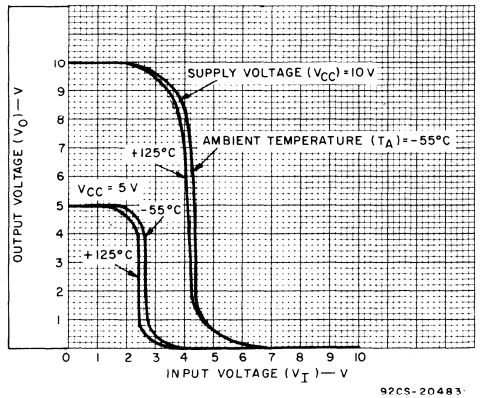


Fig. 6—Typ. voltage transfer characteristics as a function of temperature for CD4049A.

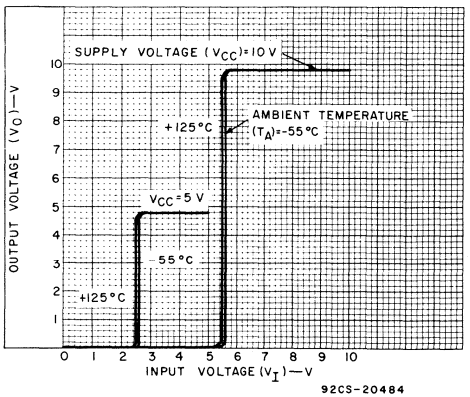


Fig. 7—Typ. voltage transfer characteristics as a function of temperature for CD4050A.

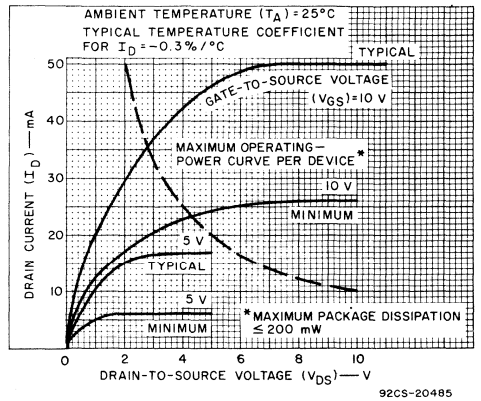


Fig. 8—Typ. & min. drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

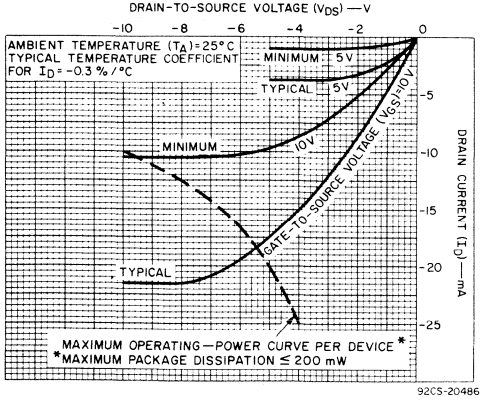


Fig. 9—Typ. & min. P-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

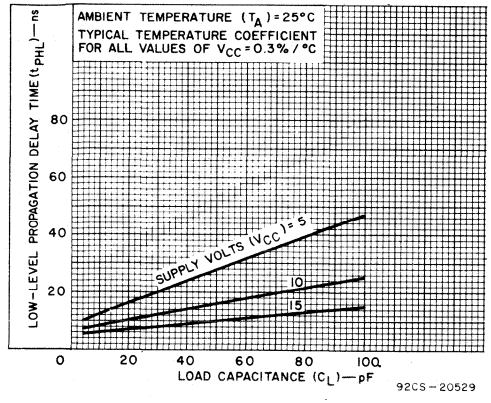


Fig. 10—Typ. high-to-low level propagation delay time vs. C_L for CD4049A.

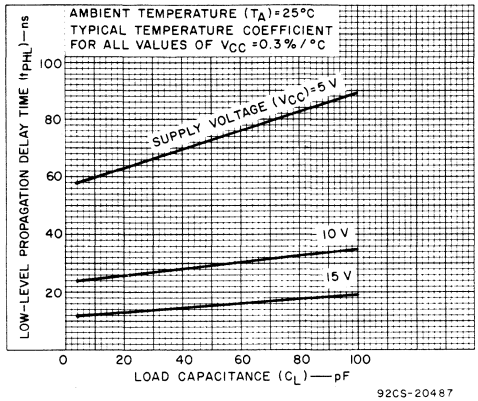


Fig. 11—Typ. high-to-low level propagation delay time vs. C_L for CD4050A.

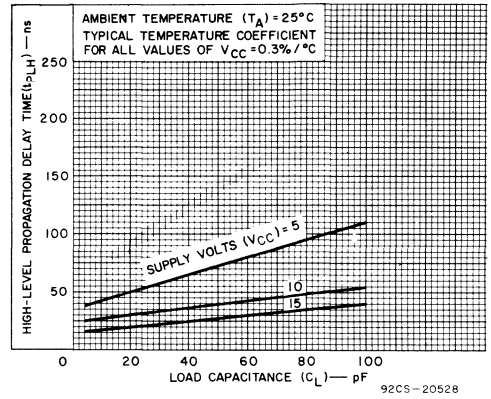


Fig. 12—Typ. low-to-high level propagation delay time vs. C_L for CD4049A.

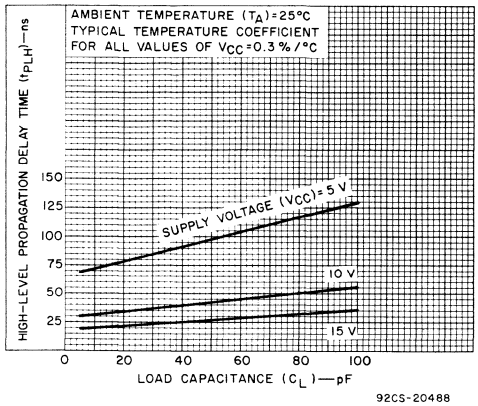


Fig. 13—Typ. low-to-high level propagation delay time vs. C_L for CD4050A.

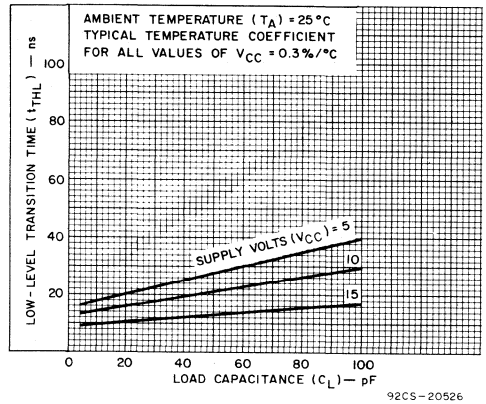


Fig. 14—Typ. high-to-low level transition time vs. C_L for CD4049A, CD4050A.

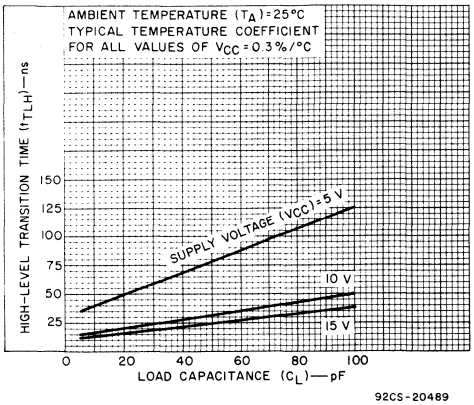


Fig. 15—Typ. low-to-high level transistion time vs C_L for CD4049A, CD4050A.

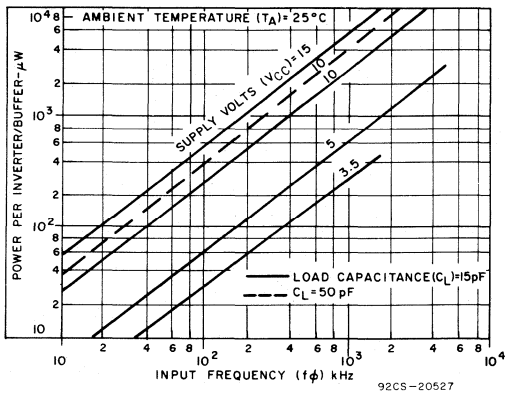


Fig. 16—Typ. dissipation characteristics for CD4049A, CD4050A.

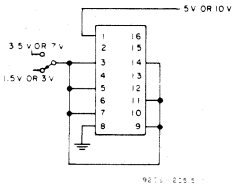


Fig. 17—Quiescent device current test circuit.

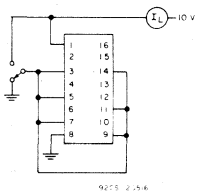


Fig. 18—Noise immunity test circuit.

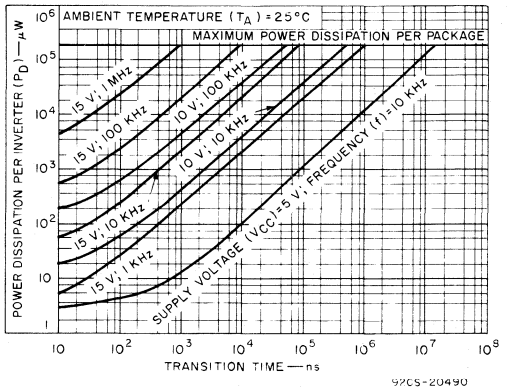


Fig. 19—Typ. power dissipation vs. transition time per inverter CD4049A.

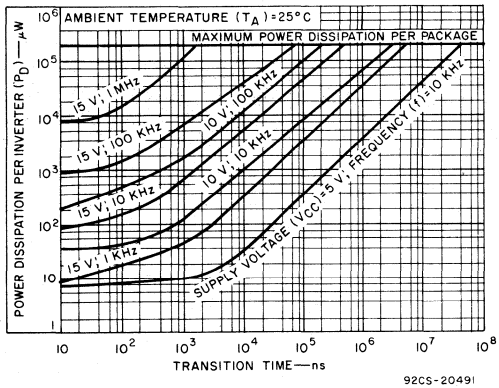


Fig. 20—Typ. power dissipation vs. transition time per inverter CD4050A.

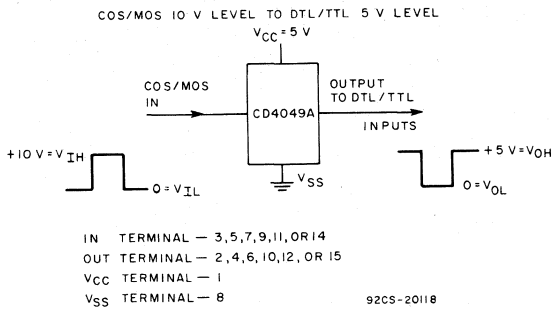


Fig. 21—Logic-level conversion application.

Handling Considerations for MOS Integrated Circuits

by S. Dansky

The input protection networks incorporated in all RCA COS/MOS devices are effective in a wide variety of device handling situations. To be totally safe, however, it is desirable to restate the general conditions for eliminating all possibilities of device damage.

Because MOS devices have extremely high input resistance, they are susceptible to damage when exposed to extremely high static electrical charges. To avoid possible damage to the devices during handling, testing, or actual operation, therefore, the following procedures should be followed:

1. The leads of devices should be in contact* with a conductive material, except when being tested or in actual operation, to avoid build-up of static charge.
2. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
3. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
4. Signals should not be applied to the inputs while the device power supply is off.
5. All unused input leads must be connected to either V_{SS} (ground) or V_{DD} (device supply), whichever is appropriate for the logic circuit involved.

Table I indicates general handling procedures recommended to prevent damage from static electrical charges.

Table I — General Handling Considerations

	Should be conductive	Should be grounded to common point
Handling Equipment	X	
Metal Parts of Fixtures and Tools		X
Handling Trays	X	X
Soldering Irons		X
Table Tops	X	X
Transport Carts		(Static Discharge Straps)
Manufacturing Operating Personnel		● (Utilize grounded metal wrist straps)
General Handling of Devices		● (Utilize grounded metal wrist straps)

Total protection results when personnel and materials are all at the same or ground potential.

Dry weather (relative humidity less than 30%) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed above take on added importance and should be adhered to without exceptions.

● 1-megohm series resistor.

Handling of Unmounted Chips

In handling of unmounted chips, care should be taken to avoid differences in voltage potential. A conductive carrier, or a carrier having a conductive overlay, should be used.

Another important consideration is the sequence in which bonds are made; the V_{DD} (device supply) connection should always be made before the V_{SS} (ground) bond.

Handling of Subassembly Boards

After COS/MOS units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system in which the proper voltages are applied, the board is no more than an extension of the leads of the device mounted on the board.

It is good practice during processing operations to put conductive clips or conductive tape[1] on the circuit-board terminals. This precaution prevents static charges from being transmitted through the board wiring to the devices mounted on the board.

* Dual-in-line leads imbedded in conductive foam, flat packs sandwiched between the foam.

[1] See Table II for sources of anti-static materials.

Table II – Partial List of Materials and Equipment Available for the Control of Static Charge

Company	Conductive Foam	Conductive Envelopes	Static Neutralizing Air Blowers	Anti-Static Sprays	Conductive Tape
Custom Material Inc. Chelmsford, Mass.	Velofoam #7672	Velobags #1798M	TEC Dynastat DS120		P. C. Contab Shunt
3M Company St. Paul, Minn.			Ionized Air Blower #905	See Technical Bulletins	Scotch Shielding Tapes
Scientific Enterprises, Inc. Bloomfield, Colo.			Micro Stat 575 Portable Ionizer		
Emerson & Cuming, Inc. Canton, Mass.	ECCOSORB LD26			See Technical Bulletins	

All normal flux removing and degreasing solvents can be used without adversely affecting the reliability of COS/MOS plastic devices.

When shipping completed boards, a conductive envelope or wrapper is desirable. Non-conductive plastic wrapping should be avoided.

Automatic Handling Equipment

When automatic handling equipment is used, static electricity may not always be eliminated through grounding techniques alone. Automatic feed mechanisms must be insulated from the devices under test at the point where the devices are connected to the test set. The device-insulated part of the automatic handling mechanism (anvil transport) can generate very high levels of static electricity which are developed by the continuous flow of devices sliding over and then separating from the anvil. Total control of these static voltages is critical because of the high throughputs associated with automatic handling.

Fortunately, the resolution of this problem is simple, practical, and inexpensive. Ionized-air blowers, which supply large volumes of ionized air to objects that are to be charge neutralized, are commercially available from many supply sources. Field experience with ionized-air techniques reveals this method to be extremely effective in eliminating static electricity when grounding techniques cannot be used.

Lead Bending and Forming Considerations

Other problems that can occur in handling COS/MOS devices relate to the proper handling of leads during mounting of devices. In any method of mounting integrated circuits that involves bending or forming of the device leads, it is extremely important that the leads be supported and clamped between the bend and the package seal, and that bends be made with extreme care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead flat-packaged integrated circuits, less than the lead thickness. It is also extremely important that the ends of the bent leads be perfectly straight and parallel to assure easy insertion through the holes in the printed-circuit board.

Bending, forming, and clinching of integrated-circuit leads produce stresses in the leads and can cause stresses in the seals if the above precautions are not taken.

Package Insertion Considerations

Special insertion jigs or automatic insertion equipment should be designed or adjusted so as not to cause damage to the IC body or package seal.

Soldering Time and Temperature

All device leads can withstand exposure to temperatures as high as 265°C for as long as ten seconds, and as close as 1/16 ± 1/32 inch from the body of the device.

Storing of COS/MOS Chips

COS/MOS chips, unlike most packaged devices, are non-hermetic devices, fragile and small in physical size, and therefore require the following special handling considerations:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper

consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

For further information on COS/MOS chip handling, refer to File No. 517, "CD4000AH Series COS/MOS Chips".

Storing of Printed-Circuit Boards

Excessive humidity (greater than 60%) should be avoided during circuit-board check-out to prevent the false impression of excessive device internal leakage. High relative humidity may cause leakage paths between closely spaced elements of the circuit boards, such as the terminals and insulated metallized connection strips. Normally this added leakage is not significant in non-COS/MOS devices. However, when the nanoampere-leakage advantages of COS/MOS devices are desired, leakage currents on circuit boards or non-hermetic modules which are affected by high humidity become of major concern and must be controlled by coating, cleaning, or better environmental controls.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure. A reasonable value of current limiting is 0.5 to 1.0 ampere.

Electrical Failure Modes Due To Improper Handling

When the possibilities exist for appreciable static-energy discharge, and proper handling techniques are not used, electrical damage can result as follows:

(a) shorted input protection diodes,

(b) shorted or open gates,

(c) opening in metal paths from the device input.

The presence of this type of device damage can be detected by curve-tracer checks of the input protection diodes, shown in Fig. 1, and also by a check of the device characteristics, especially mutual transconductance (g_m). Additional information on the RCA input protection circuit is given in ICAN-6218, "Gate-Oxide Protection Circuit in RCA COS/MOS Integrated Circuits".

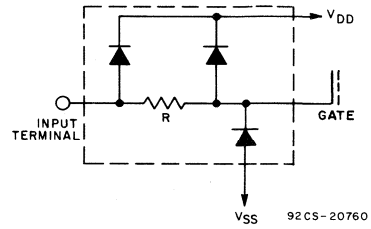


Fig. 1—An Example of COS/MOS Gate Input Protection, (For other circuits, see page 24).

Radiation Resistance of the COS/MOS CD4000A Series

by M. N. Vincoff

Complementary MOS (COS/MOS) integrated circuits possess many advantages which recommend their use in radiation-susceptible space and military environments. Several of the most significant of these advantages are: ultra-low standby-power consumption, high noise immunity,[1] extremely high packaging density, and inherently high reliability.[2] These advantages, along with the improved radiation resistance of the RCA CD4000A series over the CD4000 series described in earlier radiation studies,[3] exhibit the maturity reached by the MOS technology since 1971.

A number of studies of the radiation resistance of complementary MOS devices by NASA, the Navy and various companies in the space industry have revealed two areas of prime concern.[4-15] The first, *permanent* radiation exposure, as experienced in a space environment, causes a shift in threshold or switching voltage and a possible increase in leakage current, I_L. The second, *transient* radiation exposure, as experienced in an atomic environment, causes the output-voltage levels to respond to a pulse of ionizing radiation; this effect could change the state of the logic circuitry and require resetting of that circuitry for proper equipment or system operation.

Permanent-Radiation Resistance

The CD4000 series was resistant to permanent radiation levels of 2×10^4 rads (approximately 10^{12} e/cm^2). Now, however, RCA CD4000A-series devices without special shielding have been found to be resistant to radiation levels up to 2×10^5 rads (approximately 10^{13} e/cm^2), as shown in Fig. 1.[3] In this figure the change in switching voltage $\triangle V_S$ is plotted as a function of dose. The value of $\triangle V_S$ was calculated from the average value of $\triangle V_{TN}$ and $\triangle V_{TP}$ for the devices mentioned. The new radiation level of the CD4000A series represents a significant improvement over the CD4000 series. In addition, with minimal shielding (for example, 1/16-inch of aluminum) the CD4000A series can be used in application with levels of radiation up to 3×10^6 rads (approximately 10^{14} e/cm^2).[15]

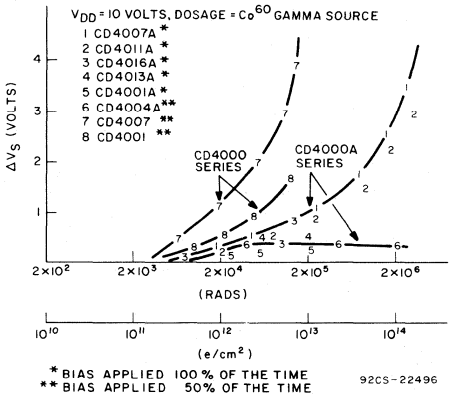


Fig. 1 – Permanent radiation resistance of CD4000A- and CD4000-series devices.

Transient-Radiation Resistance

The resistance of the CD4000A series to transient radiation is expected to be ten times better than that of the CD4000 series, which can withstand pulses of radiation of approximately 10^{10} rads/s.[5]

Design Considerations

The resistance of the CD4000A-series devices to either permanent- or transient-radiation exposure can be increased by providing either minimal shielding through the design of the equipment enclosure containing the devices or by locating the devices deep within the equipment in which they are used. In any case, the action taken will depend on the constraints dictated by the radiation environment imposed by the system or program. Each application must be tested and the results analyzed with the data in this Note as criteria. Test items to be considered are radiation environment, which

will vary greatly depending on dosage rate; time of exposure; amount of normal shielding; distance of the device from the radiation source; shielding afforded by the atmosphere; power-supply voltage selection; and switching cycles used during exposure. For example, consider the effects of permanent radiation on two spacecraft in 90-degree orbits at 600 and 1500 nautical miles from the earth, respectively. The dose-depth is determined as shown in the curves of Fig. 2. In these curves the dose in rads(Al)/day is plotted as a function of the thickness of spacecraft aluminum required to shield the devices from trapped electrons and protons.[4]

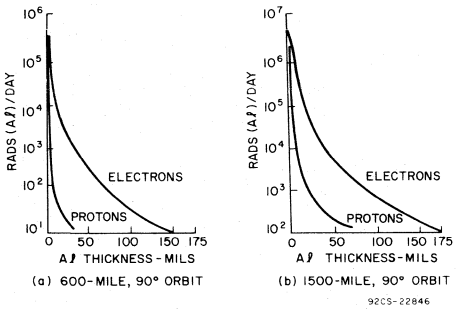


Fig. 2 – Dose-depth curves for trapped electrons and protons in spacecraft in orbit.

Conclusion

The RCA COS/MOS CD4000A series exhibits improved radiation resistance over the CD4000 series, and is well suited for use in many applications in which permanent and transient radiation effects are factors. When stringent radiation requirements are imposed, additional shielding can be employed to increase the radiation life of COS/MOS CD4000A-series devices to any desired level, i.e., to make their radiation resistance equivalent to that of bipolar devices.

Custom COS/MOS devices that can resist a radiation level of 10^6 rads are now being developed by means of an aluminum implantation process which requires one additional masking step in the production line.[11-14]

References

1. Eaton, S. S., "Noise Immunity of RCA COS/MOS Integrated Circuit Logic Gates", RCA Application Note ICAN-6176.
2. Vincoff, M. N. and Schnable, G. L., "COS/MOS is a High-Reliability Technology", RCA Technical Publication ST-6112.
3. Ezzard, G., "Radiation Effects on COS/MOS Devices", RCA Application Note ICAN-6604 (covers CD4000 series).
4. Brucker, G. J., "COS/MOS Device Sensitivity in Outer-Space Radiation Environment", Report No. X72002, Oct. 17, 1973, RCA Astro Electronics Division.
5. Dennehy, W. J., et al., "Transient Radiation Response in Complementary-Symmetry MOS Integrated Circuits", RCA Technical Publication ST-4308.
6. Poch, W. J., and Holmes-Siedle, A. G., "Permanent Radiation Effects in COS/MOS Integrated Circuits", RCA Technical Publication ST-4174 (covers CD4000 series).
7. Schambeck, W., "Radiation Resistance and Typical Applications of RCA COS/MOS Circuits in Spacecrafts", Telemetry Journal, June/July 1970 (covers CD4000 series).
8. Schambeck, W., "Effects of Ionizing Radiation on Low-Threshold C-MOS Integrated Circuits", DFVLR Institute for Satellite Electronics, Oberpfaffen-hofen, W. Germany, April 1972 (covers CD4000A series).
9. Danchenko, V., "Radiation Damage in MOS Integrated Circuits, Part I", Sept. 1971, Goddard Space Flight Center, Report X-711-71-410 (covers CD4000A series).
10. Poch, W. J., and Holmes-Siedle, A. G., "The Long-Term Effects of Radiation on Complementary MOS Logic Networks", IEEE Transactions on Nuclear Science NS-17 (6), Dec. 1970 (covers CD4000 series).
11. Smith, J. M., and Murray, L. A., "Radiation Resistant COS/MOS Devices", RCA Technical Publication ST-4723.
12. King, E. E., Nelson, G. P., and Hughes, H. L., "The Effects of Ionizing Radiation on Various COS/MOS Integrated Circuit Structures", IEEE Transaction in Nuclear Science, No. 6, pg. 264, Dec. 1972, RCA Technical Publication ST-6161.
13. Peel, John L., et al., "Radiation-Hardened Complementary MOS Using SiO_2 Gate Insulators", IEEE Transactions on Nuclear Science, No. 6, pg. 271, Dec. 1972.
14. Schlesier, K. M., et al., "COS/MOS Hardening Techniques", IEEE Transactions on Nuclear Science, No. 6, pg. 275, Dec. 1972.
15. Novell, J., "Radiation Test of RCA COS/MOS CD4000A Series Logic for IUE Orbit, Types CD4011AK/1 with and without shielding, and 1 x 256 RAM", U. S. Gov't. Spacecraft Data Management Branch, Code 734.1, June 28, 1973.

RCA Solid State Division

Digital Integrated Circuits

High-Reliability COS/MOS CD4000A Slash [/] Series Types

Screened to MIL-STD-883

RCA COS/MOS high-reliability slash (/) series digital integrated circuits are available for applications in aerospace, military, and industrial equipment. These COS/MOS circuits are supplied to six screening levels (/1N, /1R, /1, /2, /3, /4) which meet the electrical, mechanical, and environmental test methods and procedures established for microelectronic devices in MIL-STD-883. These six screening levels are equivalent to MIL-STD-883 Classes A, B, and C and are summarized in Table 1.

This bulletin defines the test procedures employed with COS/MOS devices to meet the reliability standards required by MIL-STD-883. The level /1N part includes SEM (Scanning Electron Microscope) Inspection to NASA-Goddard Specification GSFC-S-311-P-12A of MIL-M-38510, and Precap Visual Inspection, Condition A, Method 2010-1, MIL-STD-883. The level /R part includes the SEM inspection in addition to the requirements of level /1 part. RCA also offers the CD4000A slash (/) series screened to MIL-M-38510 (Slash (/) 50-Series Types). For COS/MOS devices in this series, refer to RIC-104 "COS/MOS CD4000A Series Types screened to MIL-M-38510".

The Product Flow Diagram shown in Fig. 1 lists a summary of processing, screening, tests, and sampling procedures followed in the manufacture of the COS/MOS devices.

Table 2 gives detailed information for the screening tests included in the Product Flow Diagram. Table 3 gives pre burn-in and post burn-in electrical tests and delta limits for critical test parameters. Tables 4 and 5 give test criteria for Final Electrical and Group A Electrical Tests. Tables 6 and 7 describe Group B and C Environmental Sampling Inspection tests.

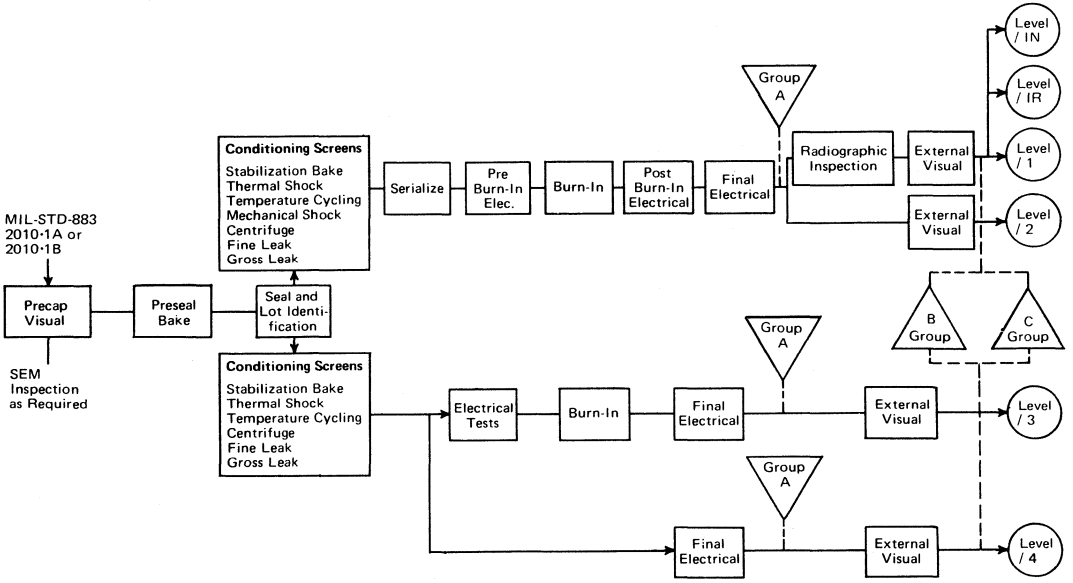


Fig. 1 — Product Flow Diagram (See Tables 2, 4, 5, 6, and 7 for Details)

Table I — Description of RCA Integrated-Circuit Screening Levels

Screening Levels		Application	Description
RCA Levels	**Equivalent to MIL-STD-883, Method 5004.1**		
For Packaged Devices			
/1N	Class A with SEM* Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **impossible and reliability is imperative**
/1R	Class A with SEM* Inspection and Condition B Precap Visual Inspection		
/1	Class A with Condition B Precap Visual Inspection		
/2	Class A with Condition B Precap Visual Inspection. Radiographic Inspection Omitted	Aerospace and Missiles	For devices intended for use where maintenance and replacement are **extremely difficult or impossible and reliability is imperative**
/3	Class B	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement **can be performed but are difficult and expensive**
/4	Class C	Military and Industrial. For example, on Ground Based Electronics	For devices intended for use where replacement **can readily be accomplished**
For Chips			
/N	SEM* Inspection and Condition A Precap Visual Inspection	Aerospace and Missiles	For hybrid applications where maintenance and replacement **are extremely difficult and reliability is imperative**
/R	SEM* Inspection and Condition B Precap Visual Inspection		
Standard Types	Condition B Precap Visual Inspection	Military and Industrial	For general applications

*SEM — Scanning Electron Microscope Inspection per NASA Specification GSFC-S-311-P-12

Note A: For details on Condition A and Condition B Precap Visual Inspection, refer to MIL-STD-883 Method 2010.1

Note B: Lot acceptance testing for chips is available on a custom basis

Ordering Information

1. **Packaged Device and Chip Type Number Identification**
When ordering a packaged device or a chip, it is important that the desired Screening Level and Package Designation for the Packaged Device, and the desired Screening Level for the Chip Version indicated by the appropriate suffix letters be added to the Part Number as shown below. For example, a CD4037A in a 14-lead dual-in-line ceramic package and processed to meet MIL-STD-883 Class A requirements with SEM Inspection plus Condition A Precap Visual would be identified as the CD4037A/1N. In similar manner, a CD4037A Chip having SEM inspection plus Condition A Precap Visual would be identified as the CD4037A/N.

2. **Data Supplied With Order for Packaged Devices**

	For the Following RCA Screening Levels
a) Product Screening Data	
Certificate of Compliance Signed by RCA Representative — Provides lot identity, customer order identity, lists and certifies tests, methods and conditions of required processing per MIL-STD-883	All
Group A Subgroup — Test Summary Attributes Data	All
Variables Data, Pre Burn-In and Post Burn-In	/1N, /1R, /1, /2
Radiographic Inspection Film and Film Inspection Record	/1N, /1R, /1
SEM Inspection Certificate of Compliance to NASA Specification GSFC-S-311-P-12 Includes lot identification and one worst-case photograph	/1N, /1R

b) Lot Quality Conformance Data —
Group B and Group C Subgroups

Attributes Data Summary of the Latest Group B and/or Group C Subgroup can be ordered at a nominal charge.

Special Group B and/or Group C quality conformance tests on samples from the specific lot of parts ordered will be considered on a custom basis only.

Description of RCA COS/MOS IC High-Reliability Part Numbers

Packaged Device CD4000AD/1N

CD4000A	D	/1N
Type Designation	**Package Suffix Letter** D = Dual-in-Line Ceramic K = Ceramic Flat Pack	**Screening Level** /1N /2 /1R /3 /1 /4 For Description, See Table 1

Chip Version, CD4000AH/N

CD4000A	H	/N
Type Designation	**Package Suffix Letter** H = Chip Version	**Screening Level** /N /R For Description, See Table 1

Table 2 – Description of Total Lot Screening (X = 100% Testing)

Test	Conditions	MIL-STD-883		RCA Screening Levels					
		Method	Conditions	/1N	/1R	/1	/2	/3	/4
SEM Inspection	NASA Per GSFC-S-311-P-12	–	–	X	X	–	–	–	–
Precap Visual	–	2010.1	A	X	–	–	–	–	–
Precap Visual	–	2010.1	B	–	X	X	X	X	X
Preseal Bake	16 to 32 hrs at 200°C	–	–	X	X	X	X	X	X
Seal & Lot Identification	–	–	–	X	X	X	X	X	X
Stabilization Bake	48 hrs. at 150°C	1008	C	X	X	X	X	X	X
Thermal Shock	15 cycles	1011	C	X	X	X	X	–	–
Temperature Cycling	10 cycles	1010	C	X	X	X	X	X	X
Mechanical Shock	5 pulses, Y_1 direction	2002	B	X	X	X	X	–	–
Centrifuge	Y_2, Y_1 direction	2001	E	X	X	X	X	–	–
	Y_1 direction only	2001	E	–	–	–	–	X	X
Fine Leak	–	1014	A	X	X	X	X	X	X
Gross Leak	–	1014	C	X	X	X	X	X	X
Electrical Tests	See Note 1	–	–	X	X	X	X	X	–
Serialize	–	–	–	X	X	X	X	–	–
Pre Burn-in Electrical	see Table 3	–	–	X	X	X	X	–	–
Burn-in	240 hours	1015	D or E	X	X	X	X	–	–
	168 hours	1015	D or E	–	–	–	–	X	–
Post Burn-in Electrical	Delta Requirements (See Table 3)	–	–	X	X	X	X	–	–
Final Electrical	–	–	–	–	–	–	–	–	–
a) 25°C	see Table 4	–	–	X	X	X	X	X	X
b) -55 and +125°C	see Table 4	–	–	X	X	X	X	X	S
Radiographic Inspection	1 view	2012	–	X	X	X	–	–	–
External Visual	–	2009	–	X	X	X	X	X	X

Note 1: See specific type data bulletin for test conditions and limits

Table 3 – Pre and Post Burn-In Electrical Tests and Delta Limits (T_A = 25°C)

CRITICAL PARAMETERS (at V_{DD} = 10 V)	SYMBOLS	LIMIT VALUES: For specific CD4000A Series Types and corresponding Δ limits for High-Reliability Versions (See Note 2).									
QUIESCENT DEVICE CURRENT	Total I_L(max)	0.1	0.5	1	2	5	10	15	25	50	Unit μA
	ΔI_L	0.05	0.2	0.3	0.5	1.0	1.3	1.5	2.5	5.0	μA
THRESHOLD VOLTAGE: "N" Channel	ΔV_{TH}"N"	◄ ±0.3 ►									V
"P" Channel	ΔV_{TH}"P"	◄ ±0.3 ►									V
DEVICE DRAIN CURRENT: Total	Total I_{DS}(min)	-0.1 - 0.5		0.5 - 2		2 - 5	5 - 10	10 - 25		25 - 50	mA
"N" Channel	ΔI_{DS}"N"	±0.1		±0.5		±0.75	±1	±2		±5	mA
"P" Channel	ΔI_{DS}"P"	±0.1		±0.5		±0.75	±1	±2		±5	mA

Note 2: For example, if a specific CD4000A Series Type has a max. quiescent device current of 0.5 μA at T_A = 25°C RCA will test to a Δ limit of 0.2 μA for the high-reliability version of that that type. In a similar manner, if a type has a quiescent device current rating of 5 μA, RCA will test to a Δ limit of 1.0 μA.

Table 4 – Final Electrical Tests

TEMPERATURE (T_A)	TEST	TEST CRITERIA		
		LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
+25°C	Selected Static Parameters	100%	100%	100%
+125°C	Selected Static Parameters	100%	100%	–
-55°C	Selected Static Parameters	100%	100%	–
+25°C	Selected Dynamic Parameters	100%	100%	–

Table 5 – Group A Electrical Sampling Inspection

SUBGROUP	TEST	CONDITION	LTPD		
			LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Selected Static Parameters	T_A = +25°C	5	5	5
2	Selected Static Parameters	T_A = +125°C	5	7	10
3	Selected Static Parameters	T_A = -55°C	5	7	10
4	Selected Dynamic Parameters	T_A = +25°C	5	5	5

Table 6 – Group B Environmental Sampling Inspection (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Physical Dimensions	2008	Test Cond. A per applicable data sheet	10	15	20
2	Marking Permanency	2008	Test Cond. B per Par. 3.2.1	4 devices (no failures)		
	Visual and Mechanical	2008	Test Cond. B 10 X mag.	1 device (no failure)		
	Bond Strength	2011	Test Cond. D 10 Devices minimum	5	15	20
3	Solderability	2003		10	15	15
4	Lead Fatigue	2004	Test Cond. B2 any 5 leads	10	15	15
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			

Note 1: Group B tests limited to a production period not to exceed 6 weeks
Note 2: Operating life circuits are included in specific type high-reliability data bulletins

Table 7 – Group C Environmental Sampling Inspection (Note 3)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1N, /1R, /1, /2	LEVEL /3	LEVEL /4
1	Thermal Shock	1011	Test Cond. C	10	15	15
	Temperature Cycling	1010	Test Cond. C			
	Moisture Resistance	1004	No Voltage Applied			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests – Note 4					
2	Mechanical Shock	2002	Test Cond. B, 0.5 ms	10	15	15
	Vibration, Var. Freq.	2007	Test Cond. A			
	Constant Acceleration	2001	Test Cond. E			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Test – Note 4					
3	Salt Atmosphere	1009	Test Cond. A Omit Initial Conditioning	10	15	15
4	High Temp. Storage	1008	Test Cond. C	7	7	7
	Critical Post Tests – Note 4		1000 hours			
5	Operating Life Critical Post Tests – Notes 2 & 4	1005	T_A - 125°C, 1000 hrs. Test Circuit (Note 2)	5	5	5
6	Steady State Bias	1015	Test Cond. A, 72 hrs.	7	–	–
	Critical Post Tests – Note 4		At T_A = 150°C (Note 4)			

Note 3: Group C tests performed at 3 month intervals
Note 4: Static parameters and limits are shown in specific type high-reliability data bulletins

RCA Solid State Division

Digital Integrated Circuits

High-Reliability COS/MOS MIL-M-38510 CD4000A Series Types

RCA COS/MOS high-reliability digital integrated circuits are available for applications in aerospace, military, and industrial equipment where screening requirements of MIL-M-38510 are specified. COS/MOS circuits are supplied to the three screening classes of MIL-M-38510 as specified in MIL-STD-883 Method 5004 Classes A, B, and C. Table 1 describes the screening levels.

This bulletin defines the procedures employed to manufacture COS/MOS CD4000A Series devices to meet the reliability requirements of MIL-M-38510. These COS/MOS devices are available in flat pack and dual-in-line ceramic packages.

Since 1970, RCA has been working closely with various aerospace and military agencies to qualify and provide COS/MOS devices to MIL-M-38510 specifications. Among these agencies are the NASA Goddard Space Flight Center, NASA Marshall Space Flight Center, NASA Headquarters Center in Washington, Rome Air Development Center, and the Defense Electronic Supply Center (DESC) at Dayton, a branch of the Defense Supply Agency.

MIL-M-38510 is the general specification for integrated circuits and is more comprehensive than MIL-STD-883. This general specification, introduced a year after MIL-STD-883 was in existence, adds a number of quality constraints not included in MIL-STD-883, which is a specification of test methods, procedures, and screening tests. COS/MOS parts are provided to MIL-M-38510 under a series of /50 numbers of which nine are in existence. These nine numbers cover twenty-seven COS/MOS types. Parts meet requirements similar to those of Classes A, B, and C of MIL-STD-883, Method 5004 screening, except that additional requirements, including more test conditions and tightened limits, are imposed. The Product Flow Diagram shown in Fig. 1 lists a summary of processing, screening, tests, and sampling procedures followed in the manufacture of COS/MOS devices. The additional criteria for each class of product are designated by an X in Table 2. Also provided in MIL-M-38510 tests are PDA's (Per-Cent Defective Allowed) of 10 per cent for the three burn-in operations performed on Class A product, and 10 per cent for the one burn-in of Class B product. Table 3 provides a list of the COS/MOS devices for which MIL-M-38510 /50-number specification sheets have been written. The 54(CD4008A) and 58(CD4016A) are still in preliminary status and are available for custom screening. Table 4 compares the processing requirements for COS/MOS integrated circuits to Class A Parts of MIL-M-38510. Tables 5 and 6 give test criteria for Final Electrical and Group A Electrical Tests. Tables 7 and 8 describe Group B and C Environmental Sampling Inspection tests. Table 9 describes the product assurance program RCA implements in the performance of MIL-M-38510. Table 10 provides a classification guide for COS/MOS circuits.

The processing of high-reliability COS/MOS integrated circuits is shown in Fig. 3. The wafer processing and metallization steps, the wafer finishing operations, and the wafer testing are the same as for standard-product COS/MOS devices. For Class A parts, an SEM inspection step is inserted after the wafer processing and metallization, as shown in Fig. 2. After these four basic operations are completed, the tested wafer is subjected to the special high-reliability processing. As shown in Fig. 3, thirty-eight additional processing and screening operations are required for Class A COS/MOS parts.

Ordering Information

Order COS/MOS MIL-M-38510 Series types by giving the appropriate reliability screen as shown in Fig. 4. For example, the CD4013AD processed to Class A requirements should be marked MIL-M-38510/05101ACA.

Table 1: Discription of MIL-M-38510 Screening Levels for RCA Integrated Circuits

MIL-M-38510	Application	Description
Class A (See Note 1)	Aerospace & Missiles	For devices intended for use where maintenance and replacement are extremely difficult or impossible and Reliability is imperative
Class B	Military & Industrial For example in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive
Class C	Military & Industrial For example, on Ground Based Electronics	For devices intended for use where replacement can readily be accomplished

Note 1: In the Condition A Visual Inspection of COS/MOS devices, the specification for metallization alignment in section 3.1.1.7(a) of the general specification will be changed, to read as follows:

No device shall be acceptable which exhibits the following defects in metallization alignment:

1. Contact window that has less than 50 per cent of its area covered by the metallization.
2. Contact which has less than 75 per cent of the length of two adjacent sides covered by the metallization.
3. A metallization path not intended to cover a contact window which is separated from the window by less than 0.25 mil.
4. Any exposure of the gate oxide.

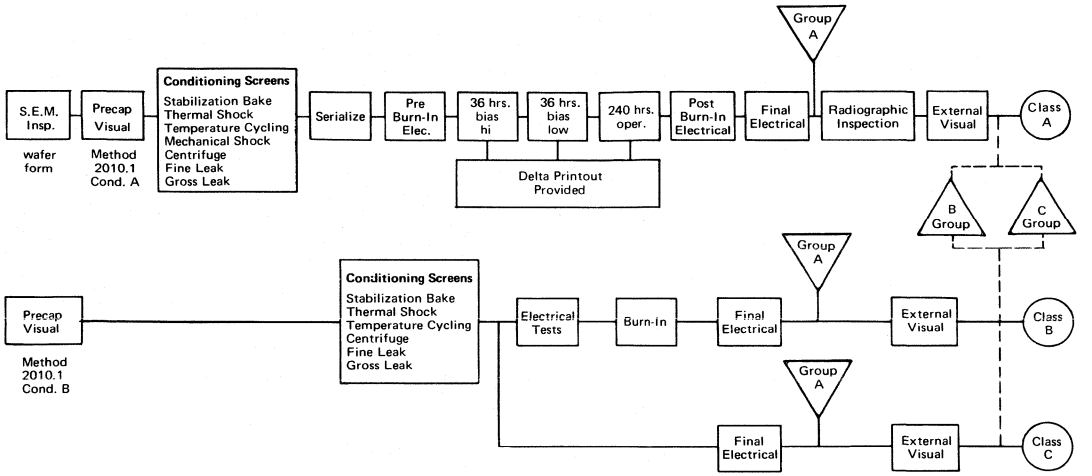


Fig. 1 — Product flow diagram for RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-M-38510

Table 2 — MIL-M-38510 Processing and Screening Requirements for RCA High-Reliability COS/MOS Integrated Circuits

MIL-M-38510 Processing	MIL-STD-883 METHOD	Condition	MIL-M-38510 CLASS		
			A	B	C
• Wafer					
SEM Inspection	GSFC-S-311-P-12	Photographs Available	X	—	—
• Assembly					
Precap Visual	2010.1	A	X	—	—
Precap Visual	2010.1	B	—	X	X
• Preconditioning					
Stabilization Bake	1008	C, 48 hours at 150°C	X	X	X
Thermal Shock	1011	C, 15 cycles, -65°C to +150°C	X	—	—
Temperature Cycle	1010	C, 10 cycles, -65°C to +150°C	X	X	X
Mechanical Shock	2002	B, 5 pulses	X	—	—
Centrifuge Y1	2001	E, 30000 G's	—	X	X
Centrifuge Y1 & Y2	2001	E, 30000 G's	X	—	—
Fine Leak	1014	A	X	X	X
Gross Leak	1014	C	X	X	X
• Test and Burn-In					
Initial Test	—	MIL-M-38510/50 Series	X	X	—
Serialize			X	—	—
Bias Burn-In, Two 36-Hr. Deltas	1015	A, Bias at 150°C	X	—	—
Operating Burn-In, 240-Hr. Deltas	1015	A, Bias at 150°C	X	—	—
Operating Burn-In 168 Hrs.	1015	D, Dynamic at +125°C	—	X	—
Final Electrical DC +25°C		MIL-M-38510/50 Series	X	X	X
Final Electrical AC +25°C		MIL-M-38510/50 Series	X	X	S
Final Electrical DC -55°C		MIL-M-38510/50 Series	X	X	S
Final Electrical AC -55°C		MIL-M-38510/50 Series	S	S	S
Final Electrical DC +125°C		MIL-M-38510/50 Series	X	X	S
Final Electrical AC +125°C		MIL-M-38510/50 Series	S	S	S
• X-ray Inspection	NH853004(3E)	Two views	X	—	—

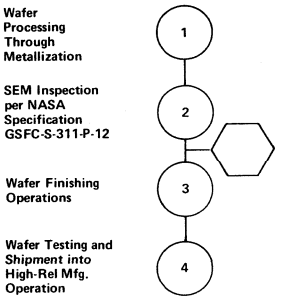


Fig. 2 — Basic processing operations for high-reliability COS/MOS integrated circuits that require SEM inspection as described in MIL-M-38510

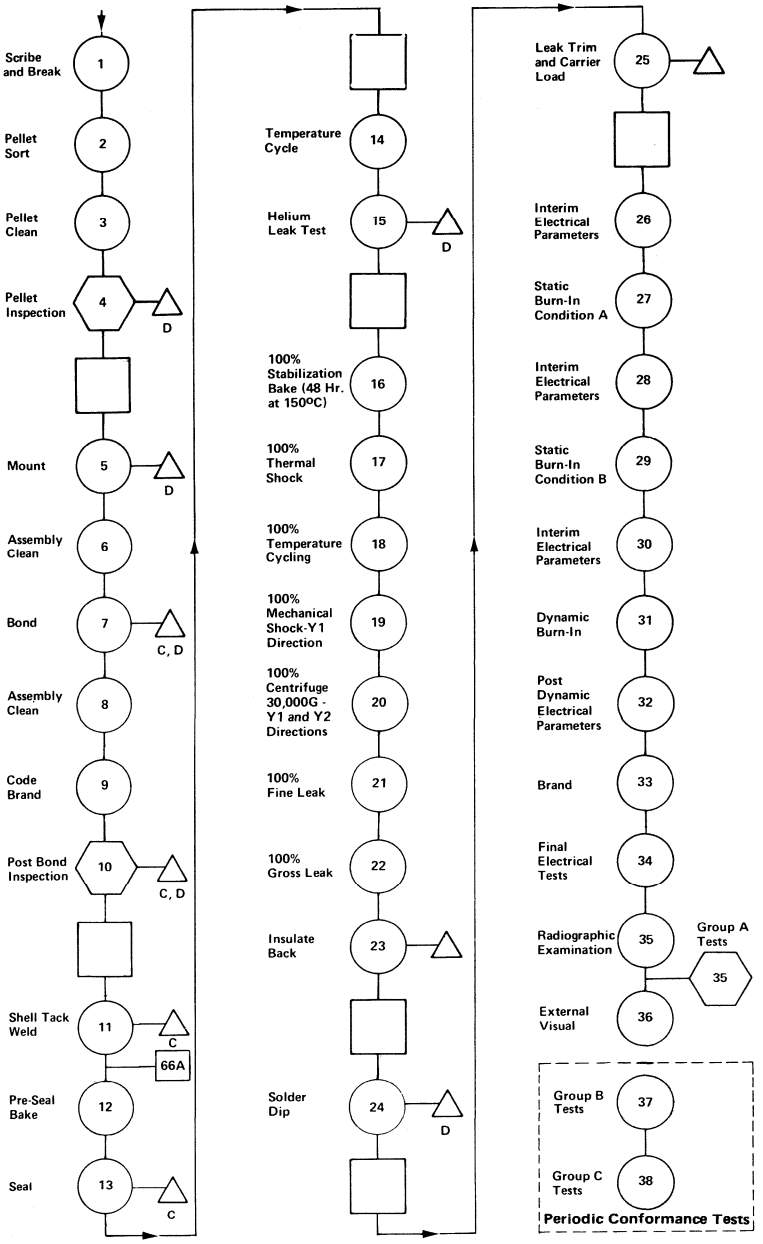


Fig. 3 — COS/MOS High-Reliability Flow Chart for Flat Pack MIL-M-38510 Class A Device.

Table 3 — COS/MOS Devices For Which MIL-M-38510/50 Specifications Have Been Written

Detailed Electrical Specification, MIL-M-38510	Device Covered
MIL-M-38510/050	
01	CD4011A
02	CD4012A
03	CD4023A
MIL-M-38510/051	
01	CD4013A
02	CD4027A
MIL-M-38510/052	
01	CD4000A
02	CD4001A
03	CD4002A
04	CD4025A
MIL-M-38510/053	
01	CD4007A
02	CD4019A
MIL-M-38510/054	
01	CD4008A

Detailed Electrical Specification, MIL-M-38510	Device Covered
MIL-M-38510/055	
01	CD4009A
02	CD4010A
03	CD4049A
04	CD4050A
MIL-M-38510/056	
01	CD4017A
02	CD4018A
03	CD4020A
04	CD4022A
05	CD4024A
MIL-M-38510/057	
01	CD4006A
02	CD4014A
03	CD4015A
04	CD4021A
05	CD4031A
MIL-M-38510/058	
01	CD4016A

Table 4 — Comparison of MIL-STD-883 and MIL-M-38510 Detailed Screening Requirements for Class A COS/MOS Devices.

SCREENING PROCEDURES	CLASS A MIL-M-38510
1. SEM Inspection	Yes
2. Visual, Precap	2010.1 Cond. A
3. Pre-conditioning	MIL-STD-883
4. Bias Burn-in High	36 hrs @ 150°C,Δ(2) PDA(1)
5. Bias Burn-in Low	36 hrs @ 150°C,Δ(2) 5%
6. Operating Burn-in	PDA 5% Max; if over 5%
240 Hrs @ 125°C	Reject Entire Lot Δ(2)
7. DC Elect. Tests	Measurements on all Inputs and Outputs
8. DC Test-Limit Resolution	1 nA Minimum 1 mV Minimum
9. AC Dynamic Tests	Measurements on all Inputs and Outputs
10. AC Test Limits	At 50-pF Load
11. Radiographic	View in Two Dimensions
12. Parts Qualification Requirement	9 Detailed Electrical Specifications
13. Group B Qualification Conformance	9 Generic Families for 27 COS/MOS Types

(1) PDA = Per-Cent Defective Allowable

(2) Δ = Delta Variables, Data Required

Table 5 — Final Electrical Tests

TEMPERATURE (T_A)	TESTS TO MIL-M-38510 SPECIFICATIONS	TEST CRITERIA		
		Class "A"	Class "B"	Class "C"
+25°C	DC & Functional Parameters	100%	100%	100%
+125°C	DC & Functional Parameters	100%	100%	–
-55°C	DC & Functional Parameters	100%	100%	–
+25°C	AC Parameters	100%	100%	–

Table 6 — Group A Electrical Sampling Inspection

SUBGROUP OF MIL-STD-883 5005.1	TESTS TO MIL-M-38510 SPECIFICATIONS	CONDITION	LTPD		
			Class "A"	Class "B"	Class "C"
1, 7	DC & Functional Parameters	T_A = +25°C	5	5	5
2, 8	DC & Functional Parameters	T_A = +125°C	5	7	10
3, 8	DC & Functional Parameters	T_A = -55°C	5	7	10
4, 9	AC Parameters	T_A = +25°C	5	5	5
10	AC Parameters	T_A = +125°C	5	5	–
11	AC Parameters	T_A = -55°C	7	7	–

Details of static, functional, and dynamic tests, conditions, and limits appear in the specific MIL-M-38510/50 Series Specifications shown in Table 10

Table 7 — Group B Environmental Sampling Inspection to MIL-M-38510 (Note 1)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1, /2	LEVEL /3	LEVEL /4
1	Physical Dimensions	2008	Test Cond. A per applicable data sheet	10	15	20
2	Marking Permanency	2008	Test Cond. B per Par. 3.2.1	4 devices (no failures)		
	Visual and Mechanical	2008	Test Cond. B 10 X mag.	1 device (no failure)		
	Bond Strength	2011	Test Cond. D 10 Devices minimum	5	15	20
3	Solderability	2003		10	15	15
4	Lead Fatigue	2004	Test Cond. B2 any 5 leads	10	15	15
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			

Note 1: Group B tests limited to a production period not to exceed 6 weeks.
Note 2: Operating life circuits are included in specific type bulletins.

Table 8 — Group C Environmental Sampling Inspection to MIL-M-38510 (Note 3)

SUBGROUP	TEST	MIL-STD-883		LTPD		
		REFERENCE	CONDITIONS	LEVELS /1, /2	LEVEL /3	LEVEL /4
1	Thermal Shock	1011	Test Cond. C	10	15	15
	Temperature Cycling	1010	Test Cond. C			
	Moisture Resistance	1004	No Voltage Applied			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Tests — Note 4					
2	Mechanical Shock	2002	Test Cond. B, 0.5 ms	10	15	15
	Vibration, Var. Freq.	2007	Test Cond. A			
	Constant Acceleration	2001	Test Cond. E			
	Fine Leak	1014	Test Cond. A			
	Gross Leak	1014	Test Cond. C			
	Critical Post Test — Note 4					
3	Salt Atmosphere	1009	Test Cond. A Omit Initial Conditioning	10	15	15
4	High Temp. Storage	1008	Test Cond. C	7	7	7
	Critical Post Tests — Note 4		1000 hours			
5	Operating Life Critical	1005	T_A = +125°C, 1000 hrs.	5	5	5
	Post Tests — Notes 2 & 4		Test Circuit (Note 2)			
6	Steady State Bias	1015	Test Cond. A, 72 hrs.	7	—	—
	Critical Post Tests — Note 4		At T_A = +150°C (Note 4)			

Note 3: Group C tests performed at 3 month intervals.
Note 4: Static parameters and limits are shown in specific type high-reliability integrated-circuit data bulletin.

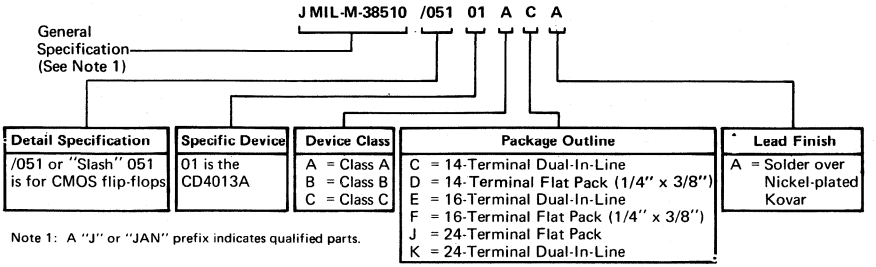


Fig. 4 — Guide to the reliability, class, package and lead finish of RCA high-reliability COS/MOS integrated circuits processed in accordance with MIL-M-38510

Table 9 – MIL-M-38510 Product-Assurance Program Requirements

In-House Documentation Covering These Areas

a. Conversion of customer requirements into manufacturer's internal instructions
b. Personnel training and testing
c. Inspection of incoming materials, utilities and work in process
d. Quality-control operations
e. Quality-assurance operations
f. Design, processing, tool and materials standards and instructions
g. Cleanliness and atmospheres in work areas
h. Design, material, and process change control
i. Tool and test equipment maintenance and calibration
j. Failure and defect analysis and data feedback
k. Corrective action and evaluation
l. Incoming, in process, and outgoing inventory control

In-House Records Covering These Areas

a. Personnel training and testing
b. Inspection operations
c. Failure reports and analyses
d. Changes in design, materials, or processing
e. Equipment calibrations
f. Process utility and material controls
g. Product lot identification

A Program Plan Covering These Areas

a. Functional block organization chart
b. Manufacturing flow chart
c. Proprietary-document listing
d. Examples of design, material, equipment, and processing instructions
e. Examples of records
f. Examples of design, material and process change control documents
g. Examples of failure and defect analysis and feedback documents
h. Examples of corrective action and evaluation documents

Table 10 – Product Classification Guide for RCA High-Reliability Integrated Circuits

COS/MOS Types (MIL-STD-883 Slash Series and MIL-M-38510 Series)					
		MIL-M-38510/50 Series Types			MIL-M-38510/50 Series Types
Standard-Product Type No.	Descriptive Title	Detailed Electrical Specification No.	Standard-Product Type No.	Descriptive Title	Detailed Electrical Specification No.
CD4000A	Dual 3-Input NOR Gate Plus Inverter	MIL-M-38510/05201	CD4032A	Triple Serial Adder (Positive Logic)	See Note 1
CD4001A	Quad 2-Input NOR Gate	MIL-M-38510/05202	CD4033A	Decade Counter/Divider	See Note 1
CD4002A	Dual 4-Input NOR Gate	MIL-M-38510/05203	CD4034A	8-Stage Parallel-In/ Parallel-Out Bidirectional Static Shift Register	See Note 1
CD4006A	18-Stage Static Shift Register	MIL-M-38510/05701			
CD4007A	Dual Complementary Pair Plus Inverter	MIL-M-38510/05301	CD4035A	4-Stage Parallel In/ Parallel Out Shift Register	See Note 1
CD4008A	4-Bit Full Adder With Parallel Carry-out	MIL-M-38510/05401	CD4036A	4-Word X 8-Bit RAM (Binary Addressing)	See Note 1
CD4009A	Hex Buffer/Converter (Inverting Type)	MIL-M-38510/05501	CD4038A	Triple Serial Adder (Negative Logic)	See Note 1
CD4010A	Hex Buffer/Converter (Non-Inverting Type)	MIL-M-38510/05502	CD4039A	4-Word X 8-Bit RAM (Direct Word-Line Addressing)	See Note 1
CD4011A	Quad 2-Input NAND Gate	MIL-M-38510/05001	CD4040A	12-Stage Binary/Ripple Counter	See Note 1
CD4012A	Dual 4-Input NAND Gate	MIL-M-38510/05002	CD4041A	Quad True/Complement Buffer	See Note 1
CD4013A	Dual "D" Type Flip-Flop With Set/Reset Capability	MIL-M-38510/05101	CD4042A	Quad Clocked "D" Latch	See Note 1
CD4014A	8-Stage Static Shift Register (Synchronous)	MIL-M-38510/05702	CD4043A	Quad 3-State NOR R/S Latch	See Note 1
CD4015A	Dual 4-Stage Static Shift Register	MIL-M-38510/05703	CD4044A	Quad 3-State NAND R/S Latch	See Note 1
CD4016A	Quad Bilateral Switch	MIL-M-38510/05801	CD4045A	21-Stage Clock-Timer Counter	See Note 1
CD4017A	Decade Counter/Divider	MIL-M-38510/05601	CD4046A	Micropower Phase-Locked Loop	See Note 1
CD4018A	Presettable Divide-By-"N" Counter	MIL-M-38510/05602	CD4047A	Low-Power Monostable/ Astable Multivibrator	See Note 1
CD4019A	Quad AND-OR Select Gate	MIL-M-38510/05302	CD4048A	Multi-Function Expandable 8-Input Gate	See Note 1
CD4020A	14-Stage Ripple-Carry Binary Counter/Divider	MIL-M-38510/05603	CD4049A	Hex Buffer/Converter (Inverting Type)	MIL-M-38510/05503
CD4021A	8-Stage Static Shift Register (Asynchronous)	MIL-M-38510/05704	CD4050A	Hex Buffer/Converter (Non-inverting Type)	MIL-M-38510/05504
CD4022A	Divide-By-8 Counter/ Divider With 8 Decoded Outputs	MIL-M-38510/05604	CD4051A	Single 8-Channel Analog Multiplexer	See Note 1
CD4023A	Triple 3-Input NAND Gate	MIL-M-38510/05003	CD4052A	Differential 4-Channel Analog Multiplexer	See Note 1
CD4024A	7-Stage Binary Ripple Counter	MIL-M-38510/05605	CD4053A	Triple 2-Channel Analog Multiplexer	See Note 1
CD4025A	Triple 3-Input NOR Gate	MIL-M-38510/05204	CD4057A	LSI 4-Bit Arithmetic Array	See Note 1
CD4026A	Decade Counter/Divider		CD4061A	256-Bit Random-Access Memory	See Note 1
CD4027A	Dual J-K Master-Slave Flip-Flop With Set/ Reset Capability	MIL-M-38510/05102	CD4066A	Quad Bilateral Switch	See Note 1
CD4028A	BCD-TO-Decimal Decoder	See Note 1			
CD4029A	Presettable Up/Down Counter	See Note 1			
CD4030A	Quad Exclusive-OR Gate	See Note 1			
CD4031A	64-Stage Static Shift Register	MIL-M-38510/05705			

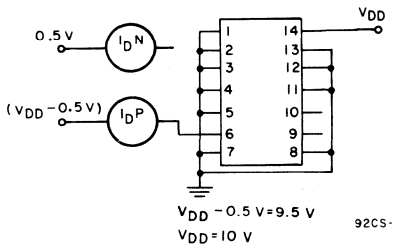
Detailed specifications for the above standard-product circuits are available in the RCA COS/MOS DATABOOK SSD-203B.
MIL-M-38510 specifications can be obtained from the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, Pa. 19120

Note 1: No MIL-M-38510 detailed electrical specifications have been defined as yet. RCA plans to add additional types to the MIL-M-38510 series starting in 1974.
These parts are available with RCA Slash (/) Series screened to MIL-STD-883. See Reliability Report RIC-102B for details.

OUTPUT DRIVE-CURRENT TEST-CIRCUIT CONNECTIONS

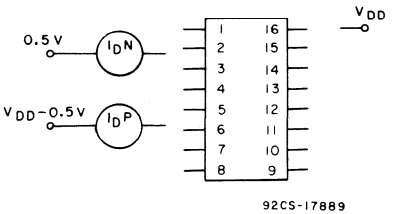
For supply voltages V_{DD} of 5 V and 10 V
Test voltages applied to output terminals

Example:
CD4000A I_DP



Example:

16-Lead Types



Type	Measurement	Ground	V_{DD}	0.5V	V_{DD}-0.5V
CD4000A	I_DN	1-4,7,8,11-13	5,14	6*	
	I_DP	1-5,7,8,11-13	14		6▲
CD4001A	I_DN	2,5-9,12,13	1,14	3*	
	I_DP	1,2,5-9,12,13	14		3▲
CD4002A	I_DN	3-5,7,9-12	2,14	1*	
	I_DP	2-5,7,9-12	14		1▲
CD4006A‡	I_DN	1,4-7	14	13	
	I_DP	4-7	1,14		13
CD4007A●	I_DN	7	6,14	8*	
	I_DP	6,7	14		13▲
CD4008A■	I_DN	9,15	16	14	
	I_DP	8	1-7,9,15,16		14
CD4009A	I_DN	5,7-9,11,14	1,3,16	2*	
	I_DP	3,5,7-9,11,14	16		2▲
CD4010A	I_DN	3,5,7-9,11,14	16	2*	
	I_DP	5,7-9,11,14	1,3,16		2▲
CD4011A	I_DN	5-9,12,13	1,2,14	3	
	I_DP	1,5-9,12,13	2,14		3
CD4012A	I_DN	7,9-12	2-5,14	1	
	I_DP	2,7,9-12	3-5,14		1
CD4013A	I_DN	3,5-11	4,14	1	
	I_DP	3-5,7-11	6,14		1
CD4014A‡	I_DN	1,4-8,11,13-15	9,16	3	
	I_DP	4-8,11,13-15	1,9,16		3

Type	Measurement	Ground	V_{DD}	0.5V	V_{DD}-0.5V
CD4015A‡	I_DN	1,6-8,14,15	16	5	
	I_DP	1,6,8,14,15	7,16		5
CD4017A	I_DN	8	13-16	3	
	I_DP	8	13-16		2
CD4018A	I_DN	1-3,7-10,12	14-16	11	
	I_DP	1-3,7,8,10	9,12,14-16		11
CD4019A	I_DN	1-9	14-16	13	
	I_DP	1-8	9,14-16		13
CD4020A‡	I_DN	8,11	16	9	
	I_DP	8,11	16		9
CD4021A	I_DN	1,4-8,10,11,13-15	9,16	3	
	I_DP	4-8,10,11,13-15	1,9,16		3
CD4022A‡	I_DN	8,13,15	16	2	
	I_DP	8,13,15	16		2
CD4023A	I_DN	1,2,7,8,11-13	3-5,14	6	
	I_DP	1-3,7,8,11-13	4,5,14		6
CD4024A (K,D)	I_DN	1,7	2,14	12	
	I_DP	2,7	14		12
CD4024A (T)	I_DN	1,12	2,3	11	
	I_DP	3,12	2		11
CD4025A	I_DN	1-4,7,8,11-13	5,14	6*	
	I_DP	1-5,7,8,11-13	14		6▲
CD4026A	I_DN	1-3,8,15	16	10	
	I_DP	1,2,8	3,15,16		10

* For V_{DD} = 5V, test voltage is 0.4V.

▲ For V_{DD} = 5V, test voltage is V_{DD} −2.5V.

‡ These types must be clocked in the proper state. Clock pulses should be applied to the following terminals:

CD4006A	Terminal 3
CD4014A	Terminal 10
CD4015A	Terminal 9
CD4020A	Terminal 10
CD4022A	Terminal 14

● These tests should also be performed using 3V and V_{DD} −3 V instead of 0.5V and V_{DD} −0.5V.

■ When I_DN and I_DP are tested at any other output, use 3V and V_{DD} −3V instead of 0.5V and V_{DD} −0.5V.

OUTPUT DRIVE-CURRENT TEST-CIRCUIT CONNECTIONS (Cont'd)

Type	Measurement	Ground	V_{DD}	0.5V	V_{DD}-0.5V
CD4027A	I_DN	3,5-13	4,16	1	
	I_DP	3-6,8-13	7,16		1
CD4028A	I_DN	8,10-13	16	2	
	I_DP	8,10-13	16		3
CD4029A	I_DN	3,4,8,10,12,13,15	1,5,9,16	6	
	I_DP	5,8,15	1,3,4,9,10,12,13,16		6
CD4030A	I_DN	1,2,5-9,12,13	14	3	
	I_DP	2,5-9,12,13	1,14		3
CD4031A	I_DN	1,2,8,10,15	7,16	6	
	I_DP	1,2,7,8,10,15	16		6
CD4032A	I_DN	2,3,5-8,10-15	16	9	
	I_DP	2,3,5,6,8,10-15	7,16		9
CD4033A	I_DN	1-3,8,14	15,16	10	
	I_DP	1-3,8,15	14,16		10
CD4034A	I_DN	1-8,10-12,15	9,13,14,24	16	
	I_DP	10-12,15	1-9,13,14,24	–	16
CD4035A	I_DN	2-4,6-12	5,16	1	
	I_DP	3,4,6-12	2,5,16		1
CD4036A	I_DN	3-12,21-23	1,2,24	20+	
	I_DP	11,12,21-23	1-10,24		20+
CD4038A	I_DN	2,3,5-8,10-15	10,11,16		9
	I_DP	2,3,5,6,8,12-15	7,10,11,16	9	
CD4039A	I_DN	3-12,21-23	1,2,24	20+	
	I_DP	11,12,21-23	1-10,24	–	20+

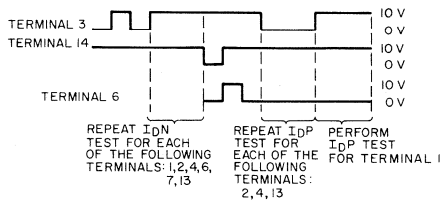
Type	Measurement	Ground	V_{DD}	0.5V	V_{DD}-0.5V
CD4040A	I_DN	8,10	11,16	9	
	I_DP	8,11	10♦,16		9
CD4041A (TRUE)	I_DN	3,6,7,10,13	14	1	
	I_DP	6,7,10,13	3,14		1
CD4041A (COMP)	I_DN	6,7,10,13	3,14	2	
	I_DP	3,6,7,10,13	14		2
CD4042A	I_DN	4,7,8,13,14	6,15,16	2	
	I_DP	7,8,13,14	4-6,16		2
CD4043A	I_DN	4,6-8,11,12,14,15	3,5,16	2	
	I_DP	3,6-8,11,12,14,15	4,5,16		2
CD4044A	I_DN	3,4,7,8	5,6,11,12,14-16	13	
	I_DP	4,7,8	3,5,6,11,12,14-16		9
CD4045A	I_DN	2,14	1,3	8	
	I_DP	2,14	1,3		8
CD4046A⊕	I_DN	8,9,11	5,12,16	1,2,4 6,7,13	
	I_DP	5,7,8,9,11	12,16		1,2 4,13
CD4047A	I_DN	5,7,12	4,6,8,9,14	10	
	I_DP	7,9	3-6,8,12,14		10
CD4048A	I_DN	3-14	2,15,16	1	
	I_DP	3-15	2,16		1
CD4049A	I_DN	8	1,3,5,7,9,11,14	6,10◆	
	I_DP	3,5,7-9,11,12	1		6,10◆
CD4050A	I_DN	3,5,7-9,11,14	1	6,10◆	
	I_DP	8	1,3,5,7,9,11,14		6,10◆

+ For V_{DD} = 5V, use terminal 13 instead of 20.

♦ Clock terminal 10 until output goes "high".

◆ For V_{DD} = 5V, use terminals 2 and 4 instead of terminals 6 and 10. I_DN and I_DP tests are not performed for the CD4016A.

⊕ Use the following waveforms for these tests:

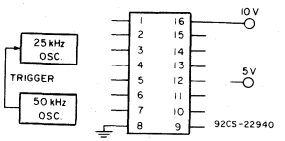


I_DN AND I_DP TESTS ARE NOT PERFORMED FOR CD4016A

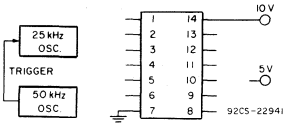
92CS-22939

LIFE-TEST CIRCUIT CONNECTIONS

Operating Life Tests

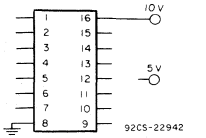


CONNECTIONS TO ALL TERMINALS (EXCEPT 8 & 16) ARE MADE THROUGH 47 kΩ RESISTORS

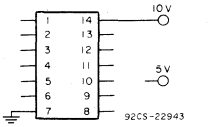


CONNECTIONS TO ALL TERMINALS (EXCEPT 7 & 14) ARE MADE THROUGH 47 kΩ RESISTORS

Biased Life Tests



CONNECTIONS TO ALL TERMINALS (EXCEPT 8 & 16) ARE MADE THROUGH 47 kΩ RESISTORS



CONNECTIONS TO ALL TERMINALS (EXCEPT 7 & 14) ARE MADE THROUGH 47 kΩ RESISTORS

Type	Open	Ground	5V	10V	Oscillator 50-KHz	Oscillator 25-KHz	Open	Ground	10V
CD4000A		1,2,4,5,7,12,13	6,9,10	14	3,8,11		6,9,10	1-5,7,8	11-14
CD4001A		2,6,7,9,13	3,4,10,11	14	1,5,8,12		3,4,10,11	1,2,5-7	8,9,12-14
CD4002A	6,8	3-5,7,10-12	1,13	14	2,9		1,6,8,13	2-5,7	9-12,14
CD4006A	2	7	8-13	14	3	1,4-6	2,8-13	5-7	1,3,4,14
CD4007A		1,4,7,9,13	12	2,5,11,14	3,6,10		1,5,8,12,13	4,6,7,9	2,3,10,11,14
CD4008A		8	10-14	16	2,4,6,15	1,3,5,7,9	10-14	4-9	1-3,15,16
CD4009A	13	8	2,4,6,10,12,15	1,16	7,9,11,14	3,5	2,4,6,10,12, 13,15	3,5,7,8	1,9,11,14,16
CD4010A	13	8	2,4,6,10,12,15	1,16	7,9,11,14	3,5	2,4,6,10,12, 13,15	3,5,7,8	1,9,11,14,16
CD4011A		7	3,4,10,11	2,6,9,13,14	1,5,8,12		3,4,10,11	1,2,5-7	8,9,12-14
CD4012A	6,8	7	1,13	3-5,10-12,14	2,9		1,6,8,13	2-5,7	9-12,14
CD4013A		4,6-8,10	1,2,12,13	14	3,11	5,9	1,2,12,13	6,7,9-11	3-5,8,14
CD4014A		1,4-9,13-15	2,3,12	16	10	11	2,3,12	1,4,6,8,14	5,7,9-11,13, 15,16
CD4015A		6,8,14	2-5,10-13	16	1,9	7,15	2-5,10-13	1,6,8,15	7,9,14,16
CD4016A		7	2,3,9,10	14	5,6,12,13	1,4,8,11	2,3,9,10	1,6-8,12	4,5,11,13,14
CD4017A		8,13,15	1-7,9-12	16	14		1-7,9-12	8,13,15	14,16
CD4018A		2,8,9,15	4-6,11,13	1,3,12,16	7,14	10	4-6,11,13	2,7,8,12,15	1,3,9,10,14,16
CD4019A		2,4,6,8,9,15	10-13	14,16	1,3,5,7		10-13	4-9	1-3,14-16
CD4020A		8,11	1-7,9,12-15	16	10		1-7,9,12-15	8-11	10,16
CD4021A		1,4-9,13-15	2,3,12	16	10	11	2,3,12	1,4,6,8,14	5,7,9-11,13, 15,16
CD4022A	6,9	8,13,15	1-5,7,10-12	16	14		1-7,9-12	8,13,15	14,16
CD4023A		7	6,9,10	1,2,4,5,12-14		3,8,11	6,9,10	1-5,7,8	11-14
CD4024A (K,D)	8,10,13	2,7	3-6,9,11,12	14	1		3-6,8-13	2,7	1,14
CD4024A (T)	8	3,12	4-7,9-11	2	1		4-11	3,12	1,2
CD4025A		1,2,4,5,7,12,13	6,9,10	14	3,8,11		6,9,10	1-5,7,8	11-14
CD4026A	4,6,7,9-14	2,3,8,15	5	16	1		4-7,9-14	8	1,2,3,15,16
CD4027A		4,7-9,12	1,2,14,15	5,6,10,11,16	3,13		1,2,14,15	8-13	3-7,16
CD4028A	1-3,6,7,9,14,15	8	4,5	10,12,13,16		11	1-7,9,14,15	8,10,11	12,13,16
CD4029A		1,3-5,8,12,13	2,6,7,11,14	9,10,16	15		2,6,7,11,14	1,3-5,8-10, 12,13,15	16
CD4030A		2,6,7	3,4,10,11	9,13,14	1,5,8,12		3,4,10,11	2,5-8	1,9,12-14

LIFE-TEST CIRCUIT CONNECTIONS (CONT'D)

	Operating Life Tests						Biased Life Tests		
					Oscillator				
Type	Open	Ground	5V	10V	50-KHz	25-KHz	Open	Ground	10V
CD4031A	3-5,7,9,11-14	1,8,10	6	16	2	15	3-7,9,11-14	1,2,8,10	15,16
CD4032A		2,5-8	1,4,9	10	3,11,13,15	10,12,14	1,4,9	2,3,5-8,10-13	14-16
CD4033A	4,6,7,9-13	2,3,8,14,15	5	16	1		4-7,9-14	8	1-3,15,16
CD4034A	16-23	9,12-14	1-8	11,24	15	10	1-8	10,12,15,17 19,21,23	9,11,13,14, 16,18,20,22,24
CD4035A	Jumpered 1,3,4	2,5,7-12,14,15	13	16	6		1,13-15	4-10	2,3,11,12,16
CD4036A		11,12,21,22	13-20	2,24	1 ,23	3-10	1,13-20	3-12,21,22	2,23,24
CD4038A		2,5-8	1,4,9	16	3,11,13,15	10,12,14	1,4,9	2,3,5-8,10-13	14-16
CD4039A		11,12	13-20	24	1,2,21-23	3-10	1,13-20	3-12,21,22	2,23,24
CD4040A		8,11	1-7,9,12-15	16	10		1-7,9,13-15	8,11	10,16
CD4041A		7	1,2,4,5,8, 9,11,12	14	3,6,10,13		1,2,4,5, 8,9,11,12	3,6,7	10,13,14
CD4042A		8	1,2,3,9-12,15	6,16	5	4,7,13,14	1-3,9-12,15	6,8,13,14	4,5,7,16
CD4043A	13	8	1,2,9,10	5,16	4,6,12,14	3,7,11,15	1,2,9,10,13	3,7,8,12,14	4,5,6,11,15,16
CD4044A	2	8	1,9,10,13	5,16	4,6,12,14	3,7,11,15	1,2,9,10,13	4,6,8,11,15	3,5,7,12,14,16
CD4045A	4-6,9-13,15	2,14•		1,3•,7,8	16		4-6,9-13,15	2,14•	1,3•,7,8,16
CD4046A	1,4,6,7, 10,11,13,15	8,9	2	3,5,12,16	14		1,2,4,6,7, 10,11,13,15	3,8,9,14	5,12,16
CD4047A		7,9,12	1,2,10,11,13	4,5,14	6,8	3	1,2,10,11,13	4,7,12	3,5,6,8,9,14
CD4048A		8,15	1	2,16	9-14	3-7	1	3-6,8,15	2,7,9-14,16
CD4049A	13	8	2,4,6,10, 12,15	1,16	7,9 11,14	3,5	2,4,6,10, 12,13,15	3,5,7,8	1,9,11,14,16
CD4050A	13	8	2,4,6,10, 12,15	1,16	3,5,7,9 11,14		2,4,6,10, 12,13,15	3,5,7,8	1,9,11,14,16

NOTE: For 14-terminal devices, terminal No. 7 is always connected directly to ground, and terminal No. 14 is always connected directly to the power supply.

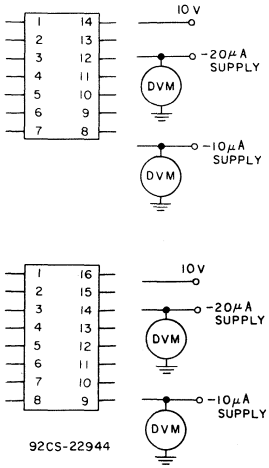
For 16-terminal devices, terminal No. 8 is always connected directly to ground, and terminal No. 16 is always connected directly to the power supply.

All other terminals are connected through a 47-KΩ resistor to the points indicated on the chart.

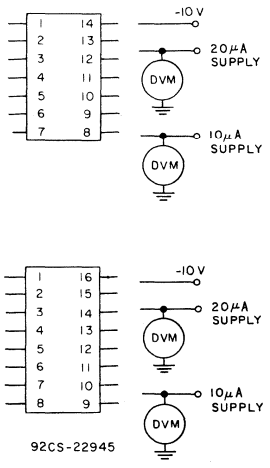
• No 47-KΩ resistor.

THRESHOLD-VOLTAGE TEST-CIRCUIT CONNECTIONS

N-Channel Tests



P-Channel Tests



Type	Ground	10V	V_{TH} measured at −20 μA Supply	V_{TH} measured at −10 μA Supply	Ground	−10V	V_{TH} measured at 20 μA Supply	V_{TH} measured at 10 μA Supply
CD4000A	3	14		1,2,4,5,7,8,11-13	3	1,2,4,5,7,8,11-13		14
CD4001A	1	14		2,5-9,12,13	1	2,5-9,12,13		14
CD4002A	2	14		3-5,7,9-12	2	3-5,7,9-12		14
CD4006A	3	14	1,4-7		3	1,4-7	14	
CD4007A	6	14,8		7	6	7,13		14
CD4008A	9	2,4,6,15,16	1,3,5,7,8		9	1,3,5,7,8	2,4,6,15,16	
CD4009A	3	1,16		5,7-9,11,14	3	5,7-9,11,14		1,16
CD4010A	3	1,16		5,7-9,11,14	3	5,7-9,11,14		1,16
CD4011A	2	1,14		5-9,12,13	2	5-9,12,13		1,14
CD4012A	2	3-5,14		7,9-12	2	7,9-12		3-5,14
CD4013A	3	14		4-11	3	4-11		14
CD4014A	10	16	1,4-9,11,13-15		10	1,4-9,11,13-15	16	
CD4015A	1	16	6-9,14,15		1	6-9,14,15	16	
CD4016A	13	5,6,12,14		7	13	5-7,12		14
CD4017A	15	16	8,13,14		15	8	13,14,16	
CD4018A	15	16	1-3,7-10,12,14		15	1-3,7-10,12,14	16	
CD4019A	9	14-16	1-8		9	1-8	14-16	
CD4020A	10,11	16	8		10	8,11	16	
CD4021A	10	16	1,4-9,11,13-15		10	1,4-9,11,13-15	16	
CD4022A	14	13,15,16	8		14	8,13,15	16	
CD4023A	3	4,5,14		1,2,7,8,11-13	3	1,2,7,8,11-13		4,5,14
CD4024A (K,D)	1,2	14	7		1	2,7	14	
CD4024A (T)	1,3	2	12		1	3,12	2	
CD4025A	3	14		1,2,4,5,7,8,11-13	3	1,2,4,5,7,8,11-13		14
CD4026A	1	2,3,15,16		8	1	2,3,8,15		16
CD4027A	13	3-7,9-12,16		8	13	3-12		16
CD4028A	10	16	8,11-13		10	8,11-13	16	
CD4029A	10	1,3-5,9,12,13,15,16	8		10	1,3-5,8,9,12,13,15	16	
CD4030A	8	14		1,2,5-7,9,12,13	8	1,2,5-7,9,12,13		14
CD4031A	2	1,10,15,16*	8		2	1,8,10,15*	16	
CD4032A	3	2,5-7,10-16		8	3	2,5-8,10-15		16
CD4033A	1	2,3,14-16	8		1	2,3,8,14,15	16	
CD4034A	10	9,11,13-24		12	10	1-9,11-15		24
CD4035A	6	16	2-5,7-12		6	2-5,7-12	16	
CD4036A	23	1-11,21,22,24	12		23	1-12,21,22	24	

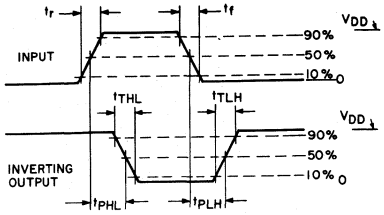
THRESHOLD-VOLTAGE TEST-CIRCUIT CONNECTIONS (CONT'D)

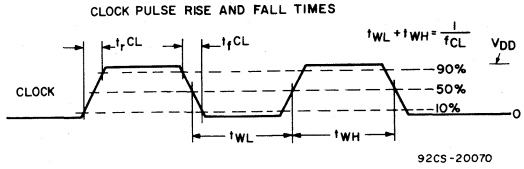
	N-Channel Tests				P-Channel Tests			
			$-V_{TH}$ measured at				$-V_{TH}$ measured at	
Type	Ground	10V	−20 μA Supply	−10 μA Supply	Ground	−10V	20 μA Supply	10 μA Supply
CD4038A	3	2,5,6,10-16		8	3	2,5-8,10-15		16
CD4039A	23	1-11,21,22,24	12		23	1-12,21,22	24	
CD4040A	10,11	16	8		10	8,11	16	
CD4041A	3	14		6,7,10,13	3	6,7,10,13		14
CD4042A	6	16		4,5,7,8,13,14	6	4,5,7,8,13,14		16
CD4043A	5	16		3,4,6-8,11,12,14,15	5	3,4,6-8,11,12,14,15		16
CD4044A	5	16		3,4,6-8,11,12,14,15	5	3,4,6-8,11,12,14,15		16
CD4045A	16	1,3•		2,14,15	16	2,14,15•		1,3
CD4046A	3,5-8,14	9,11,12,16		10	3,5-9,11,14	16		12
CD4047A	4,8,12	3,5,6,14		7	4,8,12	3,5-7,9		14
CD4048A	10	16	2-9,11-15		10	2-9,11-15	16	
CD4049A	3	1		5,7-9,11,14	3	5,7-9,11,14		1
CD4050A	3	1		5,7-9,11,14	3	5,7-9,11,14		1

• Use 5V for n-channel test, −5V for p-channel test.

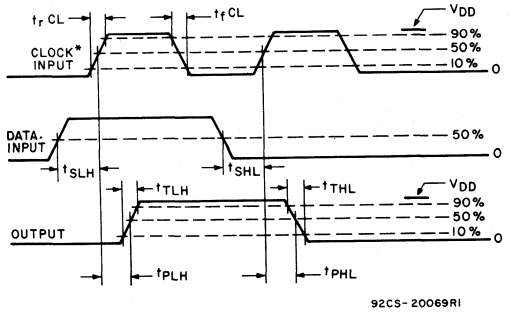
• Use 4V for n-channel test, −4V for p-channel test.

Waveforms for Measurement of Dynamic Characteristics

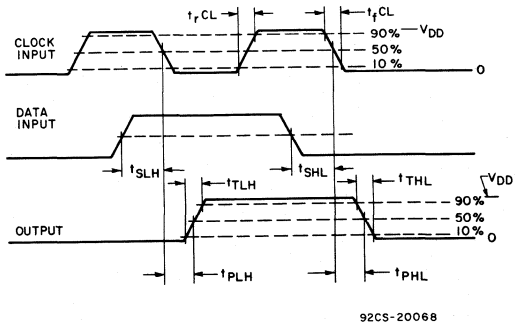




Transition Times and Propagation Delay Times for Combinational Logic Circuits



Set-Up Times, Transition Times, and Propagation Delay Times for Positive Edge Triggered Sequential Logic Circuits

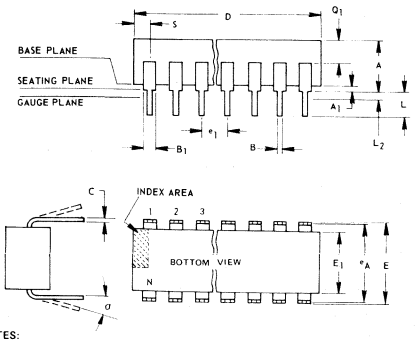


Set-Up Times, Transition Times, and Propagation Delay Times for Negative-Edge-Triggered Sequential Logic Circuits

DIMENSIONAL OUTLINES

Ceramic Dual-in-Line Packages

JEDEC MO-001-AD
14-Lead Welded-Seal



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012		0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411RI

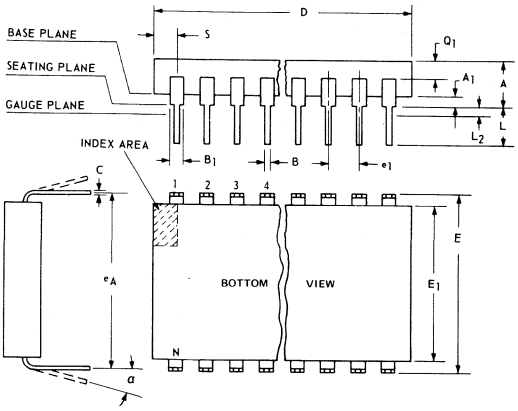
JEDEC MO-001-AE
16-Lead Welded-Seal

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012		0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.300		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R2

NOTES:
1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

JEDEC MO-015-AG
24-Lead Welded-Seal



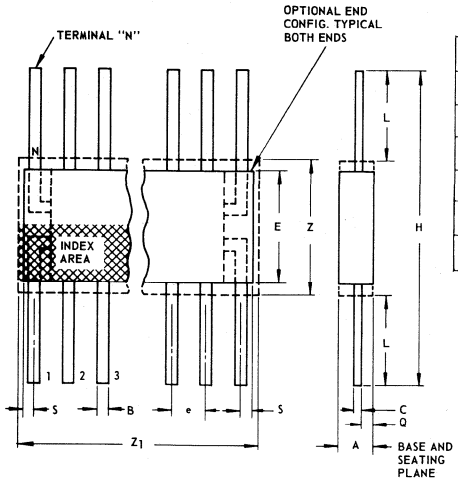
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A_1	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012		0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

92CS-19948

NOTES:
1. REFER TO RULES FOR DIMENSIONING (JEDEC PUBLICATION No. 13) AXIAL LEAD PRODUCT OUTLINES.
2. WHEN BASE OF BODY IS TO BE ATTACHED TO HEAT SINK, TERMINAL LEAD STAND-OFFS ARE NOT REQUIRED AND $A_1 = 0$. WHEN $A_1 = 0$, THE LEADS EMERGE FROM THE BODY WITH THE B_1 DIMENSION AND REDUCE TO THE B DIMENSION ABOVE THE SEATING PLANE.
3. e_1 AND e_A APPLY IN ZONE L_2 WHEN UNIT INSTALLED. LEADS WITHIN .005" RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION.
4. APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
5. N IS THE MAXIMUM QUANTITY OF LEAD POSITIONS.
6. N_1 IS THE QUANTITY OF ALLOWABLE MISSING LEADS.

Flat Packages

JEDEC MO-004-AF 14-LEAD



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300RI

NOTES:
1. Refer to Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

JEDEC MO-004-AG 16-LEAD

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

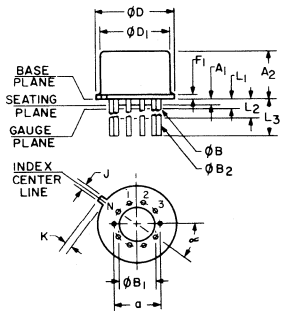
92CS-17271RI

24-LEAD

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-19949

TO-5 STYLE PACKAGE



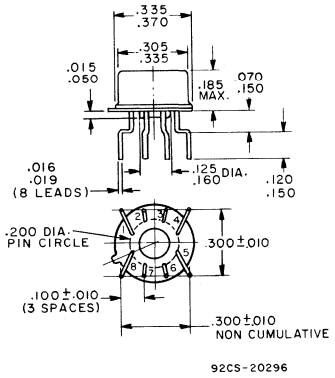
SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
a	0.230 TP		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0	0		0	0
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	36° TP			36° TP	
N	10		6	10	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

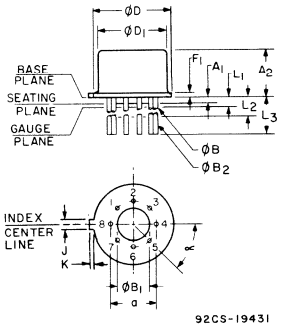
Lead Finish:

In accordance with MIL-M-38510, Paragraph 3.6.2.5, Lead Finish "A".

8-LEAD TO-5 WITH DUAL-IN-LINE DIL-CAN FORMED LEADS



8-LEAD TO-5 JEDEC MO-002-AL

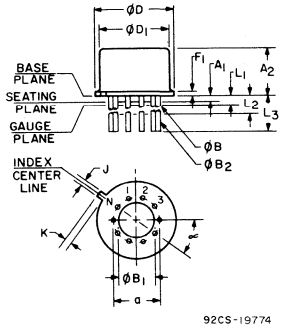


SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
a	0.200 TP		2	5.88 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0.125	0.160		3.18	4.06
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

NOTES

1. Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radium of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2.ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

12-LEAD PACKAGE JEDEC MO-006-AG



SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0	0		0	0
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	30° TP			30° TP	
N	12		6	12	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

Guide to RCA Solid-State Devices

Operating Considerations for RCA Solid State Devices

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

TRANSISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operations to provide some slack or an expansion elbow in each lead, to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

TRANSISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device.

Such devices can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between transistor and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance not less than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic high-power packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

Mounting

Recommended mounting arrangements and suggested hardware for the VERSAWATT transistors are given in the data bulletins for specific devices and in RCA Application Note AN-4124. When the transistor is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the transistor. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphtalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The transistor should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the transistor to become excessively high.

The TO-220AA plastic transistor can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the transistor to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term transistor life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with respect to their component parts, as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the

inner encapsulant to swell and damage the transistor. Alcohol and unchlorinated freons are acceptable solvents. Examples of such solvents are:

1. Freon TE
2. Freon TE-35
3. Freon TP-35 (Freon PC)
4. Alcohol (isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44)

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing packages such as the JEDEC TO-5 and "modified TO-5" is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. These packages can be mounted to the heat sink mechanically with glue or an epoxy adhesive, or by soldering. Soldering to the heat sink is preferable because it is the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. Such an arrangement is illustrated in RCA Publication MHI-300B, "Mounting Hardware Supplied with RCA Semiconductor Devices". If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

INTEGRATED CIRCUITS

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

COS/MOS (Complementary-Symmetry MOS) Integrated Circuits

1. Handling

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces fully protect COS/MOS devices from gate-oxide failure (70 to 100 volt limit) for static discharge or signal voltage up to 1 to 2 kilovolts under most transient or low-current conditions.

Although protection against electrostatic effects is provided by built-in circuitry, the following handling precautions should be taken:

1. Soldering-iron tips and test equipment should be grounded.
2. Devices should not be inserted in non-conductive containers such as conventional plastic snow or trays.

*Trade Mark: Emerson and Cumming, Inc.

2. Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4009A, CD4010A, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 0.2 to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current COS/MOS types, such as the CD4007A, CD4009A, and CD4010A. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC Handling Considerations, refer to Application Note ICAN-6000 "Handling Considerations for MOS Integrated Circuits".

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Subject Index

D

Subject Index

Subject Index

Subject Index

Subject Index

Subject Index

T

Subject Index

Index to Devices

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
1N248C	SSD-206	287	THC-500	6	RECT
1N249C	SSD-206	287	THC-500	6	RECT
1N250C	SSD-206	287	THC-500	6	RECT
1N440B	SSD-206	252	THC-500	5	RECT
1N441B	SSD-206	252	THC-500	5	RECT
1N442B	SSD-206	252	THC-500	5	RECT
1N443B	SSD-206	252	THC-500	5	RECT
1N444B	SSD-206	252	THC-500	5	RECT
1N445B	SSD-206	252	THC-500	5	RECT
1N536	SSD-206	255	THC-500	3	RECT
1N537	SSD-206	255	THC-500	3	RECT
1N538	SSD-206	255	THC-500	3	RECT
1N539	SSD-206	255	THC-500	3	RECT
1N540	SSD-206	255	THC-500	3	RECT
1N547	SSD-206	255	THC-500	3	RECT
1N1095	SSD-206	255	THC-500	3	RECT
1N1183A	SSD-206	291	THC-500	38	RECT
1N1184A	SSD-206	291	THC-500	38	RECT
1N1186A	SSD-206	291	THC-500	38	RECT
1N1187A	SSD-206	291	THC-500	38	RECT
1N1188A	SSD-206	291	THC-500	38	RECT
1N1189A	SSD-206	291	THC-500	38	RECT
1N1190A	SSD-206	291	THC-500	38	RECT
1N1195A	SSD-206	287	THC-500	6	RECT
1N1196A	SSD-206	287	THC-500	6	RECT
1N1197A	SSD-206	287	THC-500	6	RECT
1N1198A	SSD-206	287	THC-500	6	RECT
1N1199A	SSD-206	283	THC-500	20	RECT
1N1200A	SSD-206	283	THC-500	20	RECT
1N1202A	SSD-206	283	THC-500	20	RECT
1N1203A	SSD-206	283	THC-500	20	RECT
1N1204A	SSD-206	283	THC-500	20	RECT
1N1205A	SSD-206	283	THC-500	20	RECT
1N1206A	SSD-206	283	THC-500	20	RECT
1N1341B	SSD-206	281	THC-500	58	RECT
1N1342B	SSD-206	281	THC-500	58	RECT
1N1344B	SSD-206	281	THC-500	58	RECT
1N1345B	SSD-206	281	THC-500	58	RECT
1N1346B	SSD-206	281	THC-500	58	RECT
1N1347B	SSD-206	281	THC-500	58	RECT
1N1348B	SSD-206	281	THC-500	58	RECT
1N1763A	SSD-206	258	THC-500	89	RECT
1N1764A	SSD-206	258	THC-500	89	RECT
1N2858A	SSD-206	265	THC-500	91	RECT
1N2859A	SSD-206	265	THC-500	91	RECT
1N2860A	SSD-206	265	THC-500	91	RECT
1N2861A	SSD-206	265	THC-500	91	RECT
1N2862A	SSD-206	265	THC-500	91	RECT
1N2863A	SSD-206	265	THC-500	91	RECT
1N2864A	SSD-206	265	THC-500	91	RECT
1N3193	SSD-206	294	THC-500	41	RECT
1N3194	SSD-206	294	THC-500	41	RECT
1N3195	SSD-206	294	THC-500	41	RECT
1N3196	SSD-206	294	THC-500	41	RECT
1N3253	SSD-206	294	THC-500	41	RECT
1N3254	SSD-206	294	THC-500	41	RECT
1N3255	SSD-206	294	THC-500	41	RECT
1N3256	SSD-206	294	THC-500	41	RECT
1N3563	SSD-206	294	THC-500	41	RECT
1N3879	SSD-206	323	THC-500	726	RECT
1N3880	SSD-206	323	THC-500	726	RECT
1N3881	SSD-206	323	THC-500	726	RECT
1N3882	SSD-206	323	THC-500	726	RECT
1N3883	SSD-206	323	THC-500	726	RECT
1N3889	SSD-206	331	THC-500	727	RECT
1N3890	SSD-206	331	THC-500	727	RECT
1N3891	SSD-206	331	THC-500	727	RECT
1N3892	SSD-206	331	THC-500	727	RECT
1N3893	SSD-206	331	THC-500	727	RECT
1N3899	SSD-206	339	THC-500	728	RECT
1N3900	SSD-206	339	THC-500	728	RECT
1N3901	SSD-206	339	THC-500	728	RECT
1N3902	SSD-206	339	THC-500	728	RECT
1N3903	SSD-206	339	THC-500	728	RECT
1N3909	SSD-206	342	THC-500	729	RECT
1N3910	SSD-206	342	THC-500	729	RECT
1N3911	SSD-206	342	THC-500	729	RECT
1N3912	SSD-206	342	THC-500	729	RECT
1N3913	SSD-206	342	THC-500	729	RECT
1N5211	SSD-206	270	THC-500	245	RECT
1N5212	SSD-206	270	THC-500	245	RECT
1N5213	SSD-206	270	THC-500	245	RECT
1N5214	SSD-206	270	THC-500	245	RECT
1N5215	SSD-206	270	THC-500	245	RECT
1N5216	SSD-206	270	THC-500	245	RECT
1N5217	SSD-206	270	THC-500	245	RECT
1N5218	SSD-206	270	THC-500	245	RECT
1N5391	SSD-206	273	THC-500	478	RECT
1N5392	SSD-206	273	THC-500	478	RECT
1N5393	SSD-206	273	THC-500	478	RECT
1N5394	SSD-206	273	THC-500	478	RECT
1N5395	SSD-206	273	THC-500	478	RECT
1N5396	SSD-206	273	THC-500	478	RECT
1N5397	SSD-206	273	THC-500	478	RECT
1N5398	SSD-206	273	THC-500	478	RECT
1N5399	SSD-206	273	THC-500	478	RECT
2N681	SSD-206	225	THC-500	96	SCR
2N682	SSD-206	225	THC-500	96	SCR
2N683	SSD-206	225	THC-500	96	SCR
2N684	SSD-206	225	THC-500	96	SCR
2N685	SSD-206	225	THC-500	96	SCR
2N686	SSD-206	225	THC-500	96	SCR
2N687	SSD-206	225	THC-500	96	SCR
2N688	SSD-206	225	THC-500	96	SCR
2N689	SSD-206	225	THC-500	96	SCR
2N690	SSD-206	225	THC-500	96	SCR
2N697	SSD-204	493	PTD-187	16	PWR
2N699	SSD-204	495	PTD-187	22	PWR
2N918	SSD-204	692	RFT-700	83	RF
2N918	SSD-205	20	RFT-700	83	RF
2N1491	SSD-205	24	RFT-700	10	RF
2N1492	SSD-205	24	RFT-700	10	RF
2N1493	SSD-205	24	RFT-700	10	RF
2N1613	SSD-204	498	PTD-187	106	PWR
2N1711	SSD-204	503	PTD-187	26	PWR
2N1842A	SSD-206	234	THC-500	28	SCR
2N1843A	SSD-206	234	THC-500	28	SCR
2N1844A	SSD-206	234	THC-500	28	SCR
2N1845A	SSD-206	234	THC-500	28	SCR
2N1846A	SSD-206	234	THC-500	28	SCR
2N1847A	SSD-206	234	THC-500	28	SCR
2N1848A	SSD-206	234	THC-500	28	SCR
2N1849A	SSD-206	234	THC-500	28	SCR
2N1850A	SSD-206	234	THC-500	28	SCR
2N1893	SSD-204	507	PTD-187	34	PWR
2N2102	SSD-204	498	PTD-187	106	PWR
2N2102	SSD-207	34	–	–	PWR
2N2270	SSD-204	513	PTD-187	24	PWR
2N2405	SSD-204	507	PTD-187	34	PWR
2N2631	SSD-205	28	RFT-700	32	RF
2N2857	SSD-204	714	RFT-700	61	RF
2N2857	SSD-205	33	RFT-700	61	RF
2N2876	SSD-205	28	RFT-700	32	RF
2N2895	SSD-204	517	PTD-187	143	PWR
2N2896	SSD-204	517	PTD-187	143	PWR
2N2897	SSD-204	517	PTD-187	143	PWR
2N3053	SSD-204	404	PTD-187	432	PWR
2N3054	SSD-204	45	PTD-187	527	PWR
2N3054	SSD-207	34	–	–	PWR
2N3055	SSD-204	102	PTD-187	524	PWR
2N3118	SSD-205	37	RFT-700	42	RF
2N3119	SSD-205	41	RFT-700	44	RF
2N3228	SSD-206	144	THC-500	114	SCR
2N3229	SSD-205	45	RFT-700	50	RF
2N3262	SSD-205	48	RFT-700	56	RF
2N3263	SSD-204	475	PTD-187	54	PWR
2N3263	SSD-207	35	–	–	PWR
2N3264	SSD-204	475	PTD-187	54	PWR
2N3265	SSD-204	475	PTD-187	54	PWR
2N3266	SSD-204	475	PTD-187	54	PWR
2N3375	SSD-205	52	RFT-700	386	RF
2N3439	SSD-204	286	PTD-187	64	PWR
2N3440	SSD-204	286	PTD-187	64	PWR
2N3441	SSD-204	69	PTD-187	529	PWR
2N3442	SSD-204	133	PTD-187	528	PWR
2N3478	SSD-204	696	RFT-700	77	RF
2N3478	SSD-205	60	RFT-700	77	RF
2N3525	SSD-206	144	THC-500	114	SCR
2N3528	SSD-206	144	THC-500	114	SCR
2N3529	SSD-206	144	THC-500	114	SCR

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
2N3553	SSD-205	52	RFT-700	386	RF
2N3583	SSD-204	304	PTD-187	138	PWR
2N3584	SSD-204	304	PTD-187	138	PWR
2N3585	SSD-204	304	PTD-187	138	PWR
2N3600	SSD-204	692	RFT-700	83	RF
2N3600	SSD-205	20	RFT-700	83	RF
2N3632	SSD-205	52	RFT-700	386	RF
2N3650	SSD-206	238	THC-500	408	SCR
2N3651	SSD-206	238	THC-500	408	SCR
2N3652	SSD-206	238	THC-500	408	SCR
2N3653	SSD-206	238	THC-500	408	SCR
2N3654	SSD-206	245	THC-500	724	SCR
2N3655	SSD-206	245	THC-500	724	SCR
2N3656	SSD-206	245	THC-500	724	SCR
2N3657	SSD-206	245	THC-500	724	SCR
2N3658	SSD-206	245	THC-500	724	SCR
2N3668	SSD-206	203	THC-500	116	SCR
2N3669	SSD-206	203	THC-500	116	SCR
2N3670	SSD-206	203	THC-500	116	SCR
2N3733	SSD-205	64	RFT-700	72	RF
2N3771	SSD-204	141	PTD-187	525	PWR
2N3772	SSD-204	141	PTD-187	525	PWR
2N3773	SSD-204	149	PTD-187	526	PWR
2N3773	SSD-207	36	–	–	PWR
2N3839	SSD-204	718	RFT-700	229	RF
2N3839	SSD-205	69	RFT-700	229	RF
2N3866	SSD-205	73	RFT-700	80	RF
2N3870	SSD-206	218	THC-500	578	SCR
2N3871	SSD-206	218	THC-500	578	SCR
2N3872	SSD-206	218	THC-500	578	SCR
2N3873	SSD-206	218	THC-500	578	SCR
2N3878	SSD-204	443	PTD-187	299	PWR
2N3879	SSD-204	443	PTD-187	299	PWR
2N3879	SSD-207	36	–	–	PWR
2N3896	SSD-206	218	THC-500	578	SCR
2N3897	SSD-206	218	THC-500	578	SCR
2N3898	SSD-206	218	THC-500	578	SCR
2N3899	SSD-206	218	THC-500	578	SCR
2N4012	SSD-205	77	RFT-700	90	RF
2N4036	SSD-204	410	PTD-187	216	PWR
2N4036	SSD-207	37	–	–	PWR
2N4037	SSD-204	410	PTD-187	216	PWR
2N4063	SSD-204	286	PTD-187	64	PWR
2N4064	SSD-204	286	PTD-187	64	PWR
2N4101	SSD-206	144	THC-500	114	SCR
2N4102	SSD-206	144	THC-500	114	SCR
2N4103	SSD-206	203	THC-500	116	SCR
2N4240	SSD-204	304	PTD-187	135	PWR
2N4314	SSD-204	410	PTD-187	216	PWR
2N4347	SSD-204	133	PTD-187	528	PWR
2N4348	SSD-204	149	PTD-187	526	PWR
2N4427	SSD-205	81	RFT-700	228	RF
2N4440	SSD-205	87	RFT-700	217	RF
2N4932	SSD-205	92	RFT-700	249	RF
2N4933	SSD-205	92	RFT-700	249	RF
2N5016	SSD-205	96	RFT-700	255	RF
2N5038	SSD-204	461	PTD-187	698	PWR
2N5039	SSD-204	461	PTD-187	698	PWR
2N5070	SSD-205	100	RFT-700	268	RF
2N5071	SSD-205	105	RFT-700	269	RF
2N5090	SSD-205	109	RFT-700	270	RF
2N5102	SSD-205	113	RFT-700	279	RF
2N5109	SSD-204	722	RFT-700	281	RF
2N5109	SSD-205	118	RFT-700	281	RF
2N5179	SSD-204	700	RFT-700	288	RF
2N5179	SSD-205	124	RFT-700	288	RF
2N5180	SSD-205	130	RFT-700	289	RF
2N5189	SSD-204	418	PTD-187	296	PWR
2N5202	SSD-204	443	PTD-187	299	PWR
2N5239	SSD-204	373	PTD-187	321	PWR
2N5240	SSD-204	373	PTD-187	321	PWR
2N5240	SSD-207	37	–	–	PWR
2N5262	SSD-204	423	PTD-187	313	RF
2N5262	SSD-205	134	PTD-187	313	RF
2N5262	SSD-207	38	–	–	RF
2N5293	SSD-204	61	PTD-187	322	PWR
2N5294	SSD-204	61	PTD-187	322	PWR
2N5295	SSD-204	61	PTD-187	322	PWR
2N5296	SSD-204	61	PTD-187	322	PWR
2N5297	SSD-204	61	PTD-187	322	PWR
2N5298	SSD-204	61	PTD-187	322	PWR
2N5320	SSD-204	429	PTD-187	325	PWR
2N5320	SSD-207	38	–	–	PWR
2N5321	SSD-204	429	PTD-187	325	PWR
2N5322	SSD-204	429	PTD-187	325	PWR
2N5322	SSD-207	39	–	–	PWR
2N5323	SSD-204	429	PTD-187	325	PWR
2N5415	SSD-204	292	PTD-187	336	PWR
2N5416	SSD-204	292	PTD-187	336	PWR
2N5441	SSD-206	55	THC-500	593	TRI
2N5442	SSD-206	55	THC-500	593	TRI
2N5443	SSD-206	55	THC-500	593	TRI
2N5444	SSD-206	55	THC-500	593	TRI
2N5445	SSD-206	55	THC-500	593	TRI
2N5446	SSD-206	55	THC-500	593	TRI
2N5470	SSD-205	140	RFT-700	350	RF
2N5490	SSD-204	90	PTD-187	353	PWR
2N5491	SSD-204	90	PTD-187	353	PWR
2N5492	SSD-204	90	PTD-187	353	PWR
2N5493	SSD-204	90	PTD-187	353	PWR
2N5494	SSD-204	90	PTD-187	353	PWR
2N5495	SSD-204	90	PTD-187	353	PWR
2N5496	SSD-204	90	PTD-187	353	PWR
2N5497	SSD-204	90	PTD-187	353	PWR
2N5567	SSD-206	92	THC-500	457	TRI
2N5568	SSD-206	92	THC-500	457	TRI
2N5569	SSD-206	92	THC-500	457	TRI
2N5570	SSD-206	92	THC-500	457	TRI
2N5571	SSD-206	85	THC-500	458	TRI
2N5572	SSD-206	85	THC-500	458	TRI
2N5573	SSD-206	85	THC-500	458	TRI
2N5574	SSD-206	85	THC-500	458	TRI
2N5575	SSD-204	162	PTD-187	359	PWR
2N5578	SSD-204	162	PTD-187	359	PWR
2N5578	SSD-207	39	–	–	PWR
2N5671	SSD-204	481	PTD-187	383	PWR
2N5672	SSD-204	481	PTD-187	383	PWR
2N5754	SSD-206	28	THC-500	414	TRI
2N5755	SSD-206	28	THC-500	414	TRI
2N5756	SSD-206	28	THC-500	414	TRI
2N5757	SSD-206	28	THC-500	414	TRI
2N5781	SSD-204	34	PTD-187	413	PWR
2N5781	SSD-207	40	–	–	PWR
2N5782	SSD-204	34	PTD-187	413	PWR
2N5783	SSD-204	34	PTD-187	413	PWR
2N5784	SSD-204	34	PTD-187	413	PWR
2N5784	SSD-207	40	–	–	PWR
2N5785	SSD-204	34	PTD-187	413	PWR
2N5786	SSD-204	34	PTD-187	413	PWR
2N5804	SSD-204	379	PTD-187	407	PWR
2N5805	SSD-204	379	PTD-187	407	PWR
2N5838	SSD-204	356	PTD-187	410	PWR
2N5839	SSD-204	356	PTD-187	410	PWR
2N5840	SSD-204	356	PTD-187	410	PWR
2N5913	SSD-205	146	RFT-700	423	RF
2N5914	SSD-205	152	RFT-700	424	RF
2N5915	SSD-205	152	RFT-700	424	RF
2N5916	SSD-205	158	RFT-700	425	RF
2N5917	SSD-205	158	RFT-700	425	RF
2N5918	SSD-205	164	RFT-700	448	RF
2N5919A	SSD-205	169	RFT-700	505	RF
2N5920	SSD-205	175	RFT-700	440	RF
2N5921	SSD-205	181	RFT-700	427	RF
2N5954	SSD-204	170	PTD-187	675	PWR
2N5954	SSD-207	41	–	–	PWR
2N5955	SSD-204	170	PTD-187	675	PWR
2N5956	SSD-204	170	PTD-187	675	PWR
2N5992	SSD-205	189	RFT-700	451	RF
2N5993	SSD-205	194	RFT-700	452	RF
2N5994	SSD-205	199	RFT-700	453	RF
2N5995	SSD-205	205	RFT-700	454	RF
2N5996	SSD-205	210	RFT-700	455	RF
2N6032	SSD-204	487	PTD-187	462	PWR
2N6033	SSD-204	487	PTD-187	462	PWR
2N6033	SSD-207	41	–	–	PWR
2N6055	SSD-204	527	PTD-187	563	PWR
2N6056	SSD-204	527	PTD-187	563	PWR
2N6056	SSD-207	42	–	–	PWR
2N6077	SSD-204	318	PTD-187	492	PWR
2N6078	SSD-204	318	PTD-187	492	PWR

Index to Devices

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
2N6079	SSD-204	318	PTD-187	492	PWR
2N6079	SSD-207	42	–	–	PWR
2N6093	SSD-205	216	RFT-700	484	RF
2N6098	SSD-204	121	PTD-187	485	PWR
2N6099	SSD-204	121	PTD-187	485	PWR
2N6100	SSD-204	121	PTD-187	485	PWR
2N6101	SSD-204	121	PTD-187	485	PWR
2N6102	SSD-204	121	PTD-187	485	PWR
2N6103	SSD-204	121	PTD-187	485	PWR
2N6104	SSD-205	221	RFT-700	504	RF
2N6105	SSD-205	221	RFT-700	504	RF
2N6106	SSD-204	177	PTD-187	676	PWR
2N6107	SSD-204	177	PTD-187	676	PWR
2N6108	SSD-204	177	PTD-187	676	PWR
2N6109	SSD-204	177	PTD-187	676	PWR
2N6110	SSD-204	177	PTD-187	676	PWR
2N6111	SSD-204	177	PTD-187	676	PWR
2N6175	SSD-204	278	PTD-187	508	PWR
2N6176	SSD-204	278	PTD-187	508	PWR
2N6177	SSD-204	278	PTD-187	508	PWR
2N6178	SSD-204	435	PTD-187	562	PWR
2N6179	SSD-204	435	PTD-187	562	PWR
2N6180	SSD-204	435	PTD-187	562	PWR
2N6181	SSD-204	435	PTD-187	562	PWR
2N6211	SSD-204	312	PTD-187	507	PWR
2N6212	SSD-204	312	PTD-187	507	PWR
2N6213	SSD-204	312	PTD-187	507	PWR
2N6214	SSD-204	312	PTD-187	507	PWR
2N6246	SSD-204	217	PTD-187	677	PWR
2N6247	SSD-204	217	PTD-187	677	PWR
2N6248	SSD-204	217	PTD-187	677	PWR
2N6248	SSD-207	43	–	–	PWR
2N6249	SSD-204	385	PTD-187	523	PWR
2N6250	SSD-204	385	PTD-187	523	PWR
2N6251	SSD-204	385	PTD-187	523	PWR
2N6251	SSD-207	43	–	–	PWR
2N6253	SSD-204	102	PTD-187	524	PWR
2N6254	SSD-204	102	PTD-187	524	PWR
2N6257	SSD-204	141	PTD-187	525	PWR
2N6258	SSD-204	141	PTD-187	525	PWR
2N6259	SSD-204	149	PTD-187	526	PWR
2N6260	SSD-204	45	PTD-187	527	PWR
2N6261	SSD-204	45	PTD-187	527	PWR
2N6262	SSD-204	133	PTD-187	528	PWR
2N6263	SSD-204	69	PTD-187	529	PWR
2N6264	SSD-204	69	PTD-187	529	PWR
2N6265	SSD-205	228	RFT-700	543	RF
2N6266	SSD-205	234	RFT-700	544	RF
2N6267	SSD-205	240	RFT-700	545	RF
2N6268	SSD-205	246	RFT-700	546	RF
2N6269	SSD-205	246	RFT-700	546	RF
2N6288	SSD-204	177	PTD-187	676	PWR
2N6289	SSD-204	177	PTD-187	676	PWR
2N6290	SSD-204	177	PTD-187	676	PWR
2N6291	SSD-204	177	PTD-187	676	PWR
2N6292	SSD-204	177	PTD-187	676	PWR
2N6293	SSD-204	177	PTD-187	676	PWR
2N6354	SSD-204	149	PTD-187	582	PWR
2N6371	SSD-204	97	PTD-187	607	PWR
2N6372	SSD-204	170	PTD-187	675	PWR
2N6373	SSD-204	170	PTD-187	675	PWR
2N6374	SSD-204	170	PTD-187	675	PWR
2N6383	SSD-204	532	PTD-187	609	PWR
2N6384	SSD-204	532	PTD-187	609	PWR
2N6385	SSD-204	532	PTD-187	609	PWR
2N6385	SSD-207	44	–	–	PWR
2N6386	SSD-204	538	PTD-187	610	PWR
2N6387	SSD-204	538	PTD-187	610	PWR
2N6388	SSD-204	538	PTD-187	610	PWR
2N6389	SSD-204	732	RFT-700	617	RF
2N6389	SSD-205	257	RFT-700	617	RF
2N6390	SSD-205	261	RFT-700	626	RF
2N6391	SSD-205	265	RFT-700	627	RF
2N6392	SSD-205	270	RFT-700	628	RF
2N6393	SSD-205	270	RFT-700	628	RF
2N6467	SSD-204	170	PTD-187	675	PWR
2N6468	SSD-204	170	PTD-187	675	PWR
2N6469	SSD-204	217	PTD-187	677	PWR
2N6470	SSD-204	217	PTD-187	677	PWR
2N6471	SSD-204	217	PTD-187	677	PWR
2N6472	SSD-204	217	PTD-187	677	PWR
2N6473	SSD-204	177	PTD-187	676	PWR
2N6474	SSD-204	177	PTD-187	676	PWR
2N6475	SSD-204	177	PTD-187	676	PWR
2N6476	SSD-204	177	PTD-187	676	PWR
2N6477	SSD-204	83	PTD-187	680	PWR
2N6478	SSD-204	83	PTD-187	680	PWR
2N6479	SSD-204	454	PTD-187	702	PWR
2N6479	SSD-207	45	–	–	PWR
2N6480	SSD-204	454	PTD-187	702	PWR
2N6480	SSD-207	45	–	–	PWR
2N6481	SSD-204	454	PTD-187	702	PWR
2N6481	SSD-207	45	–	–	PWR
2N6482	SSD-204	454	PTD-187	702	PWR
2N6482	SSD-207	45	–	–	PWR
2N6486	SSD-204	226	PTD-187	678	PWR
2N6487	SSD-204	226	PTD-187	678	PWR
2N6488	SSD-204	226	PTD-187	678	PWR
2N6489	SSD-204	226	PTD-187	678	PWR
2N6490	SSD-204	226	PTD-187	678	PWR
2N6491	SSD-204	226	PTD-187	678	PWR
2N6496	SSD-204	461	PTD-187	698	PWR
3N128	SSD-201	634	MOS-160	309	MOS/FET
3N138	SSD-201	639	MOS-160	283	MOS/FET
3N139	SSD-201	643	MOS-160	284	MOS/FET
3N140	SSD-201	667	MOS-160	285	MOS/FET
3N141	SSD-201	667	MOS-160	285	MOS/FET
3N142	SSD-201	648	MOS-160	286	MOS/FET
3N143	SSD-201	634	MOS-160	309	MOS/FET
3N152	SSD-201	654	MOS-160	314	MOS/FET
3N153	SSD-201	659	MOS-160	320	MOS/FET
3N154	SSD-201	662	MOS-160	335	MOS/FET
3N159	SSD-201	675	MOS-160	326	MOS/FET
3N187	SSD-201	690	MOS-160	436	MOS/FET
3N200	SSD-201	698	MOS-160	437	MOS/FET
40080	SSD-205	275	RFT-700	301	RF
40081	SSD-205	275	RFT-700	301	RF
40082	SSD-205	275	RFT-700	301	RF
40279	SSD-207	119	RFT-700	46	RF
40280	SSD-205	279	RFT-700	68	RF
40281	SSD-205	279	RFT-700	68	RF
40282	SSD-205	279	RFT-700	68	RF
40290	SSD-205	283	RFT-700	70	RF
40291	SSD-205	283	RFT-700	70	RF
40292	SSD-205	283	RFT-700	70	RF
40294	SSD-207	123	RFT-700	202	RF
40296	SSD-207	130	RFT-700	603	RF
40305	SSD-207	137	RFT-700	144	RF
40306	SSD-207	137	RFT-700	144	RF
40307	SSD-207	137	RFT-700	144	RF
40309	SSD-204	655	PTD-187	78	PWR
40310	SSD-204	655	PTD-187	78	PWR
40311	SSD-204	655	PTD-187	78	PWR
40312	SSD-204	655	PTD-187	78	PWR
40313	SSD-204	655	PTD-187	78	PWR
40314	SSD-204	655	PTD-187	78	PWR
40315	SSD-204	655	PTD-187	78	PWR
40316	SSD-204	655	PTD-187	78	PWR
40317	SSD-204	655	PTD-187	78	PWR
40318	SSD-204	655	PTD-187	78	PWR
40319	SSD-204	655	PTD-187	78	PWR
40320	SSD-204	655	PTD-187	78	PWR
40321	SSD-204	655	PTD-187	78	PWR
40322	SSD-204	655	PTD-187	78	PWR
40323	SSD-204	655	PTD-187	78	PWR
40324	SSD-204	655	PTD-187	78	PWR
40325	SSD-204	655	PTD-187	78	PWR
40326	SSD-204	655	PTD-187	78	PWR
40327	SSD-204	655	PTD-187	78	PWR
40328	SSD-204	655	PTD-187	78	PWR
40340	SSD-205	287	RFT-700	74	RF
40341	SSD-205	287	RFT-700	74	RF
40346	SSD-204	393	PTD-187	211	PWR
40346V1	SSD-204	393	PTD-187	211	PWR
40346V2	SSD-204	393	PTD-187	211	PWR
40347	SSD-204	26	PTD-187	88	PWR
40347V1	SSD-204	26	PTD-187	88	PWR
40347V2	SSD-204	26	PTD-187	88	PWR
40348	SSD-204	26	PTD-187	88	PWR
40348V1	SSD-204	26	PTD-187	88	PWR

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
40348V2	SSD-204	26	PTD-187	88	PWR
40349	SSD-204	26	PTD-187	88	PWR
40349V1	SSD-204	26	PTD-187	88	PWR
40349V2	SSD-204	26	PTD-187	88	PWR
40360	SSD-204	655	PTD-187	78	PWR
40361	SSD-204	655	PTD-187	78	PWR
40362	SSD-204	655	PTD-187	78	PWR
40363	SSD-204	655	PTD-187	78	PWR
40364	SSD-204	655	PTD-187	78	PWR
40366	SSD-204	397	PTD-187	215	PWR
40367	SSD-204	397	PTD-187	215	PWR
40368	SSD-204	397	PTD-187	215	PWR
40369	SSD-204	397	PTD-187	215	PWR
40372	SSD-204	45	PTD-187	527	PWR
40373	SSD-204	69	PTD-187	529	PWR
40374	SSD-204	304	PTD-187	128	PWR
40375	SSD-204	443	PTD-187	299	PWR
40385	SSD-204	397	PTD-187	215	PWR
40389	SSD-204	404	PTD-187	432	PWR
40390	SSD-204	286	PTD-187	64	PWR
40391	SSD-204	410	PTD-187	216	PWR
40392	SSD-204	404	PTD-187	432	PWR
40394	SSD-204	410	PTD-187	216	PWR
40406	SSD-204	661	PTD-187	219	PWR
40407	SSD-204	661	PTD-187	219	PWR
40408	SSD-204	661	PTD-187	219	PWR
40409	SSD-204	661	PTD-187	219	PWR
40410	SSD-204	661	PTD-187	219	PWR
40411	SSD-204	661	PTD-187	219	PWR
40412	SSD-204	393	PTD-187	211	PWR
40412V1	SSD-204	393	PTD-187	211	PWR
40412V2	SSD-204	393	PTD-187	211	PWR
40414	SSD-207	142	RFT-700	259	RF
40446	SSD-205	275	RFT-700	301	RF
40467A	SSD-201	681	MOS-160	324	MOS/FET
40468A	SSD-201	686	MOS-160	323	MOS/FET
40537	SSD-204	668	PTD-187	320	PWR
40538	SSD-204	668	PTD-187	320	PWR
40539	SSD-204	671	PTD-187	303	PWR
40542	SSD-204	675	PTD-187	304	PWR
40543	SSD-204	675	PTD-187	304	PWR
40544	SSD-204	671	PTD-187	303	PWR
40559A	SSD-201	686	MOS-160	323	MOS/FET
40577	SSD-207	148	RFT-700	297	RF
40578	SSD-207	155	RFT-700	298	RF
40581	SSD-205	275	RFT-700	301	RF
40582	SSD-205	275	RFT-700	301	RF
40594	SSD-204	681	PTD-187	358	PWR
40595	SSD-204	681	PTD-187	358	PWR
40600	SSD-201	712	MOS-160	333	MOS/FET
40601	SSD-201	712	MOS-160	333	MOS/FET
40602	SSD-201	712	MOS-160	333	MOS/FET
40603	SSD-201	720	MOS-160	334	MOS/FET
40604	SSD-201	720	MOS-160	334	MOS/FET
40605	SSD-207	161	RFT-700	389	RF
40606	SSD-207	168	RFT-700	600	RF
40608	SSD-204	728	RFT-700	356	RF
40608	SSD-205	291	RFT-700	356	RF
40611	SSD-204	681	PTD-187	358	PWR
40613	SSD-204	681	PTD-187	358	PWR
40616	SSD-204	681	PTD-187	358	PWR
40618	SSD-204	681	PTD-187	358	PWR
40621	SSD-204	681	PTD-187	358	PWR
40622	SSD-204	681	PTD-187	358	PWR
40624	SSD-204	681	PTD-187	358	PWR
40625	SSD-204	681	PTD-187	358	PWR
40627	SSD-204	681	PTD-187	358	PWR
40628	SSD-204	681	PTD-187	358	PWR
40629	SSD-204	681	PTD-187	358	PWR
40630	SSD-204	681	PTD-187	358	PWR
40631	SSD-204	681	PTD-187	358	PWR
40632	SSD-204	681	PTD-187	358	PWR
40633	SSD-204	681	PTD-187	358	PWR
40634	SSD-204	681	PTD-187	358	PWR
40635	SSD-204	681	PTD-187	358	PWR
40636	SSD-204	681	PTD-187	358	PWR
40637A	SSD-205	295	RFT-700	655	RF
40665	SSD-205	52	RFT-700	386	RF
40666	SSD-205	52	RFT-700	386	RF
40673	SSD-201	745	MOS-160	381	MOS/FET
40819	SSD-201	704	MOS-160	463	MOS/FET
40820	SSD-201	724	MOS-160	464	MOS/FET
40821	SSD-201	724	MOS-160	464	MOS/FET
40822	SSD-201	732	MOS-160	465	MOS/FET
40823	SSD-201	732	MOS-160	465	MOS/FET
40829	SSD-204	170	PTD-187	675	PWR
40830	SSD-204	170	PTD-187	675	PWR
40831	SSD-204	170	PTD-187	675	PWR
40836	SSD-205	298	RFT-700	497	RF
40837	SSD-205	298	RFT-700	497	RF
40841	SSD-201	739	MOS-160	489	MOS/FET
40850	SSD-204	368	PTD-187	498	PWR
40851	SSD-204	368	PTD-187	498	PWR
40852	SSD-204	368	PTD-187	498	PWR
40853	SSD-204	368	PTD-187	498	PWR
40854	SSD-204	368	PTD-187	498	PWR
40871	SSD-204	685	PTD-187	699	PWR
40872	SSD-204	685	PTD-187	699	PWR
40873	SSD-204	685	PTD-187	699	PWR
40874	SSD-204	685	PTD-187	699	PWR
40875	SSD-204	685	PTD-187	699	PWR
40876	SSD-204	685	PTD-187	699	PWR
40885	SSD-204	278	PTD-187	508	PWR
40886	SSD-204	278	PTD-187	508	PWR
40887	SSD-204	278	PTD-187	508	PWR
40893	SSD-205	304	RFT-700	514	RF
40894	SSD-204	706	RFT-700	548	RF
40894	SSD-205	309	RFT-700	548	RF
40895	SSD-204	706	RFT-700	548	RF
40895	SSD-205	309	RFT-700	548	RF
40896	SSD-204	706	RFT-700	548	RF
40896	SSD-205	309	RFT-700	548	RF
40897	SSD-204	706	RFT-700	548	RF
40897	SSD-205	309	RFT-700	548	RF
40898	SSD-205	313	RFT-700	538	RF
40899	SSD-205	313	RFT-700	538	RF
40909	SSD-205	321	RFT-700	547	RF
40910	SSD-204	45	PTD-187	527	PWR
40911	SSD-204	45	PTD-187	527	PWR
40912	SSD-204	69	PTD-187	529	PWR
40913	SSD-204	69	PTD-187	529	PWR
40915	SSD-204	710	RFT-700	574	RF
40915	SSD-205	325	RFT-700	574	RF
40934	SSD-205	329	RFT-700	550	RF
40936	SSD-205	333	RFT-700	551	RF
40940	SSD-205	337	RFT-700	553	RF
40941	SSD-205	342	RFT-700	554	RF
40953	SSD-205	346	RFT-700	579	RF
40954	SSD-205	346	RFT-700	579	RF
40955	SSD-205	346	RFT-700	579	RF
40964	SSD-205	351	RFT-700	581	RF
40965	SSD-205	351	RFT-700	581	RF
40967	SSD-205	355	RFT-700	596	RF
40968	SSD-205	355	RFT-700	596	RF
40970	SSD-205	359	RFT-700	656	RF
40971	SSD-205	359	RFT-700	656	RF
40972	SSD-205	365	RFT-700	597	RF
40973	SSD-205	365	RFT-700	597	RF
40974	SSD-205	365	RFT-700	597	RF
40975	SSD-205	369	RFT-700	606	RF
40976	SSD-205	369	RFT-700	606	RF
40977	SSD-205	369	RFT-700	606	RF
41008	SSD-205	373	RFT-700	616	RF
41008A	SSD-205	373	RFT-700	616	RF
41009	SSD-205	373	RFT-700	616	RF
41009A	SSD-205	373	RFT-700	616	RF
41010	SSD-205	373	RFT-700	616	RF
41024	SSD-205	379	RFT-700	658	RF
41025	SSD-205	383	RFT-700	641	RF
41026	SSD-205	383	RFT-700	641	RF
41027	SSD-205	390	RFT-700	640	RF
41028	SSD-205	390	RFT-700	640	RF
41038	SSD-205	397	RFT-700	679	RF
41508	SSD-204	157	PTD-187	622	PWR
45190	SSD-204	273	PTD-187	559	PWR
45191	SSD-204	273	PTD-187	559	PWR
45192	SSD-204	273	PTD-187	559	PWR
45193	SSD-204	273	PTD-187	559	PWR
45194	SSD-204	273	PTD-187	559	PWR
45195	SSD-204	273	PTD-187	559	PWR

Index to Devices

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
BD142	SSD-204	110	–	701	PWR
BD181	SSD-204	115	–	700	PWR
BD182	SSD-204	115	–	700	PWR
BD183	SSD-204	115	–	700	PWR
BD239	SSD-204	193	–	669	PWR
BD239A	SSD-204	193	–	669	PWR
BD239B	SSD-204	193	–	669	PWR
BD239C	SSD-204	193	–	669	PWR
BD240	SSD-204	197	–	670	PWR
BD240A	SSD-204	197	–	670	PWR
BD240B	SSD-204	197	–	670	PWR
BD240C	SSD-204	197	–	670	PWR
BD241	SSD-204	201	–	671	PWR
BD241A	SSD-204	201	–	671	PWR
BD241B	SSD-204	201	–	671	PWR
BD241C	SSD-204	201	–	671	PWR
BD242	SSD-204	205	–	672	PWR
BD242A	SSD-204	205	–	672	PWR
BD242B	SSD-204	205	–	672	PWR
BD242C	SSD-204	205	–	672	PWR
BD243	SSD-204	209	–	673	PWR
BD243A	SSD-204	209	–	673	PWR
BD243B	SSD-204	209	–	673	PWR
BD243C	SSD-204	209	–	673	PWR
BD244	SSD-204	213	–	674	PWR
BD244A	SSD-204	213	–	674	PWR
BD244B	SSD-204	213	–	674	PWR
BD244C	SSD-204	213	–	674	PWR
BD277	SSD-204	189	–	667	PWR
BD278	SSD-204	129	–	668	PWR
BDX33	SSD-204	545	–	693	PWR
BDX33A	SSD-204	545	–	693	PWR
BDX33B	SSD-204	545	–	693	PWR
BDX33C	SSD-204	545	–	693	PWR
BDX34	SSD-204	551	–	694	PWR
BDX34A	SSD-204	551	–	694	PWR
BDX34B	SSD-204	551	–	694	PWR
BDX34C	SSD-204	551	–	694	PWR
BFT19	SSD-204	298	–	683	PWR
BFT19A	SSD-204	298	–	683	PWR
BFT19B	SSD-204	298	–	683	PWR
BU106	SSD-204	363	–	716	PWR
CA108AS	SSD-201	105	CDL-820	621	LIC
CA108AT	SSD-201	105	CDL-820	621	LIC
CA108S	SSD-201	105	CDL-820	621	LIC
CA108T	SSD-201	105	CDL-820	621	LIC
CA208AS	SSD-201	105	CDL-820	621	LIC
CA208AT	SSD-201	105	CDL-820	621	LIC
CA208S	SSD-201	105	CDL-820	621	LIC
CA208T	SSD-201	105	CDL-820	621	LIC
CA308AS	SSD-201	105	CDL-820	621	LIC
CA308AT	SSD-201	105	CDL-820	621	LIC
CA308H	SSD-201	590	CDL-820	516	LIC
CA308S	SSD-201	105	CDL-820	621	LIC
CA308T	SSD-201	105	CDL-820	621	LIC
CA741/1-4	SSD-207	188	–	718	LIC
CA741CH	SSD-201	590	CDL-820	516	LIC
CA741CS	SSD-201	74	CDL-820	531	LIC
CA741CT	SSD-201	74	CDL-820	531	LIC
CA741L	SSD-201	605	CDL-820	515	LIC
CA741S	SSD-201	74	CDL-820	531	LIC
CA741T	SSD-201	74	CDL-820	531	LIC
CA747/1-4	SSD-207	188	–	718	LIC
CA747CE	SSD-201	74	CDL-820	531	LIC
CA747CF	SSD-201	74	CDL-820	531	LIC
CA747CH	SSD-201	590	CDL-820	516	LIC
CA747CT	SSD-201	74	CDL-820	531	LIC
CA747E	SSD-201	74	CDL-820	531	LIC
CA747F	SSD-201	74	CDL-820	531	LIC
CA747T	SSD-201	74	CDL-820	531	LIC
CA748/1-4	SSD-207	188	–	718	LIC
CA748CH	SSD-201	590	CDL-820	516	LIC
CA748CS	SSD-201	74	CDL-820	531	LIC
CA748CT	SSD-201	74	CDL-820	531	LIC
CA748S	SSD-201	74	CDL-820	531	LIC
CA748T	SSD-201	74	CDL-820	531	LIC
CA1398E	SSD-201	573	CDL-820	686	LIC
CA1458S	SSD-201	74	CDL-820	531	LIC
CA1458T	SSD-201	74	CDL-820	531	LIC
CA1541D	SSD-201	395	CDL-820	536	LIC
CA1541H	SSD-201	590	CDL-820	516	LIC
CA1558/1-4	SSD-207	188	CDL-820	718	LIC
CA1558S	SSD-201	74	CDL-820	531	LIC
CA1558T	SSD-201	74	CDL-820	531	LIC
CA2111AE	SSD-201	520	CDL-820	612	LIC
CA2111AQ	SSD-201	520	CDL-820	612	LIC
CA3000	SSD-201	288	CDL-820	121	LIC
CA3000/1-4	SSD-207	196	–	705	LIC
CA3000H	SSD-201	590	CDL-820	516	LIC
CA3001	SSD-201	294	CDL-820	122	LIC
CA3001/1-4	SSD-207	203	–	714	LIC
CA3001H	SSD-201	590	CDL-820	516	LIC
CA3002	SSD-201	256	CDL-820	123	LIC
CA3002/1-4	SSD-207	210	–	713	LIC
CA3002H	SSD-201	590	CDL-820	516	LIC
CA3004	SSD-201	300	CDL-820	124	LIC
CA3004/1-4	SSD-207	216	–	712	LIC
CA3005	SSD-201	306	CDL-820	125	LIC
CA3005H	SSD-201	590	CDL-820	516	LIC
CA3006	SSD-201	306	CDL-820	125	LIC
CA3007	SSD-201	313	CDL-820	126	LIC
CA3008	SSD-201	80	CDL-820	316	LIC
CA3008A	SSD-201	89	CDL-820	310	LIC
CA3010	SSD-201	80	CDL-820	316	LIC
CA3010A	SSD-201	89	CDL-820	310	LIC
CA3011	SSD-201	262	CDL-820	128	LIC
CA3012	SSD-201	262	CDL-820	128	LIC
CA3012H	SSD-201	590	CDL-820	516	LIC
CA3013	SSD-201	471	CDL-820	129	LIC
CA3014	SSD-201	471	CDL-820	129	LIC
CA3015	SSD-201	80	CDL-820	316	LIC
CA3015A	SSD-201	89	CDL-820	310	LIC
CA3015A/1-4	SSD-207	222	–	715	LIC
CA3015H	SSD-201	590	CDL-820	516	LIC
CA3015L	SSD-201	605	CDL-820	515	LIC
CA3016	SSD-201	80	CDL-820	316	LIC
CA3016A	SSD-201	89	CDL-820	310	LIC
CA3018	SSD-201	160	CDL-820	338	LIC
CA3018A	SSD-201	160	CDL-820	338	LIC
CA3018H	SSD-201	590	CDL-820	516	LIC
CA3018L	SSD-201	605	CDL-820	515	LIC
CA3019	SSD-201	118	CDL-820	236	LIC
CA3019/1-4	SSD-207	229	–	722	LIC
CA3019H	SSD-201	590	CDL-820	516	LIC
CA3020	SSD-201	268	CDL-820	339	LIC
CA3020A	SSD-201	268	CDL-820	339	LIC
CA3020H	SSD-201	590	CDL-820	516	LIC
CA3021	SSD-201	276	CDL-820	243	LIC
CA3022	SSD-201	276	CDL-820	243	LIC
CA3023	SSD-201	276	CDL-820	243	LIC
CA3023H	SSD-201	590	CDL-820	516	LIC
CA3026	SSD-201	226	CDL-820	388	LIC
CA3026/1-4	SSD-207	235	–	706	LIC
CA3026H	SSD-201	590	CDL-820	516	LIC
CA3028A	SSD-201	318	CDL-820	382	LIC
CA3028AF	SSD-201	318	CDL-820	382	LIC
CA3028AH	SSD-201	590	CDL-820	516	LIC
CA3028AL	SSD-201	605	CDL-820	515	LIC
CA3028AS	SSD-201	318	CDL-820	382	LIC
CA3028B	SSD-201	318	CDL-820	382	LIC
CA3028B/1-4	SSD-207	243	–	711	LIC
CA3028BF	SSD-201	318	CDL-820	382	LIC
CA3028BS	SSD-201	318	CDL-820	382	LIC
CA3029	SSD-201	80	CDL-820	316	LIC
CA3029A	SSD-201	89	CDL-820	310	LIC
CA3030	SSD-201	80	CDL-820	316	LIC
CA3030A	SSD-201	89	CDL-820	310	LIC
CA3033	SSD-201	61	CDL-820	360	LIC
CA3033A	SSD-201	61	CDL-820	360	LIC
CA3033H	SSD-201	590	CDL-820	516	LIC
CA3035	SSD-201	243	CDL-820	274	LIC
CA3035H	SSD-201	590	CDL-820	516	LIC
CA3035V1	SSD-201	243	CDL-820	274	LIC
CA3036	SSD-201	158	CDL-820	275	LIC
CA3037	SSD-201	80	CDL-820	316	LIC
CA3037A	SSD-201	89	CDL-820	310	LIC
CA3038	SSD-201	80	CDL-820	316	LIC
CA3038A	SSD-201	89	CDL-820	310	LIC
CA3039	SSD-201	122	CDL-820	343	LIC
CA3039/1-4	SSD-207	250	–	704	LIC

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
CA3039H	SSD-201	590	CDL-820	516	LIC
CA3039L	SSD-201	605	CDL-820	515	LIC
CA3040	SSD-201	282	CDL-820	363	LIC
CA3041	SSD-201	498	CDL-820	318	LIC
CA3042	SSD-201	506	CDL-820	319	LIC
CA3043	SSD-201	466	CDL-820	331	LIC
CA3043H	SSD-201	590	CDL-820	516	LIC
CA3044	SSD-201	484	CDL-820	340	LIC
CA3044V1	SSD-201	484	CDL-820	340	LIC
CA3045	SSD-201	177	CDL-820	341	LIC
CA3045/1-4	SSD-207	255	–	710	LIC
CA3045F	SSD-201	177	CDL-820	341	LIC
CA3045H	SSD-201	590	CDL-820	516	LIC
CA3045L	SSD-201	605	CDL-820	515	LIC
CA3046	SSD-201	177	CDL-820	341	LIC
CA3047	SSD-201	61	CDL-820	360	LIC
CA3047A	SSD-201	61	CDL-820	360	LIC
CA3048	SSD-201	247	CDL-820	377	LIC
CA3048H	SSD-201	590	CDL-820	516	LIC
CA3049/1-4	SSD-207	263	–	707	LIC
CA3049H	SSD-201	590	CDL-820	516	LIC
CA3049L	SSD-201	605	CDL-820	515	LIC
CA3049T	SSD-201	234	CDL-820	611	LIC
CA3050	SSD-201	329	CDL-820	361	LIC
CA3051	SSD-201	329	CDL-820	361	LIC
CA3052	SSD-201	432	CDL-820	387	LIC
CA3053	SSD-201	318	CDL-820	382	LIC
CA3053F	SSD-201	318	CDL-820	382	LIC
CA3053S	SSD-201	318	CDL-820	382	LIC
CA3054	SSD-201	226	CDL-820	388	LIC
CA3054H	SSD-201	590	CDL-820	516	LIC
CA3054L	SSD-201	605	CDL-820	515	LIC
CA3058	SSD-201	338	CDL-820	490	LIC
CA3058/1-4	SSD-207	269	–	703	LIC
CA3059	SSD-201	338	CDL-820	490	LIC
CA3059H	SSD-201	590	CDL-820	516	LIC
CA3060AD	SSD-201	38	CDL-820	537	LIC
CA3060BD	SSD-201	38	CDL-820	537	LIC
CA3060D	SSD-201	38	CDL-820	537	LIC
CA3060E	SSD-201	38	CDL-820	537	LIC
CA3060H	SSD-201	590	CDL-820	516	LIC
CA3062	SSD-201	367	CDL-820	421	LIC
CA3064	SSD-201	490	CDL-820	396	LIC
CA3064E	SSD-201	490	CDL-820	396	LIC
CA3065	SSD-201	514	CDL-820	412	LIC
CA3066	SSD-201	533	CDL-820	466	LIC
CA3067	SSD-201	533	CDL-820	466	LIC
CA3068	SSD-201	525	CDL-820	467	LIC
CA3070	SSD-201	549	CDL-820	468	LIC
CA3071	SSD-201	549	CDL-820	468	LIC
CA3072	SSD-201	549	CDL-820	468	LIC
CA3075	SSD-201	462	CDL-820	429	LIC
CA3075H	SSD-201	590	CDL-820	516	LIC
CA3076	SSD-201	479	CDL-820	430	LIC
CA3076H	SSD-201	590	CDL-820	516	LIC
CA3078AS	SSD-201	52	CDL-820	535	LIC
CA3078AT	SSD-201	52	CDL-820	535	LIC
CA3078H	SSD-201	590	CDL-820	516	LIC
CA3078S	SSD-201	52	CDL-820	535	LIC
CA3078T	SSD-201	52	CDL-820	535	LIC
CA3079	SSD-201	338	CDL-820	490	LIC
CA3080	SSD-201	30	CDL-820	475	LIC
CA3080/1-4	SSD-207	277	–	709	LIC
CA3080A	SSD-201	30	CDL-820	475	LIC
CA3080A/1-4	SSD-207	277	–	709	LIC
CA3080AS	SSD-201	30	CDL-820	475	LIC
CA3080H	SSD-201	590	CDL-820	516	LIC
CA3080S	SSD-201	30	CDL-820	475	LIC
CA3081	SSD-201	126	CDL-820	480	LIC
CA3081F	SSD-201	126	CDL-820	480	LIC
CA3081H	SSD-201	590	CDL-820	516	LIC
CA3082	SSD-201	126	CDL-820	480	LIC
CA3082F	SSD-201	126	CDL-820	480	LIC
CA3082H	SSD-201	590	CDL-820	516	LIC
CA3083	SSD-201	130	CDL-820	481	LIC
CA3083F	SSD-201	130	CDL-820	481	LIC
CA3083H	SSD-201	590	CDL-820	516	LIC
CA3083L	SSD-201	605	CDL-820	515	LIC
CA3084	SSD-201	134	CDL-820	482	LIC
CA3084H	SSD-201	590	CDL-820	516	LIC
CA3084L	SSD-201	605	CDL-820	515	LIC
CA3085	SSD-201	375	CDL-820	491	LIC
CA3085/1-4	SSD-207	285	–	708	LIC
CA3085A	SSD-201	375	CDL-820	491	LIC
CA3085A/1-4	SSD-207	285	–	708	LIC
CA3085AF	SSD-201	375	CDL-820	491	LIC
CA3085AS	SSD-201	375	CDL-820	491	LIC
CA3085B	SSD-201	375	CDL-820	491	LIC
CA3085B/1-4	SSD-207	285	–	708	LIC
CA3085BF	SSD-201	375	CDL-820	491	LIC
CA3085BS	SSD-201	375	CDL-820	491	LIC
CA3085F	SSD-201	375	CDL-820	491	LIC
CA3085H	SSD-201	590	CDL-820	516	LIC
CA3085L	SSD-201	605	CDL-820	515	LIC
CA3085S	SSD-201	375	CDL-820	491	LIC
CA3086	SSD-201	183	CDL-820	483	LIC
CA3086F	SSD-201	183	CDL-820	483	LIC
CA3088E	SSD-201	446	CDL-820	560	LIC
CA3089E	SSD-201	455	CDL-820	561	LIC
CA3090AQ	SSD-201	440	CDL-820	684	LIC
CA3091D	SSD-201	383	CDL-820	534	LIC
CA3091H	SSD-201	590	CDL-820	516	LIC
CA3093E	SSD-201	152	CDL-820	533	LIC
CA3093H	SSD-201	590	CDL-820	516	LIC
CA3094/1-4	SSD-207	291	–	692	LIC
CA3094A/1-4	SSD-207	291	–	692	LIC
CA3094AT	SSD-201	346	CDL-820	598	LIC
CA3094B/1-4	SSD-207	291	–	692	LIC
CA3094BT	SSD-201	346	CDL-820	598	LIC
CA3094H	SSD-207	590	CDL-820	516	LIC
CA3094T	SSD-201	346	CDL-820	598	LIC
CA3095E	SSD-201	189	CDL-820	591	LIC
CA3096AE	SSD-201	141	CDL-820	595	LIC
CA3096E	SSD-201	141	CDL-820	595	LIC
CA3096H	SSD-201	590	CDL-820	516	LIC
CA3097E	SSD-201	199	CDL-820	633	LIC
CA3097H	SSD-201	590	CDL-820	516	LIC
CA3099E	SSD-201	359	CDL-820	620	LIC
CA3099H	SSD-201	590	CDL-820	516	LIC
CA3100H	SSD-201	590	CDL-820	516	LIC
CA3100S	SSD-201	98	CDL-820	625	LIC
CA3100T	SSD-201	98	CDL-820	625	LIC
CA3102E	SSD-201	234	CDL-820	611	LIC
CA3102H	SSD-201	590	CDL-820	516	LIC
CA3118AT	SSD-201	166	CDL-820	532	LIC
CA3118H	SSD-201	590	CDL-820	516	LIC
CA3118T	SSD-201	166	CDL-820	532	LIC
CA3120E	SSD-201	531	CDL-820	691	LIC
CA3121E	SSD-201	567	CDL-820	688	LIC
CA3123E	SSD-201	450	CDL-820	631	LIC
CA3125E	SSD-201	577	CDL-820	685	LIC
CA3126Q	SSD-201	565	CDL-820	Prel.	LIC
CA3140E	SSD-201	113	CDL-820	630	LIC
CA3140H	SSD-201	590	CDL-820	516	LIC
CA3146AE	SSD-201	166	CDL-820	532	LIC
CA3146E	SSD-201	166	CDL-820	532	LIC
CA3146H	SSD-201	590	CDL-820	516	LIC
CA3183AE	SSD-201	166	CDL-820	532	LIC
CA3183E	SSD-201	166	CDL-820	532	LIC
CA3183H	SSD-201	590	CDL-820	516	LIC
CA3401	SSD-201	113	CDL-820	630	LIC
CA3600E	SSD-201	213	CDL-820	619	LIC
CA6078AS	SSD-201	69	CDL-820	592	LIC
CA6078AT	SSD-201	69	CDL-820	592	LIC
CA6741S	SSD-201	69	CDL-820	592	LIC
CA6741T	SSD-201	69	CDL-820	592	LIC
CD2150	SSD-201	409	CDL-820	308	LIC
CD2151	SSD-201	409	CDL-820	308	LIC
CD2152	SSD-201	409	CDL-820	308	LIC
CD2153	SSD-201	409	CDL-820	308	LIC
CD2154	SSD-201	421	CDL-820	402	LIC
CD2500E	SSD-201	403	CDL-820	392	LIC
CD2501E	SSD-201	403	CDL-820	392	LIC
CD2502E	SSD-201	403	CDL-820	392	LIC
CD2503E	SSD-201	403	CDL-820	392	LIC
CD4000A/1-4	SSD-207	309	–	687	COS/MOS
CD4000AD	SSD-203	30	COS-278	479	COS/MOS
CD4000AE	SSD-203	30	COS-278	479	COS/MOS
CD4000AF	SSD-203	30	COS-278	479	COS/MOS
CD4000AH	SSD-203	307	COS-278	517	COS/MOS

Index to Devices

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
CD4000AK	SSD-203	30	COS-278	479	COS/MOS
CD4001A/1-4	SSD-207	309	–	687	COS/MOS
CD4001AD	SSD-203	30	COS-278	479	COS/MOS
CD4001AE	SSD-203	30	COS-278	479	COS/MOS
CD4001AF	SSD-203	30	COS-278	479	COS/MOS
CD4001AH	SSD-203	307	COS-278	517	COS/MOS
CD4001AK	SSD-203	30	COS-278	479	COS/MOS
CD4002A/1-4	SSD-207	309	–	687	COS/MOS
CD4002AD	SSD-203	30	COS-278	479	COS/MOS
CD4002AE	SSD-203	30	COS-278	479	COS/MOS
CD4002AF	SSD-203	30	COS-278	479	COS/MOS
CD4002AH	SSD-203	307	COS-278	517	COS/MOS
CD4002AK	SSD-203	30	COS-278	479	COS/MOS
CD4004A Series	Replaced by CD4024A Series				
CD4006A/1-4	SSD-207	316	–	689	COS/MOS
CD4006AD	SSD-203	37	COS-278	479	COS/MOS
CD4006AE	SSD-203	37	COS-278	479	COS/MOS
CD4006AF	SSD-203	37	COS-278	479	COS/MOS
CD4006AH	SSD-203	307	COS-278	517	COS/MOS
CD4006AK	SSD-203	37	COS-278	479	COS/MOS
CD4007A/1-4	SSD-207	321	–	695	COS/MOS
CD4007AD	SSD-203	43	COS-278	479	COS/MOS
CD4007AE	SSD-203	43	COS-278	479	COS/MOS
CD4007AF	SSD-203	43	COS-278	479	COS/MOS
CD4007AH	SSD-203	307	COS-278	517	COS/MOS
CD4007AK	SSD-203	43	COS-278	479	COS/MOS
CD4008A/1-4	SSD-207	327	–	696	COS/MOS
CD4008AD	SSD-203	49	COS-278	479	COS/MOS
CD4008AE	SSD-203	49	COS-278	479	COS/MOS
CD4008AF	SSD-203	49	COS-278	479	COS/MOS
CD4008AH	SSD-203	307	COS-278	517	COS/MOS
CD4008AK	SSD-203	49	COS-278	479	COS/MOS
CD4009A/1-4	SSD-207	332	–	719	COS/MOS
CD4009AD	SSD-203	54	COS-278	479	COS/MOS
CD4009AE	SSD-203	54	COS-278	479	COS/MOS
CD4009AH	SSD-203	307	COS-278	517	COS/MOS
CD4009AK	SSD-203	54	COS-278	479	COS/MOS
CD4010A/1-4	SSD-207	332	–	719	COS/MOS
CD4010AD	SSD-203	54	COS-278	479	COS/MOS
CD4010AE	SSD-203	54	COS-278	479	COS/MOS
CD4010AH	SSD-203	307	COS-278	517	COS/MOS
CD4010AK	SSD-203	54	COS-278	479	COS/MOS
CD4011A/1-4	SSD-207	339	–	717	COS/MOS
CD4011AD	SSD-203	61	COS-278	479	COS/MOS
CD4011AE	SSD-203	61	COS-278	479	COS/MOS
CD4011AF	SSD-203	61	COS-278	479	COS/MOS
CD4011AH	SSD-203	307	COS-278	517	COS/MOS
CD4011AK	SSD-203	61	COS-278	479	COS/MOS
CD4012A/1-4	SSD-207	339	–	717	COS/MOS
CD4012AD	SSD-203	61	COS-278	479	COS/MOS
CD4012AE	SSD-203	61	COS-278	479	COS/MOS
CD4012AF	SSD-203	61	COS-278	479	COS/MOS
CD4012AH	SSD-203	307	COS-278	517	COS/MOS
CD4012AK	SSD-203	61	COS-278	479	COS/MOS
CD4013A/1-4	SSD-207	346	–	697	COS/MOS
CD4013AD	SSD-203	68	COS-278	479	COS/MOS
CD4013AE	SSD-203	68	COS-278	479	COS/MOS
CD4013AF	SSD-203	68	COS-278	479	COS/MOS
CD4013AH	SSD-203	307	COS-278	517	COS/MOS
CD4013AK	SSD-203	68	COS-278	479	COS/MOS
CD4014A/1-4	SSD-207	352	–	720	COS/MOS
CD4014AD	SSD-203	74	COS-278	479	COS/MOS
CD4014AE	SSD-203	74	COS-278	479	COS/MOS
CD4014AF	SSD-203	74	COS-278	479	COS/MOS
CD4014AH	SSD-203	307	COS-278	517	COS/MOS
CD4014AK	SSD-203	74	COS-278	479	COS/MOS
CD4015A/1-4	SSD-207	357	–	721	COS/MOS
CD4015AD	SSD-203	79	COS-278	479	COS/MOS
CD4015AE	SSD-203	79	COS-278	479	COS/MOS
CD4015AF	SSD-203	79	COS-278	479	COS/MOS
CD4015AH	SSD-203	307	COS-278	517	COS/MOS
CD4015AK	SSD-203	79	COS-278	479	COS/MOS
CD4016A/1-4	SSD-207	362	–	744	COS/MOS
CD4016AD	SSD-203	84	COS-278	479	COS/MOS
CD4016AE	SSD-203	84	COS-278	479	COS/MOS
CD4016AF	SSD-203	84	COS-278	479	COS/MOS
CD4016AH	SSD-203	307	COS-278	517	COS/MOS
CD4016AK	SSD-203	84	COS-278	479	COS/MOS
CD4017A/1-4	SSD-207	370	–	741	COS/MOS
CD4017AD	SSD-203	90	COS-278	479	COS/MOS
CD4017AE	SSD-203	90	COS-278	479	COS/MOS
CD4017AF	SSD-203	90	COS-278	479	COS/MOS
CD4017AH	SSD-203	307	COS-278	517	COS/MOS
CD4017AK	SSD-203	90	COS-278	479	COS/MOS
CD4018A/1-4	SSD-207	375	–	742	COS/MOS
CD4018AD	SSD-203	95	COS-278	479	COS/MOS
CD4018AE	SSD-203	95	COS-278	479	COS/MOS
CD4018AF	SSD-203	95	COS-278	479	COS/MOS
CD4018AH	SSD-203	307	COS-278	517	COS/MOS
CD4018AK	SSD-203	95	COS-278	479	COS/MOS
CD4019A/1-4	SSD-207	380	–	743	COS/MOS
CD4019AD	SSD-203	100	COS-278	479	COS/MOS
CD4019AE	SSD-203	100	COS-278	479	COS/MOS
CD4019AF	SSD-203	100	COS-278	479	COS/MOS
CD4019AH	SSD-203	307	COS-278	517	COS/MOS
CD4019AK	SSD-203	100	COS-278	479	COS/MOS
CD4020A/1-4	SSD-207	384	–	750	COS/MOS
CD4020AD	SSD-203	105	COS-278	479	COS/MOS
CD4020AE	SSD-203	105	COS-278	479	COS/MOS
CD4020AF	SSD-203	105	COS-278	479	COS/MOS
CD4020AH	SSD-203	307	COS-278	517	COS/MOS
CD4020AK	SSD-203	105	COS-278	479	COS/MOS
CD4021A/1-4	SSD-207	389	–	730	COS/MOS
CD4021AD	SSD-203	110	COS-278	479	COS/MOS
CD4021AE	SSD-203	110	COS-278	479	COS/MOS
CD4021AF	SSD-203	110	COS-278	479	COS/MOS
CD4021AH	SSD-203	307	COS-278	517	COS/MOS
CD4021AK	SSD-203	110	COS-278	479	COS/MOS
CD4022A/1-4	SSD-207	394	–	731	COS/MOS
CD4022AD	SSD-203	115	COS-278	479	COS/MOS
CD4022AE	SSD-203	115	COS-278	479	COS/MOS
CD4022AF	SSD-203	115	COS-278	479	COS/MOS
CD4022AH	SSD-203	307	COS-278	517	COS/MOS
CD4022AK	SSD-203	115	COS-278	479	COS/MOS
CD4023A/1-4	SSD-207	339	–	717	COS/MOS
CD4023AD	SSD-203	61	COS-278	479	COS/MOS
CD4023AE	SSD-203	61	COS-278	479	COS/MOS
CD4023AF	SSD-203	61	COS-278	479	COS/MOS
CD4023AH	SSD-203	307	COS-278	517	COS/MOS
CD4023AK	SSD-203	61	COS-278	479	COS/MOS
CD4024A/1-4	SSD-207	399	–	732	COS/MOS
CD4024AD	SSD-203	120	COS-278	503	COS/MOS
CD4024AE	SSD-203	120	COS-278	503	COS/MOS
CD4024AF	SSD-203	120	COS-278	503	COS/MOS
CD4024AH	SSD-203	307	COS-278	517	COS/MOS
CD4025A/1-4	SSD-207	309	–	687	COS/MOS
CD4025AD	SSD-203	30	COS-278	479	COS/MOS
CD4025AE	SSD-203	30	COS-278	479	COS/MOS
CD4025AF	SSD-203	30	COS-278	479	COS/MOS
CD4025AH	SSD-203	307	COS-278	517	COS/MOS
CD4025AK	SSD-203	30	COS-278	479	COS/MOS
CD4026A/1-4	SSD-207	404	–	733	COS/MOS
CD4026AD	SSD-203	126	COS-278	503	COS/MOS
CD4026AE	SSD-203	126	COS-278	503	COS/MOS
CD4026AF	SSD-203	126	COS-278	503	COS/MOS
CD4026AH	SSD-203	307	COS-278	517	COS/MOS
CD4026AK	SSD-203	126	COS-278	503	COS/MOS
CD4027A/1-4	SSD-207	411	–	734	COS/MOS
CD4027AD	SSD-203	135	COS-278	503	COS/MOS
CD4027AE	SSD-203	135	COS-278	503	COS/MOS
CD4027AH	SSD-203	307	COS-278	517	COS/MOS
CD4027AK	SSD-203	135	COS-278	503	COS/MOS
CD4028A/1-4	SSD-207	417	–	735	COS/MOS
CD4028AD	SSD-203	141	COS-278	503	COS/MOS
CD4028AE	SSD-203	141	COS-278	503	COS/MOS
CD4028AF	SSD-203	141	COS-278	503	COS/MOS
CD4028AH	SSD-203	307	COS-278	517	COS/MOS
CD4028AK	SSD-203	141	COS-278	503	COS/MOS
CD4029A/1-4	SSD-207	421	–	736	COS/MOS
CD4029AD	SSD-203	146	COS-278	503	COS/MOS
CD4029AE	SSD-203	146	COS-278	503	COS/MOS
CD4029AH	SSD-203	307	COS-278	517	COS/MOS
CD4029AK	SSD-203	146	COS-278	503	COS/MOS
CD4030A/1-4	SSD-207	427	–	737	COS/MOS
CD4030AD	SSD-203	153	COS-278	503	COS/MOS
CD4030AE	SSD-203	153	COS-278	503	COS/MOS
CD4030AF	SSD-203	153	COS-278	503	COS/MOS
CD4030AH	SSD-203	307	COS-278	517	COS/MOS
CD4030AK	SSD-203	153	COS-278	503	COS/MOS
CD4031A/1-4	SSD-207	432	–	738	COS/MOS

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
CD4031AD	SSD-203	158	COS-278	569	COS/MOS
CD4031AE	SSD-203	158	COS-278	569	COS/MOS
CD4031AH	SSD-203	307	COS-278	517	COS/MOS
CD4031AK	SSD-203	158	COS-278	569	COS/MOS
CD4032A/1-4	SSD-207	438	–	739	COS/MOS
CD4032AD	SSD-203	164	COS-278	503	COS/MOS
CD4032AE	SSD-203	164	COS-278	503	COS/MOS
CD4032AH	SSD-203	307	COS-278	517	COS/MOS
CD4032AK	SSD-203	164	COS-278	503	COS/MOS
CD4033A/1-4	SSD-207	404	–	733	COS/MOS
CD4033AD	SSD-203	126	COS-278	503	COS/MOS
CD4033AE	SSD-203	126	COS-278	503	COS/MOS
CD4033AF	SSD-203	126	COS-278	503	COS/MOS
CD4033AH	SSD-203	307	COS-278	517	COS/MOS
CD4033AK	SSD-203	126	COS-278	503	COS/MOS
CD4034A/1-4	SSD-207	442	–	740	COS/MOS
CD4034AD	SSD-203	169	COS-278	575	COS/MOS
CD4034AE	SSD-203	169	COS-278	575	COS/MOS
CD4034AH	SSD-203	307	COS-278	517	COS/MOS
CD4034AK	SSD-203	169	COS-278	575	COS/MOS
CD4035A/1-4	SSD-207	449	–	751	COS/MOS
CD4035AD	SSD-203	177	COS-278	568	COS/MOS
CD4035AE	SSD-203	177	COS-278	568	COS/MOS
CD4035AH	SSD-203	307	COS-278	517	COS/MOS
CD4035AK	SSD-203	177	COS-278	568	COS/MOS
CD4036A/1-4	SSD-207	455	–	749	COS/MOS
CD4036AD	SSD-203	184	COS-278	613	COS/MOS
CD4036AE	SSD-203	184	COS-278	613	COS/MOS
CD4036AH	SSD-203	307	COS-278	517	COS/MOS
CD4036AK	SSD-203	184	COS-278	613	COS/MOS
CD4037AD	SSD-203	191	COS-278	576	COS/MOS
CD4037AE	SSD-203	191	COS-278	576	COS/MOS
CD4037AF	SSD-203	191	COS-278	576	COS/MOS
CD4037AH	SSD-203	307	COS-278	517	COS/MOS
CD4037AK	SSD-203	191	COS-278	576	COS/MOS
CD4038A/1-4	SSD-207	438	–	739	COS/MOS
CD4038AD	SSD-203	164	COS-278	503	COS/MOS
CD4038AE	SSD-203	164	COS-278	503	COS/MOS
CD4038AH	SSD-203	307	COS-278	517	COS/MOS
CD4038AK	SSD-203	164	COS-278	503	COS/MOS
CD4039A/1-4	SSD-207	455	–	749	COS/MOS
CD4039AD	SSD-203	184	COS-278	613	COS/MOS
CD4039AH	SSD-203	307	COS-278	517	COS/MOS
CD4039AK	SSD-203	184	COS-278	613	COS/MOS
CD4040A/1-4	SSD-207	461	–	748	COS/MOS
CD4040AD	SSD-203	197	COS-278	624	COS/MOS
CD4040AE	SSD-203	197	COS-278	624	COS/MOS
CD4040AF	SSD-203	197	COS-278	624	COS/MOS
CD4040AH	SSD-203	307	COS-278	517	COS/MOS
CD4040AK	SSD-203	197	COS-278	624	COS/MOS
CD4041A/1-4	SSD-207	469	–	753	COS/MOS
CD4041AD	SSD-203	203	COS-278	572	COS/MOS
CD4041AE	SSD-203	203	COS-278	572	COS/MOS
CD4041AH	SSD-203	307	COS-278	517	COS/MOS
CD4041AK	SSD-203	203	COS-278	572	COS/MOS
CD4042A/1-4	SSD-207	473	–	756	COS/MOS
CD4042AD	SSD-203	210	COS-278	589	COS/MOS
CD4042AE	SSD-203	210	COS-278	589	COS/MOS
CD4042AF	SSD-203	210	COS-278	589	COS/MOS
CD4042AH	SSD-203	307	COS-278	517	COS/MOS
CD4042AK	SSD-203	210	COS-278	589	COS/MOS
CD4043A/1-4	SSD-207	477	–	754	COS/MOS
CD4043AD	SSD-203	214	COS-278	590	COS/MOS
CD4043AE	SSD-203	214	COS-278	590	COS/MOS
CD4043AH	SSD-203	307	COS-278	517	COS/MOS
CD4043AK	SSD-203	214	COS-278	590	COS/MOS
CD4044A/1-4	SSD-207	477	–	754	COS/MOS
CD4044AD	SSD-203	214	COS-278	590	COS/MOS
CD4044AE	SSD-203	214	COS-278	590	COS/MOS
CD4044AH	SSD-203	307	COS-278	517	COS/MOS
CD4044AK	SSD-203	214	COS-278	590	COS/MOS
CD4045A/1-4	SSD-207	482	–	755	COS/MOS
CD4045AD	SSD-203	220	COS-278	614	COS/MOS
CD4045AE	SSD-203	220	COS-278	614	COS/MOS
CD4045AH	SSD-203	307	COS-278	517	COS/MOS
CD4045AK	SSD-203	220	COS-278	614	COS/MOS
CD4046A/1-4	SSD-207	487	–	752	COS/MOS
CD4046AD	SSD-203	226	COS-278	637	COS/MOS
CD4046AE	SSD-203	226	COS-278	637	COS/MOS
CD4046AH	SSD-203	307	COS-278	517	COS/MOS
CD4046AK	SSD-203	226	COS-278	637	COS/MOS
CD4047A/1-4	SSD-207	495	–	745	COS/MOS
CD4047AD	SSD-203	233	COS-278	623	COS/MOS
CD4047AE	SSD-203	233	COS-278	623	COS/MOS
CD4047AH	SSD-203	307	COS-278	517	COS/MOS
CD4047AK	SSD-203	233	COS-278	623	COS/MOS
CD4048A/1-4	SSD-207	506	–	747	COS/MOS
CD4048AD	SSD-203	244	COS-278	636	COS/MOS
CD4048AE	SSD-203	244	COS-278	636	COS/MOS
CD4048AH	SSD-203	307	COS-278	517	COS/MOS
CD4048AK	SSD-203	244	COS-278	636	COS/MOS
CD4049A/1-4	SSD-207	513	–	746	COS/MOS
CD4049AD	SSD-203	251	COS-278	599	COS/MOS
CD4049AE	SSD-203	251	COS-278	599	COS/MOS
CD4049AF	SSD-203	251	COS-278	599	COS/MOS
CD4049AH	SSD-203	307	COS-278	517	COS/MOS
CD4049AK	SSD-203	251	COS-278	599	COS/MOS
CD4050A/1-4	SSD-207	513	–	746	COS/MOS
CD4050AD	SSD-203	251	COS-278	599	COS/MOS
CD4050AE	SSD-203	251	COS-278	599	COS/MOS
CD4050AF	SSD-203	251	COS-278	599	COS/MOS
CD4050AH	SSD-203	307	COS-278	517	COS/MOS
CD4050AK	SSD-203	251	COS-278	599	COS/MOS
CD4051AD	SSD-203	258	COS-278	Prel.	COS/MOS
CD4051AE	SSD-203	258	COS-278	Prel.	COS/MOS
CD4051AK	SSD-203	258	COS-278	Prel.	COS/MOS
CD4052AD	SSD-203	258	COS-278	Prel.	COS/MOS
CD4052AE	SSD-203	258	COS-278	Prel.	COS/MOS
CD4052AK	SSD-203	258	COS-278	Prel.	COS/MOS
CD4053AD	SSD-203	258	COS-278	Prel.	COS/MOS
CD4053AE	SSD-203	258	COS-278	Prel.	COS/MOS
CD4053AK	SSD-203	258	COS-278	Prel.	COS/MOS
CD4054AD	SSD-203	266	COS-278	634	COS/MOS
CD4054AE	SSD-203	266	COS-278	634	COS/MOS
CD4054AH	SSD-203	307	COS-278	517	COS/MOS
CD4054AK	SSD-203	266	COS-278	634	COS/MOS
CD4055AD	SSD-203	266	COS-278	634	COS/MOS
CD4055AE	SSD-203	266	COS-278	634	COS/MOS
CD4055AK	SSD-203	266	COS-278	634	COS/MOS
CD4056AD	SSD-203	266	COS-278	634	COS/MOS
CD4056AE	SSD-203	266	COS-278	634	COS/MOS
CD4056AH	SSD-203	307	COS-278	517	COS/MOS
CD4056AK	SSD-203	266	COS-278	634	COS/MOS
CD4057AD	SSD-203	272	COS-278	635	COS/MOS
CD4057AH	SSD-203	307	COS-278	517	COS/MOS
CD4059A	SSD-203	285	COS-278	Prel.	COS/MOS
CD4061A	SSD-203	291	COS-278	Prel.	COS/MOS
CD4062A	SSD-203	295	COS-278	Prel.	COS/MOS
CD4066A	SSD-203	303	COS-278	Prel.	COS/MOS
CH2102	SSD-204	737	SPG-201	632	PWR
CH2270	SSD-204	737	SPG-201	632	PWR
CH2405	SSD-204	737	SPG-201	632	PWR
CH3053	SSD-204	737	SPG-201	632	PWR
CH3439	SSD-204	737	SPG-201	632	PWR
CH3440	SSD-204	737	SPG-201	632	PWR
CH4036	SSD-204	737	SPG-201	632	PWR
CH4037	SSD-204	737	SPG-201	632	PWR
CH5320	SSD-204	737	SPG-201	632	PWR
CH5321	SSD-204	737	SPG-201	632	PWR
CH5322	SSD-204	737	SPG-201	632	PWR
CH5323	SSD-204	737	SPG-201	632	PWR
CH5262	SSD-204	737	SPG-201	632	PWR
CH6479	SSD-204	737	SPG-201	632	PWR
D1201A	SSD-206	278	THC-500	495	RECT
D1201B	SSD-206	278	THC-500	495	RECT
D1201D	SSD-206	278	THC-500	495	RECT
D1201F	SSD-206	278	THC-500	495	RECT
D1201M	SSD-206	278	THC-500	495	RECT
D1201N	SSD-206	278	THC-500	495	RECT
D1201P	SSD-206	278	THC-500	495	RECT
D2101S	SSD-206	298	THC-500	522	RECT
D2103S	SSD-206	298	THC-500	522	RECT
D2103SF	SSD-206	298	THC-500	522	RECT
D2201A	SSD-206	313	THC-500	629	RECT
D2201B	SSD-206	313	THC-500	629	RECT
D2201D	SSD-206	313	THC-500	629	RECT
D2201F	SSD-206	313	THC-500	629	RECT
D2201M	SSD-206	313	THC-500	629	RECT
D2201N	SSD-206	313	THC-500	629	RECT
D2406A	SSD-206	318	THC-500	663	RECT

Index to Devices

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
D2406B	SSD-206	318	THC-500	663	RECT
D2406C	SSD-206	318	THC-500	663	RECT
D2406D	SSD-206	318	THC-500	663	RECT
D2406F	SSD-206	318	THC-500	663	RECT
D2406M	SSD-206	318	THC-500	663	RECT
D2412A	SSD-206	326	THC-500	664	RECT
D2412B	SSD-206	326	THC-500	664	RECT
D2412C	SSD-206	326	THC-500	664	RECT
D2412D	SSD-206	326	THC-500	664	RECT
D2412F	SSD-206	326	THC-500	664	RECT
D2412M	SSD-206	326	THC-500	664	RECT
D2520A	SSD 206	334	THC 500	665	RECT
D2520B	SSD-206	334	THC-500	665	RECT
D2520C	SSD-206	334	THC-500	665	RECT
D2520D	SSD-206	334	THC-500	665	RECT
D2520F	SSD-206	334	THC-500	665	RECT
D2520M	SSD-206	334	THC-500	665	RECT
D2540A	SSD-206	345	THC-500	580	RECT
D2540B	SSD-206	345	THC-500	580	RECT
D2540D	SSD-206	345	THC-500	580	RECT
D2540F	SSD-206	345	THC-500	580	RECT
D2540M	SSD-206	345	THC-500	580	RECT
D2601A	SSD-206	308	THC-500	723	RECT
D2601B	SSD-206	308	THC-500	723	RECT
D2601D	SSD-206	308	THC-500	723	RECT
D2601F	SSD-206	308	THC-500	723	RECT
D2601M	SSD-206	308	THC-500	723	RECT
D2601N	SSD-206	308	THC-500	723	RECT
D2600EF	SSD-206	303	THC-500	354	RECT
D2601DF	SSD-206	303	THC-500	354	RECT
D2601EF	SSD-206	303	THC-500	354	RECT
D3202Y	SSD-206	350	THC-500	577	DIAC
D3202U	SSD-206	350	THC-500	577	DIAC
HC2000H	SSD-204	744	–	566	HYB
HC2500	SSD-204	749	–	681	HYB
HR2N2857	SSD-207	83	–	–	RF
HR2N3866	SSD-207	85	–	–	RF
HR2N5090	SSD-207	87	–	–	RF
HR2N5470	SSD-207	89	–	–	RF
HR2N5916	SSD-207	91	–	–	RF
HR2N5918	SSD-207	93	–	–	RF
HR2N5919A	SSD-207	95	–	–	RF
HR2N5920	SSD-207	97	–	–	RF
HR2N5921	SSD-207	99	–	–	RF
HR2N6105	SSD-207	101	–	–	RF
HR2N6265	SSD-207	103	–	–	RF
HR2N6266	SSD-207	105	–	–	RF
HR2N6267	SSD-207	107	–	–	RF
HR2N6268	SSD-207	109	–	–	RF
HR2N6269	SSD-207	109	–	–	RF
HR2N6390	SSD-207	111	–	–	RF
HR2N6391	SSD-207	113	–	–	RF
HR2N6392	SSD-207	115	–	–	RF
HR2N6393	SSD-207	115	–	–	RF
HR2003	SSD-207	111	–	–	RF
HR2005	SSD-207	113	–	–	RF
HR2010	SSD-207	115	–	–	RF
HR3001	SSD-207	117	–	–	RF
HR3003	SSD-207	117	–	–	RF
HR3005	SSD-207	117	–	–	RF
JAN2N918	SSD-207	78	–	–	RF
JAN2N1482	SSD-207	26	–	–	PWR
JAN2N1486	SSD-207	26	–	–	PWR
JAN2N1490	SSD-207	27	–	–	PWR
JAN2N1493	SSD-207	78	–	–	RF
JAN2N2016	SSD-207	27	–	–	PWR
JAN2N2857	SSD-207	79	–	–	RF
JAN2N3055	SSD-207	28	–	–	PWR
JAN2N3375	SSD-207	80	–	–	RF
JAN2N3439	SSD-207	28	–	–	PWR
JAN2N3441	SSD-207	29	–	–	PWR
JAN2N3442	SSD-207	29	–	–	PWR
JAN2N3553	SSD-207	80	–	–	RF
JAN2N3585	SSD-207	30	–	–	PWR
JAN2N3772	SSD-207	30	–	–	PWR
JAN2N3866	SSD-207	81	–	–	RF
JAN2N4440	SSD-207	80	–	–	RF
JAN2N5038	SSD-207	31	–	–	PWR
JAN2N5071	SSD-207	81	–	–	RF
JAN2N5109	SSD-207	82	–	–	RF
JAN2N5416	SSD-207	31	–	–	PWR
JAN2N5672	SSD-207	32	–	–	PWR
JAN2N5840	SSD-207	32	–	–	PWR
JAN2N5918	SSD-207	82	–	–	RF
JAN2N6213	SSD-207	33	–	–	PWR
JANTX2N1486	SSD-207	26	–	–	PWR
JANTX2N2857	SSD-207	79	–	–	RF
JANTX2N3055	SSD-207	28	–	–	PWR
JANTX2N3375	SSD-207	80	–	–	RF
JANTX2N3439	SSD-207	28	–	–	PWR
JANTX2N3441	SSD-207	29	–	–	PWR
JANTX2N3553	SSD-207	80	–	–	RF
JANTX2N3585	SSD-207	30	–	–	PWR
JANTX2N4440	SSD-207	80	–	–	RF
JANTX2N5038	SSD-207	31	–	–	PWR
JANTX2N5071	SSD-207	81	–	–	RF
JANTX2N5109	SSD-207	82	–	–	RF
JANTX2N5416	SSD-207	31	–	–	PWR
JANTX2N5672	SSD-207	32	–	–	PWR
JANTX2N5840	SSD-207	32	–	–	PWR
JANTX2N6213	SSD-207	33	–	–	PWR
JANTXV2N3375	SSD-207	80	–	–	RF
JANTXV2N3553	SSD-207	80	–	–	RF
JANTXV2N4440	SSD-207	80	–	–	RF
R47M10	SSD-205	407	RFT-700	605	RF
R47M13	SSD-205	407	RFT-700	605	RF
R47M15	SSD-205	407	RFT-700	605	RF
RCA1A01	SSD-204	636	PTD-187	651	PWR
RCA1A02	SSD-204	636	PTD-187	651	PWR
RCA1A03	SSD-204	636	PTD-187	651	PWR
RCA1A04	SSD-204	636	PTD-187	651	PWR
RCA1A05	SSD-204	636	PTD-187	651	PWR
RCA1A06	SSD-204	636	PTD-187	651	PWR
RCA1A07	SSD-204	636	PTD-187	651	PWR
RCA1A08	SSD-204	636	PTD-187	651	PWR
RCA1A09	SSD-204	636	PTD-187	651	PWR
RCA1A10	SSD-204	636	PTD-187	651	PWR
RCA1A11	SSD-204	636	PTD-187	651	PWR
RCA1A15	SSD-204	636	PTD-187	651	PWR
RCA1A16	SSD-204	636	PTD-187	651	PWR
RCA1A17	SSD-204	636	PTD-187	651	PWR
RCA1A18	SSD-204	636	PTD-187	651	PWR
RCA1A19	SSD-204	636	PTD-187	651	PWR
RCA1B01	SSD-204	600	PTD-187	647	PWR
RCA1B04	SSD-204	618	PTD-187	649	PWR
RCA1B05	SSD-204	627	PTD-187	650	PWR
RCA1B06	SSD-204	609	PTD-187	648	PWR
RCA1C03	SSD-204	647	PTD-187	652	PWR
RCA1C04	SSD-204	647	PTD-187	652	PWR
RCA1C05	SSD-204	575	PTD-187	644	PWR
RCA1C06	SSD-204	575	PTD-187	644	PWR
RCA1C07	SSD-204	592	PTD-187	646	PWR
RCA1C08	SSD-204	592	PTD-187	646	PWR
RCA1C09	SSD-204	583	PTD-187	645	PWR
RCA1C10	SSD-204	558	PTD-187	642	PWR
RCA1C11	SSD-204	558	PTD-187	642	PWR
RCA1C12	SSD-204	647	PTD-187	652	PWR
RCA1C13	SSD-204	647	PTD-187	652	PWR
RCA1C14	SSD-204	566	PTD-187	643	PWR
RCA1E02	SSD-204	651	PTD-187	653	PWR
RCA1E03	SSD-204	651	PTD-187	653	PWR
RCA29	SSD-204	232	PTD-187	583	PWR
RCA29A	SSD-204	232	PTD-187	583	PWR
RCA29B	SSD-204	232	PTD-187	583	PWR
RCA29C	SSD-204	232	PTD-187	583	PWR
RCA30	SSD-204	237	PTD-187	584	PWR
RCA30A	SSD-204	237	PTD-187	584	PWR
RCA30B	SSD-204	237	PTD-187	584	PWR
RCA30C	SSD-204	237	PTD-187	584	PWR
RCA31	SSD-204	242	PTD-187	585	PWR
RCA31A	SSD-204	242	PTD-187	585	PWR
RCA31B	SSD-204	242	PTD-187	585	PWR
RCA31C	SSD-204	242	PTD-187	585	PWR
RCA32	SSD-204	247	PTD-187	586	PWR
RCA32A	SSD-204	247	PTD-187	586	PWR
RCA32B	SSD-204	247	PTD-187	586	PWR
RCA32C	SSD-204	247	PTD-187	586	PWR
RCA41	SSD-204	252	PTD-187	587	PWR
RCA41A	SSD-204	252	PTD-187	587	PWR
RCA41B	SSD-204	252	PTD-187	587	PWR

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
RCA41C	SSD-204	252	PTD-187	587	PWR
RCA42	SSD-204	257	PTD-187	588	PWR
RCA42A	SSD-204	257	PTD-187	588	PWR
RCA42B	SSD-204	257	PTD-187	588	PWR
RCA42C	SSD-204	257	PTD-187	588	PWR
RCA101	SSD-204	262	PTD-187	557	PWR
RCA102	SSD-204	262	PTD-187	557	PWR
RCA103	SSD-204	262	PTD-187	557	PWR
RCA104	SSD-204	262	PTD-187	557	PWR
RCA105	SSD-204	266	PTD-187	556	PWR
RCA201	SSD-204	262	PTD-187	557	PWR
RCA202	SSD-204	262	PTD-187	557	PWR
RCA203	SSD-204	262	PTD-187	557	PWR
RCA204	SSD-204	262	PTD-187	557	PWR
RCA205	SSD-204	266	PTD-187	556	PWR
RCA370	SSD-204	270	PTD-187	558	PWR
RCA371	SSD-204	270	PTD-187	558	PWR
RCA410	SSD-204	326	PTD-187	509	PWR
RCA411	SSD-204	332	PTD-187	510	PWR
RCA413	SSD-204	338	PTD-187	511	PWR
RCA423	SSD-204	344	PTD-187	512	PWR
RCA431	SSD-204	350	PTD-187	513	PWR
RCA520	SSD-204	270	PTD-187	558	PWR
RCA521	SSD-204	270	PTD-187	558	PWR
RCA1000	SSD-204	524	PTD-187	594	PWR
RCA1001	SSD-204	524	PTD-187	594	PWR
RCA2003	SSD-205	261	RFT-700	626	RF
RCA2005	SSD-205	265	RFT-700	627	RF
RCA2010	SSD-205	270	RFT-700	628	RF
RCA3001	SSD-205	401	RFT-700	657	RF
RCA3003	SSD-205	401	RFT-700	657	RF
RCA3005	SSD-205	401	RFT-700	657	RF
RCA3054	SSD-204	53	PTD-187	618	PWR
RCA3055	SSD-204	53	PTD-187	618	PWR
RCA3441	SSD-204	77	PTD-187	666	PWR
RCA6263	SSD-204	77	PTD-187	666	PWR
S2060A	SSD-206	138	THC-500	654	SCR
S2060B	SSD-206	138	THC-500	654	SCR
S2060C	SSD-206	138	THC-500	654	SCR
S2060D	SSD-206	138	THC-500	654	SCR
S2060E	SSD-206	138	THC-500	654	SCR
S2060F	SSD-206	138	THC-500	654	SCR
S2060M	SSD-206	138	THC-500	654	SCR
S2060Q	SSD-206	138	THC-500	654	SCR
S2060Y	SSD-206	138	THC-500	654	SCR
S2061A	SSD-206	138	THC-500	654	SCR
S2061B	SSD-206	138	THC-500	654	SCR
S2061C	SSD-206	138	THC-500	654	SCR
S2061D	SSD-206	138	THC-500	654	SCR
S2061E	SSD-206	138	THC-500	654	SCR
S2061F	SSD-206	138	THC-500	654	SCR
S2061M	SSD-206	138	THC-500	654	SCR
S2061Q	SSD-206	138	THC-500	654	SCR
S2061Y	SSD-206	138	THC-500	654	SCR
S2062A	SSD-206	138	THC-500	654	SCR
S2062B	SSD-206	138	THC-500	654	SCR
S2062C	SSD-206	138	THC-500	654	SCR
S2062D	SSD-206	138	THC-500	654	SCR
S2062E	SSD-206	138	THC-500	654	SCR
S2062F	SSD-206	138	THC-500	654	SCR
S2062M	SSD-206	138	THC-500	654	SCR
S2062Q	SSD-206	138	THC-500	654	SCR
S2062Y	SSD-206	138	THC-500	654	SCR
S2400A	SSD-206	151	THC-500	567	SCR
S2400B	SSD-206	151	THC-500	567	SCR
S2400D	SSD-206	151	THC-500	567	SCR
S2400M	SSD-206	151	THC-500	567	SCR
S2600B	SSD-206	156	THC-500	496	SCR
S2600D	SSD-206	156	THC-500	496	SCR
S2600M	SSD-206	156	THC-500	496	SCR
S2610B	SSD-206	156	THC-500	496	SCR
S2610D	SSD-206	156	THC-500	496	SCR
S2610M	SSD-206	156	THC-500	496	SCR
S2620B	SSD-206	156	THC-500	496	SCR
S2620D	SSD-206	156	THC-500	496	SCR
S2620M	SSD-206	156	THC-500	496	SCR
S2710B	SSD-206	164	THC-500	266	SCR
S2710D	SSD-206	164	THC-500	266	SCR
S2710M	SSD-206	164	THC-500	266	SCR
S2800A	SSD-206	166	THC-500	501	SCR
S2800B	SSD-206	166	THC-500	501	SCR
S2800D	SSD-206	166	THC-500	501	SCR
S3700B	SSD-206	172	THC-500	306	SCR
S3700D	SSD-206	172	THC-500	306	SCR
S3700M	SSD-206	172	THC-500	306	SCR
S3701M	SSD-206	192	THC-500	476	SCR
S3702SF	SSD-206	194	THC-500	522	SCR
S3703SF	SSD-206	194	THC-500	522	SCR
S3704A	SSD-206	180	THC-500	690	SCR
S3704B	SSD-206	180	THC-500	690	SCR
S3704D	SSD-206	180	THC-500	690	SCR
S3704M	SSD-206	180	THC-500	690	SCR
S3704S	SSD-206	180	THC-500	690	SCR
S3705M	SSD-206	187	THC-500	354	SCR
S3706M	SSD-206	187	THC-500	354	SCR
S3714A	SSD-206	180	THC-500	690	SCR
S3714B	SSD-206	180	THC-500	690	SCR
S3714D	SSD-206	180	THC-500	690	SCR
S3714M	SSD-206	180	THC-500	690	SCR
S3714S	SSD-206	180	THC-500	690	SCR
S3800D	SSD-206	199	THC-500	639	ITR
S3800E	SSD-206	199	THC-500	639	ITR
S3800EF	SSD-206	199	THC-500	639	ITR
S3800M	SSD-206	199	THC-500	639	ITR
S3800MF	SSD-206	199	THC-500	639	ITR
S3800S	SSD-206	199	THC-500	639	ITR
S3800SF	SSD-206	199	THC-500	639	ITR
S6200A	SSD-206	210	THC-500	418	SCR
S6200B	SSD-206	210	THC-500	418	SCR
S6200D	SSD-206	210	THC-500	418	SCR
S6200M	SSD-206	210	THC-500	418	SCR
S6210A	SSD-206	210	THC-500	418	SCR
S6210B	SSD-206	210	THC-500	418	SCR
S6210D	SSD-206	210	THC-500	418	SCR
S6210M	SSD-206	210	THC-500	418	SCR
S6220A	SSD-206	210	THC-500	418	SCR
S6220B	SSD-206	210	THC-500	418	SCR
S6220D	SSD-206	210	THC-500	418	SCR
S6220M	SSD-206	210	THC-500	418	SCR
S6400N	SSD-206	218	THC-500	578	SCR
S6410N	SSD-206	218	THC-500	578	SCR
S6420A	SSD-206	218	THC-500	578	SCR
S6420B	SSD-206	218	THC-500	578	SCR
S6420D	SSD-206	218	THC-500	578	SCR
S6420M	SSD-206	218	THC-500	578	SCR
S6420N	SSD-206	218	THC-500	578	SCR
S6431M	SSD-206	228	THC-500	247	SCR
S7430M	SSD-206	238	THC-500	408	SCR
S7432M	SSD-206	245	THC-500	724	SCR
T2300A	SSD-206	33	THC-500	470	TRI
T2300B	SSD-206	33	THC-500	470	TRI
T2300D	SSD-206	33	THC-500	470	TRI
T2301A	SSD-206	40	THC-500	431	TRI
T2301B	SSD-206	40	THC-500	431	TRI
T2301D	SSD-206	40	THC-500	431	TRI
T2302A	SSD-206	33	THC-500	470	TRI
T2302B	SSD-206	33	THC-500	470	TRI
T2302D	SSD-206	33	THC-500	470	TRI
T2304B	SSD-206	41	THC-500	441	TRI
T2304D	SSD-206	41	THC-500	441	TRI
T2305B	SSD-206	41	THC-500	441	TRI
T2305D	SSD-206	41	THC-500	441	TRI
T2306A	SSD-206	47	THC-500	406	TRI
T2306B	SSD-206	47	THC-500	406	TRI
T2306D	SSD-206	47	THC-500	406	TRI
T2310A	SSD-206	33	THC-500	470	TRI
T2310B	SSD-206	33	THC-500	470	TRI
T2310D	SSD-206	33	THC-500	470	TRI
T2311A	SSD-206	40	THC-500	431	TRI
T2311B	SSD-206	40	THC-500	431	TRI
T2311D	SSD-206	40	THC-500	431	TRI
T2312A	SSD-206	33	THC-500	470	TRI
T2312B	SSD-206	33	THC-500	470	TRI
T2312D	SSD-206	33	THC-500	470	TRI
T2313A	SSD-206	28	THC-500	414	TRI
T2313B	SSD-206	28	THC-500	414	TRI
T2313D	SSD-206	28	THC-500	414	TRI
T2313M	SSD-206	28	THC-500	414	TRI
T2316A	SSD-206	47	THC-500	406	TRI
T2316B	SSD-206	47	THC-500	406	TRI

Index to Devices

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
T2316D	SSD-206	47	THC-500	406	TRI
T2500B	SSD-206	49	THC-500	615	TRI
T2500D	SSD-206	49	THC-500	615	TRI
T2700B	SSD-206	62	THC-500	351	TRI
T2700D	SSD-206	62	THC-500	351	TRI
T2706B	SSD-206	47	THC-500	406	TRI
T2706D	SSD-206	47	THC-500	406	TRI
T2710B	SSD-206	62	THC-500	351	TRI
T2710D	SSD-206	62	THC-500	351	TRI
T2716B	SSD-206	47	THC-500	406	TRI
T2716D	SSD-206	47	THC-500	406	TRI
T2800B	SSD-206	69	THC-500	364	TRI
T2800D	SSD-206	69	THC-500	364	TRI
T2800M	SSD-206	69	THC-500	364	TRI
T2801DF	SSD-206	75	THC-500	493	TRI
T2806B	SSD-206	47	THC-500	406	TRI
T2806D	SSD-206	47	THC-500	406	TRI
T2850A	SSD-206	79	THC-500	540	TRI
T2850B	SSD-206	79	THC-500	540	TRI
T2850D	SSD-206	79	THC-500	540	TRI
T4100M	SSD-206	85	THC-500	458	TRI
T4101M	SSD-206	92	THC-500	457	TRI
T4103B	SSD-206	99	THC-500	443	TRI
T4103D	SSD-206	99	THC-500	443	TRI
T4104B	SSD-206	99	THC-500	443	TRI
T4104D	SSD-206	99	THC-500	443	TRI
T4105B	SSD-206	99	THC-500	443	TRI
T4105D	SSD-206	99	THC-500	443	TRI
T4106B	SSD-206	47	THC-500	406	TRI
T4106D	SSD-206	47	THC-500	406	TRI
T4107B	SSD-206	47	THC-500	406	TRI
T4107D	SSD-206	47	THC-500	406	TRI
T4110M	SSD-206	85	THC-500	458	TRI
T4111M	SSD-206	92	THC-500	457	TRI
T4113B	SSD-206	99	THC-500	443	TRI
T4113D	SSD-206	99	THC-500	443	TRI
T4114B	SSD-206	99	THC-500	443	TRI
T4114D	SSD-206	99	THC-500	443	TRI
T4115B	SSD-206	99	THC-500	443	TRI
T4115D	SSD-206	99	THC-500	443	TRI
T4116B	SSD-206	47	THC-500	406	TRI
T4116D	SSD-206	47	THC-500	406	TRI
T4117B	SSD-206	47	THC-500	406	TRI
T4117D	SSD-206	47	THC-500	406	TRI
T4120B	SSD-206	85	THC-500	458	TRI
T4120D	SSD-206	85	THC-500	458	TRI
T4120M	SSD-206	85	THC-500	458	TRI
T4121B	SSD-206	92	THC-500	457	TRI
T4121D	SSD-206	92	THC-500	457	TRI
T4121M	SSD-206	92	THC-500	457	TRI
T4706B	SSD-206	47	THC-500	406	TRI
T4706D	SSD-206	47	THC-500	406	TRI
T6400N	SSD-206	55	THC-500	593	TRI
T6401B	SSD-206	107	THC-500	459	TRI
T6401D	SSD-206	107	THC-500	459	TRI
T6401M	SSD-206	107	THC-500	459	TRI
T6404B	SSD-206	114	THC-500	487	TRI
T6404D	SSD-206	114	THC-500	487	TRI
T6405B	SSD-206	114	THC-500	487	TRI
T6405D	SSD-206	114	THC-500	487	TRI
T6406B	SSD-206	47	THC-500	406	TRI
T6406D	SSD-206	47	THC-500	406	TRI
T6406M	SSD-206	47	THC-500	406	TRI
T6407B	SSD-206	47	THC-500	406	TRI
T6407D	SSD-206	47	THC-500	406	TRI
T6407M	SSD-206	47	THC-500	406	TRI
T6410N	SSD-206	55	THC-500	593	TRI
T6411B	SSD-206	107	THC-500	459	TRI
T6411D	SSD-206	107	THC-500	459	TRI
T6411M	SSD-206	107	THC-500	459	TRI
T6414B	SSD-206	114	THC-500	487	TRI
T6414D	SSD-206	114	THC-500	487	TRI
T6415B	SSD-206	114	THC-500	487	TRI
T6415D	SSD-206	114	THC-500	487	TRI
T6416B	SSD-206	47	THC-500	406	TRI
T6416D	SSD-206	47	THC-500	406	TRI
T6416M	SSD-206	47	THC-500	406	TRI
T6417B	SSD-206	47	THC-500	406	TRI
T6417D	SSD-206	47	THC-500	406	TRI
T6417M	SSD-206	47	THC-500	406	TRI
T6420B	SSD-206	55	THC-500	593	TRI
T6420D	SSD-206	55	THC-206	593	TRI
T6420M	SSD-206	55	THC-500	593	TRI
T6420N	SSD-206	55	THC-500	593	TRI
T6421B	SSD-206	107	THC-500	459	TRI
T6421D	SSD-206	107	THC-500	459	TRI
T6421M	SSD-206	107	THC-500	459	TRI
T8401B	SSD-206	122	THC-500	725	TRI
T8401D	SSD-206	122	THC-500	725	TRI
T8401M	SSD-206	122	THC-500	725	TRI
T8411B	SSD-206	122	THC-500	725	TRI
T8411D	SSD-206	122	THC-500	725	TRI
T8411M	SSD-206	122	THC-500	725	TRI
T8421B	SSD-206	122	THC-500	725	TRI
T8421D	SSD-206	122	THC-500	725	TRI
T8421M	SSD-206	122	THC-500	725	TRI
T8430B	SSD-206	130	THC-500	549	TRI
T8430D	SSD-206	130	THC-500	549	TRI
T8430M	SSD-206	130	THC-500	549	TRI
T8440B	SSD-206	130	THC-500	549	TRI
T8440D	SSD-206	130	THC-500	549	TRI
T8440M	SSD-206	130	THC-500	549	TRI
T8450B	SSD-206	130	THC-500	549	TRI
T8450D	SSD-206	130	THC-500	549	TRI
T8450M	SSD-206	130	THC-500	549	TRI